High Density ST-MRAM Technology (Invited)

J.M. Slaughter, N.D. Rizzo, J. Janesky, R. Whig, F.B. Mancoff, D. Houssameddine, J.J. Sun, S. Aggarwal, K. Nagel, S. Deshpande, S.M. Alam, T. Andre and P. LoPresti
Everspin Technologies, Inc., Chandler, Arizona 85224 (USA)
Phone: (480) 347-1111, FAX: (480) 347-1175, email: jon.slaughter@everspin.com

Abstract

We review key properties for commercial ST-MRAM circuits, discuss the challenges to achieving the many performance and scaling goals that are being addressed in current development around the world, recent results in the field, and present first results from a new, fully-functional 64Mb, DDR3, ST-MRAM circuit.

Introduction

Spin-torque Magnetoresistive Random Access Memory (ST-MRAM) is being developed for a number of purposes: extending MRAM technology to densities beyond those achieved with Toggle switching, enabling embedded nonvolatile memory with a small cell size, and as an eventual successor to high-density DRAM with the potential to solve extreme scaling problems.

Fig. 1 shows typical memory cells for Toggle MRAM, the field-switched technology in production today at Everspin, and ST-MRAM, both with a one magnetic tunnel junction (MTJ) and a pass transistor per cell. In both cells the data is stored in the magnetic state of the MTJ and read back by sensing the corresponding resistance of the MTJ. In Toggle MRAM, the free layer magnetization is switched by a magnetic field created by current pulses through adjacent write lines and the transistor only passes the read current. This separation of read and write current paths has advantages, but scaling of field-switched MRAM is generally difficult. In ST-MRAM a write current is passed directly through the MTJ that switches the free layer magnetization by spin torque transfer (1,2), creating the additional requirement that the pass transistor be sized to support the required current.

The basic scaling argument for ST-MRAM is illustrated in Fig. 2. If the critical current density for spin-torque

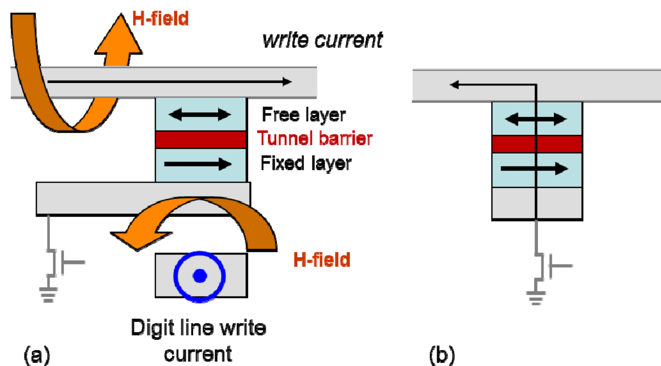

Figure 1. Cell diagrams of a) Toggle MRAM and b) 1T-1MTJ ST-MRAM under development. Toggle MRAM switches with magnetic fields from current in nearby lines; ST-MRAM uses spin torque from the spin-polarized tunneling current.

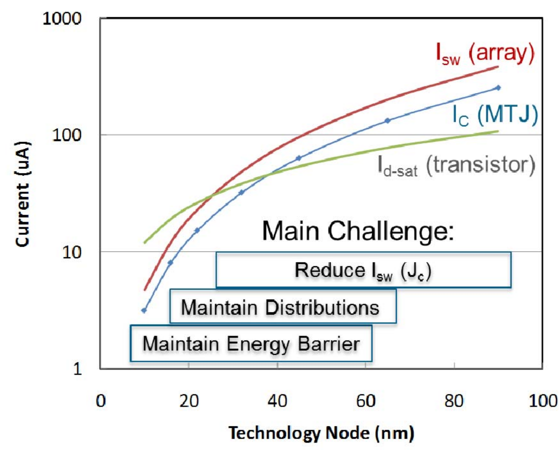

Figure 2. I_C and associated I_{SW} calculated for spin-torque switching of MTJ arrays assuming J_C can be held constant while scaling. Id-sat is assumed to be ~700µA per µm of width, independent of node.

switching (J_c) can be held constant, then compatibility with a minimum-size transistor improves with decreasing feature size, λ, since the critical current for switching, I_c, will scale as λ^2 while the saturation current, $I_{d\text{-}sat}$, of a minimum-size transistor scales as λ. However, there are a number of challenges to achieving this ideal behavior, some of which are described below.

Significant results from several ST-MRAM demonstration circuits have been published, beginning with a 4kb test vehicle in 2005 (3) followed by many others including: a 2Mb circuit and device data in 2007 (4), statistical data on 4 kb integrated arrays with 70×210 nm^2 bits (5) and devices with perpendicular magnetization (6) in 2008, arrays integrated with 54nm CMOS technology (7) and perpendicular bit switching in 2010 (8), and single-bit data for 20nm diameter perpendicular devices in 2011 (9). The continuous improvement reported in these papers, and many others, reflects significant innovation and progress toward the use of spin-torque switching in products.

Key Properties of ST-MRAM Devices

One key requirement for a fully functional ST-MRAM is achieving a critical voltage (V_c) distribution that is well separated from the tunnel barrier breakdown distribution. For a switching voltage *Vsw* that reliably switches Mbits without breakdown fails, at least 6σ separation is needed from V_{sw} to both distributions as shown in Fig. 3. In practice more is needed to allow for write voltage variation and time-dependent dielectric breakdown (TDDB) effects. Since the voltage required to breakdown a dielectric layer (V_{bd}) is

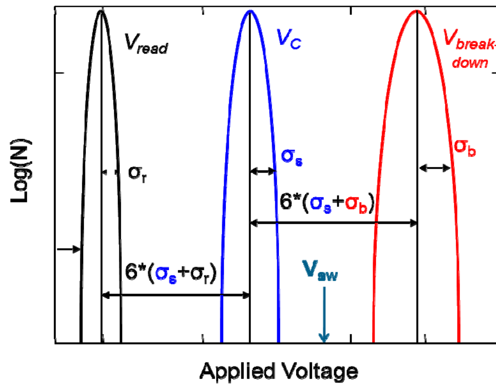

Figure 3. An illustration of key distributions in ST-MRAM arrays. The bit switching voltage (V_{sw}) must be separated from the V_C the V_{bd} distributions. To avoid disturbs, the read voltage V_{read} must not overlap V_C. Narrow distributions are critical for error-free operation.

reduced as the time at bias is increased, repeated cycling of the bias results in a shift of the breakdown distribution to the left, reducing separation from the V_C distribution. This TDDB effect is quite significant over the life of a part and extra single-cycle separation must be engineered into the devices to achieve the desired endurance. Fig. 4 shows experimental data for integrated arrays with over 30σ separation.

A low J_c is required for low V_C and also minimizes I_c, allowing a smaller pass transistor. Smaller MTJ area A also reduces I_c but measures must be taken to maintain data retention since energy barrier to switching (E_b) is approximately proportional to A. We have determined experimentally that E_b for in-plane magnetization is optimum for shaped bits with aspect ratio near 3. Small

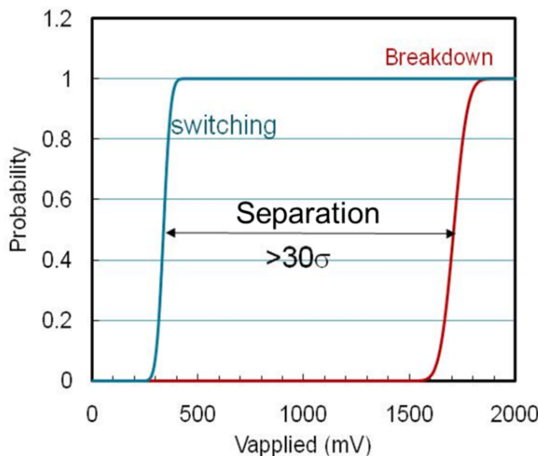

Figure 4. Probability of bit switching (AP-to-P) and tunnel barrier breakdown vs. applied voltage ($V_{applied}$) for bits with the optimized CoFeB-based free layer measured in kb ST-MRAM arrays integrated with CMOS with pulse duration t_p≈100ns. The separation between the switching and breakdown is >30σ.

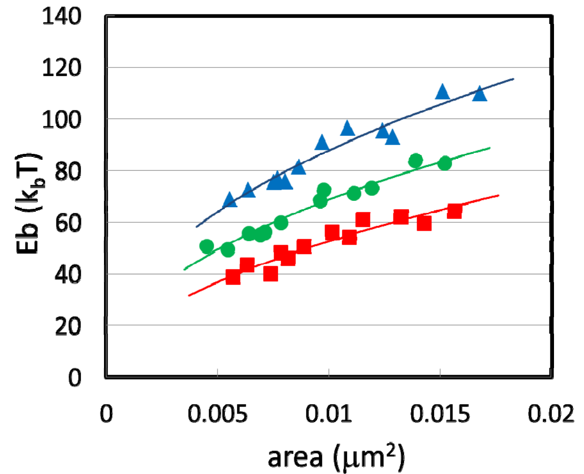

Figure 5. Energy barrier (measured with pulsed magnetic field) vs bit area and free layer thickness. Bits ranged from 50nm to 90nm ellipses with aspect ratio from 2.3 to 3.5. Thicknesses varied from baseline (green circles) + (triangles)/- (squares) 10% in total moment.

increases in thickness can increase E_b at the expense of somewhat higher V_C as shown experimentally in Fig. 5. An increase in saturation magnetization of only 10% can dramatically increase the energy barrier, for example from 60 k_BT to 80 k_BT. Since data retention time (τ) is exponentially dependent on E_b, the mean value of τ increases by 8 orders of magnitude with this small magnetization increase.

Recent developments in CoFeB-based perpendicular materials (10, 11) have renewed interest in perpendicular MTJ devices. These devices are of great practical interest because MTJ stacks based on CoFeB alloys and MgO tunnel barriers have already proven to have the highest MR values and meet many requirements for manufacturability. In devices with perpendicular magnetization, the strong perpendicular anisotropy from the CoFeB/MgO interface is used to create the large perpendicular anisotropy needed for the perpendicular free layer.

Theory predicts that free layers with a perpendicular easy axis may have a lower achievable J_c and a lower I_C for a given E_b. Experimental data has shown similar J_c values with both types, J_c≈3MA/cm^2, for E_b≈50-70k_bT. Since the energy barrier is related to the perpendicular magnetic anisotropy rather than bit shape, it is possible to use circular bits for potentially smaller cell sizes. Better I_C/E_b ratios have been demonstrated for perpendicular devices but, in many cases, with E_b values that seem to be limited to less than required. However, the rapid progress in perpendicular MTJ device properties over the past two years is continuing and providing evidence that I_C can be further reduced and E_b can be increased in practical devices (12-15). These recent reports describe CoFeB-based perpendicular MTJ devices with diameters between 20 nm and 70 nm having energy

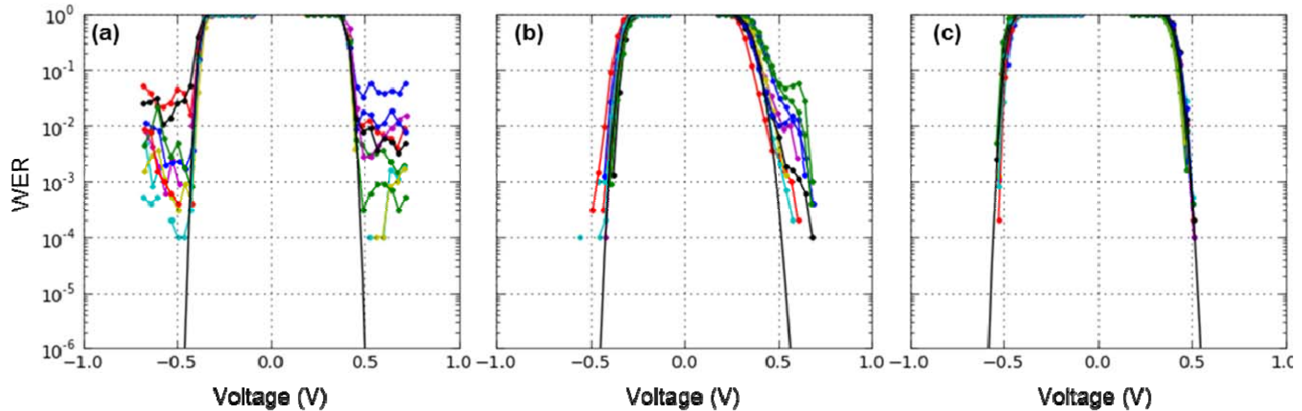

Figure 6. Write Error Rate (WER) out of 10,000 attempts for 9 bits, nominally 85nm x 240 nm, with write pulses of 25ns duration applied for (P-to-AP)(V<0) and AP-to-P (V>0) switching. The black line is a fit of the experimental data assuming a Gaussian distribution of WER. Each panel is a different free layer material

barriers enhanced by improved materials and patterning techniques.

Another key requirement for ST-MRAM is high quality switching. Fig. 6 shows the results of optimizing CoFeB-based, in-plane free layer materials for low error rates. The non-Gaussian behavior demonstrated by some of the un-optimized bits is an extrinsic mechanism that does not affect all bits. For example, the non-normal increase in error rate on the right side of Fig. 6b is seen in some bits, usually in only one bias direction (16), and has been termed "ballooning." Other bits seem to plateau at a certain error rate rather than continuing to decrease with increasing *Vsw*. Such effects are usually worse for shorter switching pulses, a behavior indicating magnetic defects in the free layer that create metastable magnetic states which interfere with switching. Optimized material dramatically reduces the occurrence of such switching and improves the intrinsic

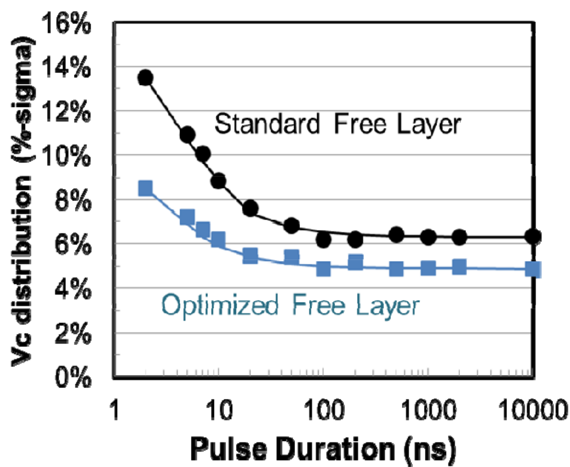

Figure 7. ST switching sigma (%) vs. pulse duration (ns) measured for a standard CoFeB based free layer (black circles) and an optimized CoFeB based free layer (blue squares). The data was taken on kb ST-MRAM arrays integrated with CMOS.

properties as seen by the well-behaved distributions and low bit-to-bit variation in Fig. 6c. The overall improvement in σ_{Vc} shown in Fig. 7, and particularly the improvement for short write pulses in the t_p<20 ns range, show clearly how improvements in the magnetic materials can improve the intrinsic switching behavior.

Recent progress in magnetic switching

In addition to developments in devices with perpendicular magnetization, described above, there are continuing advancements in ultra-thin magnetic films and devices that may find applications in future MRAM technology. Two exciting examples are electric field control of interfacial anisotropy and the generation of spin currents with the spin Hall effect (SHE). For example, spin-torque switching of both in-plane and perpendicular free layers using the SHE has already been demonstrated by Liu, et al. (17) and a transition from in-plane to perpendicular anisotropy was demonstrated in CoFeB/oxide systems by Kita, et al. (18)

The rapid pace of discovery in the fields of spintronics and MTJ devices/materials bodes well for continued improvements in MRAM technology. One can easily imagine approaches that combine new ways of controlling magnetic states with high tunneling magnetoresistance and spin-torque transfer to extend device scaling to smaller dimensions, reduce the energy needed to write, and provide additional degrees of freedom for circuit architectures.

64Mb DDR3 ST-MRAM

A 64Mb DDR3 ST-MRAM circuit (shown in Fig. 8) and a companion 16Mb test vehicle have been designed and fabricated using 90nm CMOS technology. Four standard Cu layers and one Al RDL layer are used with the MTJ located between M3 and M4. Packaged in a JEDEC standard DDR3 BGA, the 64Mb DDR3 ST-MRAM is compatible with

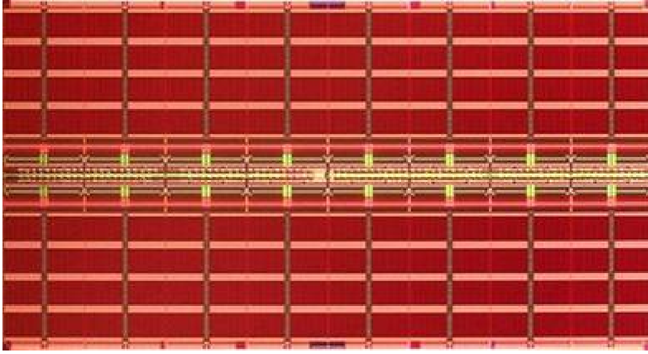

Figure 8. Everspin 64Mb DDR3 ST-MRAM Die Photo. Wordline drivers run vertically through the center of each of eight 8Mb banks. Strips of column circuits run horizontally, dividing each bank into 8 sub-arrays..

commercially available controllers. Supporting x4, x8, and x16 configurations, the 8-bank architecture minimizes initial latency while sustaining 1.6GT/s (DDR3-1600) sequential data rate.

With the optimized MTJ material described above, we have achieved full functionality of these 64Mb devices, which apply new circuit techniques to address specific challenges of ST-MRAM. Switching distributions for 256kb in our 16Mb ST-MRAM test vehicle are shown in Fig. 9. A 100% natural switching yield is achieved for both antiparallel-to-parallel and parallel-to-antiparallel switching.

Fig. 10 is a shows the operating region for up and down write bias using a March6N pattern run on the 64Mb device, demonstrating a large write window with zero fails for a range of applied write voltages.

We have demonstrated high speed DDR3 functionality by achieving zero fails on 64Mb devices with the March6N pattern at 1.5V VDD. Full functionality of these parts was further demonstrated using an evaluation board controlled by an industry standard FPGA.

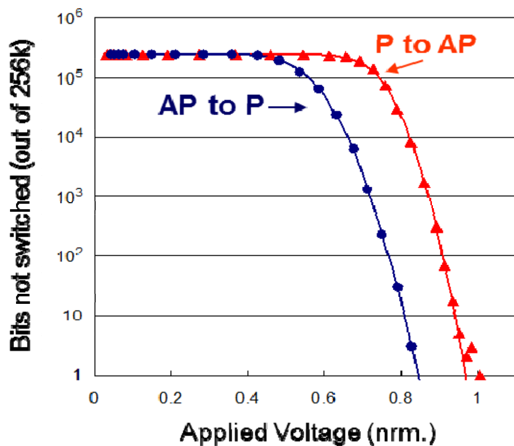

Figure 9. 256kb switching distributions from our 16Mb ST-MRAM test vehicle for both AP-to-P (blue) and P-to-AP (red) directions with applied switching voltage in arbitrary units. The write voltage pulse duration was 50ns. The solid lines are error function fits to the data.

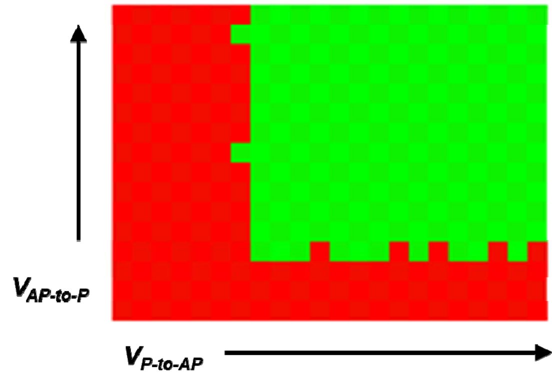

Figure 10. P-to-AP vs AP-to-P applied voltage shmoo plot for a March6N test pattern run on 16Mb within the 64Mb. Each square represents pass/fail, with green signifying 0 fails and red signifying >0 fails. The voltage step size is approximately 10mV and the origin is offset from zero for both axes.

Conclusion

Our results demonstrate high-quality switching and high performance for integrated arrays of CoFeB/MgO-based MTJ devices with in-plane magnetization. Initial results from a 64Mb circuit showing fully functional DDR3 operation is an important step toward the first ST-MRAM product introduction. Recent progress in perpendicular materials, SHE, and electric-field control of anisotropy show that there is great potential for continued improvement and scaling of MRAM technology.

References

1) J. C. Slonczewski, J. Magn. Magn. Mater. 159 L1 (1996).
2) L. Berger, Phys. Rev. B 54 9353 (1996).
3) M. Hosomi, et al., IEDM Tech. Dig. 459 (2005)..
4) T. Kawahara, et al., Proc. ISSCC, p. 480 (2007).
5) R. Beach, et al., IEDM Tech. Dig. 305 (2008),.
6) T. Kishi, et al., IEDM Tech. Dig., p. 1 (2008).
7) S. Chung, IEDM Tech. Dig.. 12.7.1 (2010).
8) D. C. Worledge, et al, IEDM Tech. Dig. 12.5.1 (2010).
9) W. Kim, et al., IEDM Tech. Dig. 24.1.1 (2011).
10) S. Ikeda et al., Nat. Mater. 9, p. 721 (2010).
11) D. C. Worledge et al., Appl. Phys. Lett. 98 022501 (2011).
12) H. Kubota et al., J. Appl. Phys. 111 07C723 (2012).
13) J.-H. Park et al., VLSI Technology, 57 (2012).
14) H. Sato, et al., Appl. Phys. Lett. 101 022414 (2012).
15) Guenole Jan, et al., Applied Physics Express 5 093008 (2012).
16) Tai Min, et al., IEEE Trans. Mag. 46, 2322 (2010).
17) Luqiao Liu, et al., Science 336, 555 (2012).
18) Koji Kita, et al., Appl. Phys. 112, 033919 (2012).