60GHz Passive and Active RF-path Phase Shifters in Silicon

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***Abstract* — Integrated 60-GHz active and passive phase shifters for RF-path phase-shifting phased array transceivers are demonstrated in this paper. The reflection-type passive phase shifter achieves >180° phase variation across the 57GHz-64GHz band with insertion loss varying from 4.2dB-7.5dB at 60GHz. The active phase shifter employs vector-interpolation architecture and achieves 360° phase variation, -2dB gain, 12GHz 3dB bandwidth and 16.5dB noise figure at 60GHz. Measurements over process and temperature are also discussed and comparisons are drawn between active and passive phase shifting approach for 60GHz phased arrays.**

***Index Terms* — Phase shifter, mm-wave, phased array**

I. Introduction

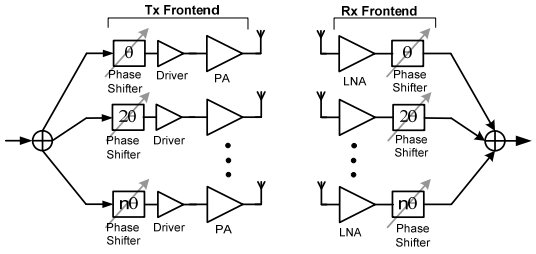
The market opportunity for 60GHz radio has been made apparent by the need for high-definition video and multi-Gbps data transfer across short distances in home and office. These applications require NLOS links that can be achieved using phased array transmitters and receivers, that enable electronic beamforming and beam steering. Integrated phased arrays implementations require variable phase shifters before signal combining (Rx) or after signal division (Tx). In this paper, we present the design of integrated 60GHz active and passive phase shifters and compare their performance in the context of their suitability for a RF-path phase shifting array architecture.

The phase shifters are implemented in the IBM 0.13-μm SiGe BiCMOS technology (the varactor-based passive phase shifter is CMOS compatible). The overall requirements and impact of phase shifter performance on the system are presented in Section II. The design of the passive phase shifter and vector interpolator are presented in Section III and Section IV respectively. The measured results of the RTPS and vector interpolator are discussed in the context of system architecture in Section V.

II. 60GHz Phased Array Transceiver

RF-path phase shifting and combining promises the lowest power solution for 60GHz wireless applications. Given the architecture in Fig. 1, the phase shifters in each element must provide 360° variable phase shift. Furthermore, the phase shifters are in the signal path and hence the phase shifter gain, noise figure and linearity impacts system performance as quantitatively shown in Fig. 1. In the Tx, loss in the phase shifter impacts the required driver gain and linearity and hence overall power consumption. It also influences the choice of distribution network as active stages may be required to compensate for the loss in the phase shifters. In the Rx, the noise figure of the phase shifter does not significantly impact front-end noise figure for typical values but the lower front-end gain increases sensitivity to mixer noise.

Both passive and active phase shifting topologies were studied during this work. The loss of passive phase shifters generally increases with phase shift range and it



Phase Shifter Performance	Driver Gain [dB]	Reqd. Driver P1dB [dBm]		Gain [dB]	NF [dB]
Gain: -3dB, NF: 15dB, P1dB,Inp: -10dBm	15	6		20	6.16
Gain: -10dB, NF: 10dB, P1dB,Inp: -5dBm	15	4		13	6.05
Gain: -15dB, NF: 15dB, P1dB,Inp: -5dBm	15	4		8	6.05

Fig 1. Impact of phase shifter performance on RF-path phase-shifting array transmitter and receiver.

was found that achieving full 360° phase variation with fine resolution from a passive phase shifter was too lossy. Since it is possible to achieve a discrete 180° phase shift in integrated Rx and Tx frontends by swapping differential signals, the phase variation requirement in the passive phase shifter was limited to 180° with a differential phase inverting stage providing the remaining 180° phase shift.

III. Reflection-Type Phase Shifter (RTPS)

Passive phase shifters are well-suited for arrays with large number of elements due to their low power consumption and high linearity. Architectures for passive phase shifters include switched transmission lines, loaded lines, and, high-pass low-pass phase shifters[1]. Silicon-based phase shifters in literature include a 24-GHz RTPS using transformer-based coupler [2] and a 60-GHz phase shifter based on varactor-loaded transmission lines[3]. The phase shifter in [3] achieved 8.5-10.3-dB insertion loss and 158° phase variation with MOS varactor Q of 15-45 in 65-nm CMOS technology. However, the high loss and <180° phase shift range makes it difficult to achieve 360° phase shift by cascading multiple RTPS stages or inserting a discrete 0/180 stage following the RTPS.

In this work, the focus of the RTPS design was to minimize loss while achieving at least 180° of phase shift across the 57GHz-64GHz band. The schematic of the designed RTPS is shown in Fig. 2. For a load with reactance X_L attached to the *coupled* and *through* ports of a quadrature coupler of impedance Z_o, the phase shift between *input* and *isolated (output)* ports is shown in Fig. 2. Thus, the phase shift through the RTPS varies with the

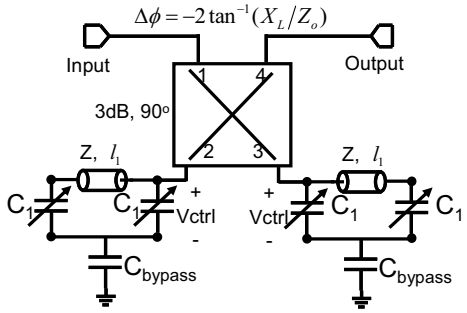


Fig. 2. Schematic of RTPS with π-type C-L-C load.

load reactance. In practical implementations, coupler loss and finite load quality factors result in RTPS insertion loss which increases with desired phase shift range.

1) *Low-loss 3-dB quadrature coupler*:

The key design parameters for the Lange coupler are the voltage coupling coefficient (c) and the even- and odd-mode characteristic impedances ($Z_{o,even}$ and $Z_{o,odd}$) of a 2-conductor coupled line, related by the equations shown in Fig. 3 [4]. The coupler was implemented in the thick top metal layer as opposed to [5] to achieve lower loss and tighter coupling. The 3um line spacing ensured good $Z_{o,even}$ to $Z_{o,odd}$ ratio with $Z_{o,even}$ = 92Ω and $Z_{o,odd}$ = 19Ω, which results in 42–Ω Z_o. Measurements show that the coupler achieves -3.7 dB to the through port and -4.1 dB to the coupled port at 60GHz indicating that the coupler insertion loss is 1.8 dB.

2) *Reflective load design*:

A π–type C-L-C load is used to achieve 180° continuous phase tuning in the RTPS (Fig. 4). For the load in Fig. 4, the effective reactance, X_{eff}, is given by,

$$X_{eff} = -\{\omega C_1[1-(1+\tan\beta l_1/C_1\omega Z)(C_1\omega Z\tan\beta l_1 - 1)^{-1}]\}^{-1} \quad (1)$$

where β, Z, and, l_1 are the propagation constant, impedance, and length of the transmission line and C_1 is the accumulation-mode varactor capacitance. Based on eqn. (1), the effective reactance can be varied from inductive to capacitive over the varactor tuning range to achieve desired phase shift variation. For the 0.24μm channel length MOS varactor in this process, the measured capacitance tuning ratio is around 2.8 with a quality factor that varies from 3 to 8. The simulated input impedance of the load with Z = 70Ω, L=440 μm and C_1 from 45*f*F to 130*f*F is shown in Fig. 4. The impedance location on the Smith chart is swept more than half circle, e.g. 180° by varying varactor capacitance. Ideally, the curve should be on the unit circle (|Γ|=1) of the Smith chart; however, the finite Q of the varactor dominates the insertion loss. The reflection loss of the reflective load (at $\omega L_{eff}=2/\omega C_1$; corresponding to imag($\Gamma_{load}$)=0) is given by,

$$|\Gamma_{load}| = |(F-Z_o)/(F+Z_o)|, \text{ where } F \simeq (1+Q_c^2)/(2\omega C_1 Q_c) \quad (2)$$

where the L_{eff} is the equivalent inductance of the transmission line. For the design values, C_1=50*f*F, and Q_c=6, the expected RTPS loss due to the finite-Q varactor is -5.5dB which is the dominant source of loss.

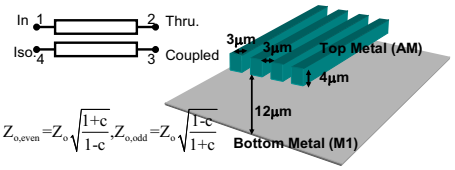


Fig. 3. Cross section view of Lange coupler using AM metal in IBM 0.13μm SiGe process.

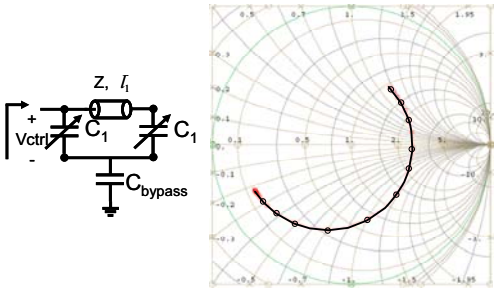


Fig. 4. Schematic and simulated input impedance of RTPS load at 60GHz for different control voltages.

IV. Active Vector Interpolator

The active phase shifter employs the vector interpolator architecture to achieve 360° phase shift range. The input is single-ended and is provided to a quadrature Lange coupler followed by Lange-Lange baluns to obtain broadband differential quadrature signals[6]. As shown in Fig. 5, vector interpolation is equivalent to summing the output of two variable-gain amplifiers that have quadrature inputs. The VGA topology used in this work is shown in Fig. 5. The gain is controlled by the difference between the DC bias of the cascode transistors, ΔVg. Ignoring the resistors in the cascode emitters, the difference between the output currents I_1 and I_2, is given by,

$$I_1 - I_2 = I_o \tanh(\Delta V_{in})\tanh(\Delta V_g) \quad .(3).$$

Resistors are included in the cascode emitters (R_1= R_2= R_3=R_4=20Ω) to linearize the gain with respect to the control voltage. The gain control voltage is generated using an inverse tanh cell further linearizing the gain response (the measured gain response is shown in Fig. 5)

Since the dc current through the RF input transistors, Q_1 and Q_2, is kept constant, the input match and linearity do not change significantly with gain setting. This topology maintains constant input match (necessary for the baluns) while ensuring that noise of Q1 and Q2 has the same transfer function to the output as the signal. Therefore, as the output signal decreases with lower gain, the noise at

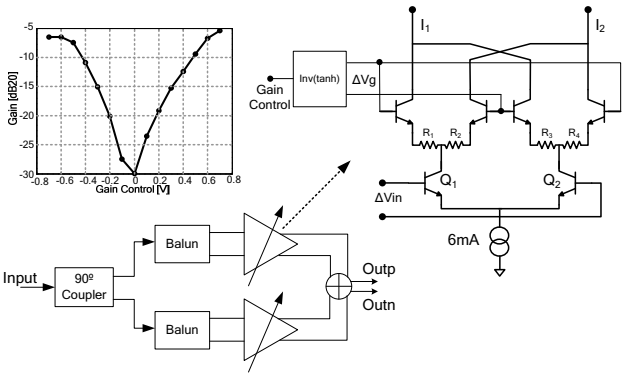


Fig 5. Vector interpolator schematic with measured gain variation.

the output decreases as well. In this design, the loss of the passives generating quadrature adds 2dB loss and hence 2dB to the noise figure.

V. Measurement Results

1) *Reflection-type phase shifter*:

The RTPS was measured using a 67GHz probe-based setup. The measured insertion loss and phase variation across control voltage at 57, 60 and 64GHz are shown in Fig. 6a. The RTPS achieves 180° phase variation across the band with <1dB loss variation across frequency, while the loss varies from 4.2dB to 7.5dB across phase settings. A phase-inverting variable gain amplifier (PIVGA) with 4dB variable gain would compensate for this gain variation while providing 180° phase shift. The maximum *rms*-phase error across the four IEEE channel bands between 57GHz and 65GHz is 2.7° (Fig. 6b)[7]. As the temperature is changed from 10C to 85C, the maximum variation in relative phase shift is 9° while the loss variation is < 0.7dB (Fig. 6c). Measurements across a wafer indicate that the *rms* error in relative phase shift is around 2.7° and *rms* amplitude error is 0.2dB (Fig. 6d and Fig. 6e). These measurements show that the RTPS is temperature insensitive and has good matching across the wafer, indicating that circuits such as the LNA or PA will dominate variations due to temperature and mismatch.

2) *Active Vector Interpolator*:

The interpolator was measured on-wafer using probes with one differential output terminated to 50Ω. The gain control voltages of the IVGA and the QVGA, V_{GI} and V_{GQ}, are the control signals fed to the interpolator (VGA gain vs control voltage is shown in Fig. 5). Fig. 7a plots the measured s-parameters for $\{V_{GI} = V_{GQ} = 0.8V\}$ which is the highest gain setting. In Fig. 7b, the real and imaginary part of S21 at 60GHz across gain settings is represented in the complex plane. It can be seen that the vector interpolator is able to provide 360° phase shift as well as large gain variation which can be useful for beam synthesis [8]. Fig. 7c plots the phase shift for 16 different settings across frequency. The maximum rms error across the four channel bands between 57GHz and 64GHz band is 3°. Measurements across temperature show that maximum relative error for temperature from 25C to 85C is 7°(Fig. 7d). The noise figure of the vector interpolator at 60GHz changes from 17.3dB at 25C to 18.1dB at 85C (Fig. 7e). The measured P1dB at 60GHz is -10dBm. The interpolator draws 12mA from 2.7V and the core occupies 0.64mm^2 of die area (Fig. 8).

Since the phase shifters in this design have analog control, a phase resolution cannot be assigned as it depends on resolution of the DACs that generate the voltages. However, from measurements, 11.25° phase resolution with a phase error <5° can be achieved in the RTPS using a 6-bit DAC while in the case of the active interpolator 11.25° phase resolution can be achieved with <5° phase error with 4-bit DACs generating V_{GI} and V_{GQ}. The I and Q control bits in the interpolator provide amplitude control as well.

Table 1 compares the performance of the vector interpolator, passive RTPS, and the cascade of passive RTPS with a 0/180 PIVGA (measured independently).

From a Rx perspective, the linearity and the NF of the two methods are comparable while the gain is lower in the RTPS+PIVGA case. However, the gain can be recovered with lower total power consumption by including gain stages in the signal combining network. Therefore, as long as the impact of lower frontend gain on Rx noise figure is acceptable, the cascade of passive RTPS and PIVGA leads to lower total power consumption. In cases, where mixer/combining network noise contributes significantly to array SNR, the active interpolator may be better suited.

In the case of the Tx, again the cascade of passive RTPS and PI leads to lower power consumption but also leads to active signal distribution stages in order to achieve desired linearity. The use of active interpolator would simplify the RF distribution network at the cost of increased power consumption in each frontend.

VI. Conclusion

In this paper, 60GHz low-loss reflection-type phase shifter and 60GHz active vector interpolator are demonstrated in silicon. The RTPS achieves desired 180° phase variation with loss varying from 4.2dB to 7.8dB while the active interpolator provides 360° phase variation across the 57GHz-64GHz band while providing >10dB gain control. The phase shifters were characterized across wafer and temperature and the suitability of the arrays for RF-path phase shifting phased array architectures was discussed.

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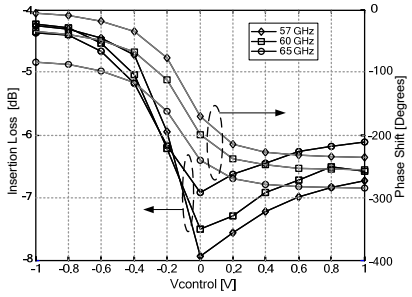

Fig. 6a. RTPS performance at 57GHz, 60GHz and 64GHz.

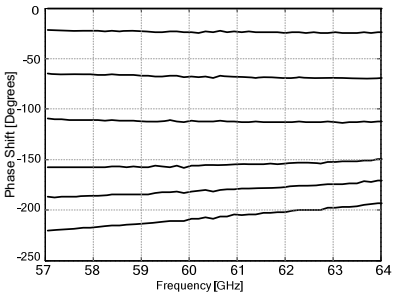

Fig. 6b. RTPS phase shift for different control voltages

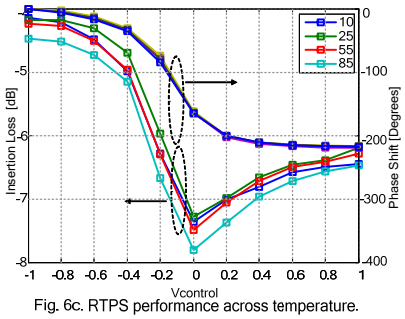

Fig. 6c. RTPS performance across temperature.

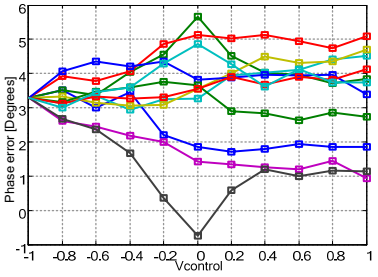

Fig. 6d. RTPS relative phase shift error across 11 samples.

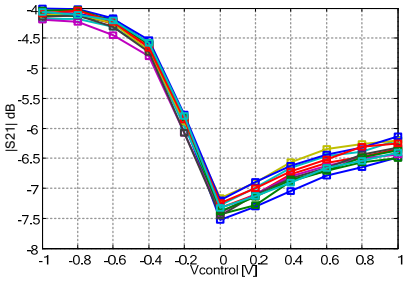

Fig. 6e. RTPS insertion loss across 11 samples

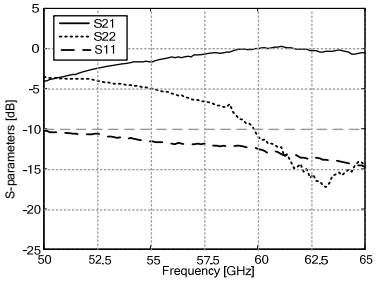

Fig. 7a. Active Vector Interpolator s-parameters at Gain Control, I = 0.8V , Gain Control, Q = 0.8V

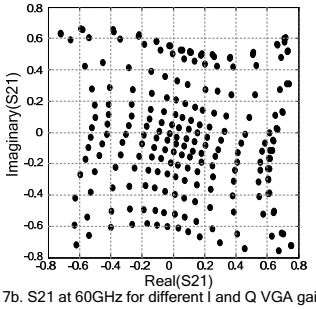

Fig. 7b. S21 at 60GHz for different I and Q VGA gain settings.

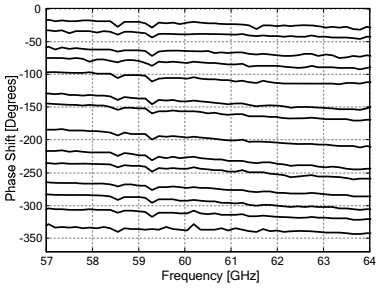

Fig. 7c. Vector Interpolator phase shift for different settings.

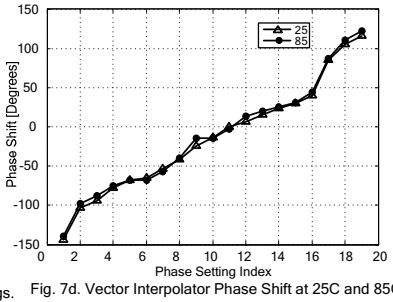

Fig. 7d. Vector Interpolator Phase Shift at 25C and 85C.

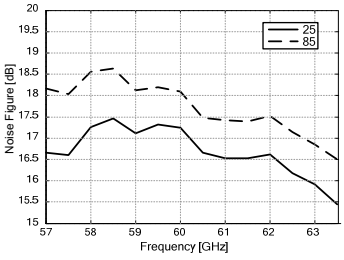

Fig. 7e. Vector Interpolator Noise Figure at 25C and 85C.

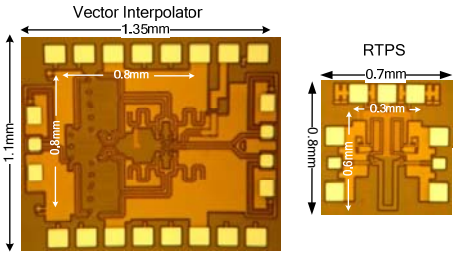

Fig. 8. Die Photograph of RTPS and Vector Interpolator.

Table 1.
RTPS and Vector Interpolator Performance Summary

Topology	RTPS	RTPS+PIVGA*	Vector Interpolator
Current	0 mA	6 mA	12 mA
Phase range	>180º	360º	360º
Gain	~ -7 dB	-5.5dB	~ -2 dB
iP1dB	-	-3 dBm	-7 dBm
oP1dB	-	-8 dBm	-8 dBm
NF	~ 7 dB	~ 16 dB	~ 17 dB
Bandwidth	>7GHz	>7GHz	>7GHz