31.2 A Fully Integrated MIMO Multi-Band Direct-Conversion CMOS Transceiver for WLAN Applications (802.11n)

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The IEEE 802.11a and g WLAN protocols provide data rates up to 54Mb/s using a 20MHz channel bandwidth in the 2.4 and 5GHz ISM and UNII bands, respectively. The rapid adoption of these systems in the past few years, which is partly due toadvancements in transceiver design and integration [1], has led to growing demands for more robust wireless links with higher data rates. These demands can be met by the adoption of multi-input multi-output (MIMO) techniques, the use of wider-band channels, utilization of higher-order constellations, and/or the use of lower coding rates for the modulation. The emerging 802.11n standard will use some or all of these techniques to provide a robust and high data rate wireless link. Such a standard would therefore need to utilize a high performance transceiver. In order to keep the cost down, the transceiver would need to be highly integrated and preferably implemented in CMOS technology.

In this paper, a single-chip fully integrated multi-band direct-conversion CMOS MIMO transceiver targeted for WLAN applications is presented. This transceiver is capable of satisfying the requirements of the Enhanced Wireless Consortium (EWC) as it stands today. The transceiver presented here is implemented in a 2×2 format. The RX and TX blocks are fed by a shared PLL through the LO generation and distribution circuitry. As compared to the previously published MIMO transceivers for WLAN, this transceiver is implemented in a low-cost 0.18μm CMOS technology, covers both the G band as well as the entire worldwide A band, is smaller in area, is capable of operating over RF channel bandwidths of 10, 20, or 40MHz, and achieves lower NF, phase noise, and EVM. Furthermore, transceiver performance under various EWC modulation and coding schemes (MCSs) are presented and PHY rates of >270Mb/s are shown.

A block diagram of each one of the receiver slices is shown in Fig. 31.2.1a. The 5GHz or 2GHz signal is received and amplified by the appropriate differential LNA, then directly downconverted by the quadrature mixers associated with that band. The downconverted signal is then applied to the first high-pass VGA (HPVGA1) where the signal is amplified and the DC offsets associated with the self mixing of the mixers and device mismatches are rejected. The signal is then filtered by 4th-order Butterworth filters to reject interferers and is then further amplified by HPVGA2 and HPVGA3, each with their own DC offset cancellation loops. The resultant I and Q outputs are then buffered and sent to I and Q ADCs on the companion PHY+MAC chip. Each one of the HPVGAs has a programmable gain of 0 to 30dB in 3dB steps. The corner frequency of the each HPF in the HPVGAs is calibrated using an on-chip RC calibration loop. Further, the HPF corners are programmable over a wide range to satisfy the integrity of the lower index OFDM subcarriers during the payload while allowing for fast settling during the preamble. The corner frequency of the LPF is also calibrated to the desired bandwidth (5MHz, 10MHz, or 20MHz) to ensure proper system operation in the presence of large adjacent-channel interferers. Two wideband RSSI signals as well as one narrowband RSSI signal ensure the proper operation of the system over a wide dynamic range and in the presence of large (CCK, OFDM, Bluetooth, etc.) interferers.

Figure 31.2.1b displays the block diagram of each one of the transmitter slices. Received quadrature signals from the DACs are applied to the programmable bandwidth and gain low-pass filters. The outputs of the LPFs are then applied to the appropriate upconversion quadrature mixers which directly convert the baseband signal to the desired RF band. The upconversion mixers (with associated transconductors) are designed for high linearity and low LO feedthrough over a wide gain-control range [2]. The RF signal is then amplified through 2 stages of programmable gain. The final gain stage is capable of driving a 50Ω load through a balun and is internally matched to 100Ω differential. The RF gain stages are designed such that they consume less power at lower gain settings. Figure 31.2.2 shows the simplified schematic of the PA driver. A 3-stage transconductance linearization is used to improve the linearity of the driver over wide range of inputs [1].

A shared integer-N PLL is used to synthesize the proper LO. The on-chip crystal oscillator whose divided output provides the reference to the PFD is capable of operating with a 20MHz, 40MHz, or 80MHz crystal. In order to minimize the impact of the VCO noise, The PFD comparison frequency is chosen to be as high as possible to allow wide PLL loop bandwidth. Further, in order to minimize the phase noise arising from the loop filter and charge pump, a low programmable K_{VCO} and high charge pump current are used. The PLL utilizes a single VCO with a wide tuning range to cover both 802.11 frequency bands. A 9b VCO calibration is implemented to choose the best VCO sub-band for the desired channel.

In order to avoid any pulling effects by any of the transmitters on the VCO, the VCO operates at 2/3 of the channel frequency for the 802.11a band and at 3/4 of the channel frequency for the 802.11b/g bands (Fig. 31.2.3).

The full 2×2 MIMO transceiver is composed of two multi-band RX chains (Fig 31.2.1a), two multi-band TX chains (Fig. 31.2.1b), a PLL and LO generation and distribution section (Fig. 31.2.3), various calibration blocks, digital control section, and some other miscellaneous circuits. In order to ensure optimal performance, the chip design, chip floor planning, package design, and many aspects of the board design are conducted simultaneously.

The transceiver uses many self-contained and/or DSP-assisted auto-calibration circuitry. These calibrations include independent and multi-phase LO feedthrough calibration (RF coupling and DC offsets) on each TX core, independent quadrature calibration on each RX and TX core, resistor calibration for bias current generation blocks, LPF and HPF corner calibration on filters, multi-phase VCO gain calibration and TX power calibration. Additionally, a high-accuracy temperature sensor allows for temperature-based calibrations, if necessary. These calibrations ensure optimal operation over PVT as well as a high-yield part.

The phase noise of the PLL for the 5.240GHz A bands is shown in Fig. 31.2.4a. The phase noise plot is obtained with the PLL and XO voltage supply being provided by the integrated ultra-low-noise regulators, and with a 20MHz crystal used as the reference. As shown in the EVM versus sub-carrier plot of Fig. 31.2.4b, operating in legacy 802.11g mode, each TX achieves an EVM of –41dB while transmitting at –2dBm. Each TX achieves an EVM of –40dBm at –5dBm TX power. Chip referred sensitivity level of –78dBm (at each antenna) is achieved in MRC mode. Under similar conditions the sensitivity for an 802.11a signal at 5.24GHz is –79dBm. In EWC MCS 15, 40MHz mode, AWGN channel, with standard GI (270Mb/s PHY rate), a sensitivity of –72dBm and a Chariot effective throughput of 200Mb/s is achieved (Fig. 31.2.5).

The chip micrograph is shown in Fig. 31.2.6. Typical IC performance data is shown in Figure 31.2.7. The chip is designed such that it can be used, in a multi-IC configuration, to build a larger MIMO system (e.g., 4×4).

Acknowledgment:
The authors would like to acknowledge and thank the contributions by the layout, WLAN System, Digital, Software, Board, RF, Test, CAD, and Operations Groups at Broadcom.

References:
[1] A. Behzad, et al., "A 5-GHz Direct-Conversion CMOS Transceiver Utilizing Automatic Frequency Control for the IEEE 802.11a Wireless LAN Standard," *J. Solid-State Circuits,* vol. 38, pp. 2209-2220, Dec., 2003.
[2] C. P. Lee, et. al., "A Highly Linear Direct-Conversion Transmit Mixer Transconductance Stage with Local Oscillation Feedthrough and I/Q Imbalance Cancellation Scheme," *ISSCC Dig. Tech. Papers,* pp. 368-369, Feb., 2006.

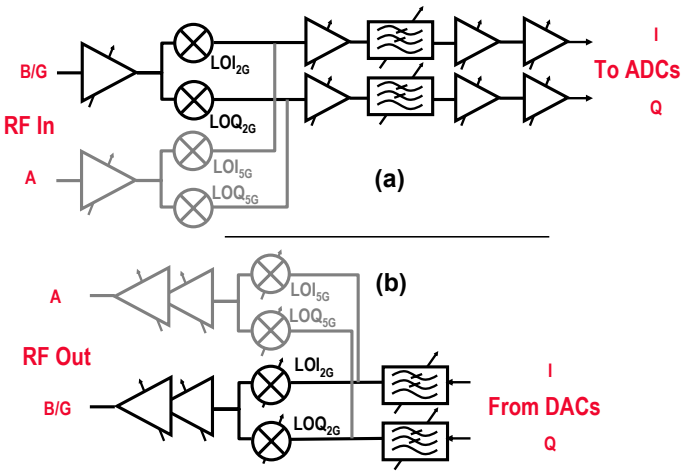

Figure 31.2.1 (a) Block diagram of each receive slice and (b) block diagram of each transmit slice.

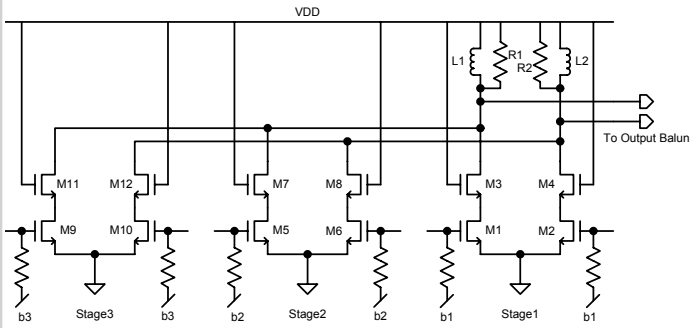

Figure 31.2.2 A-band PA driver transconductance linearization.

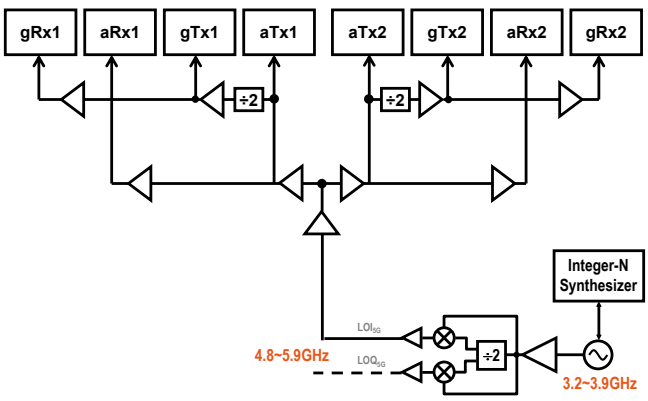

Figure 31.2.3 LO generation and distribution (Q path not shown).

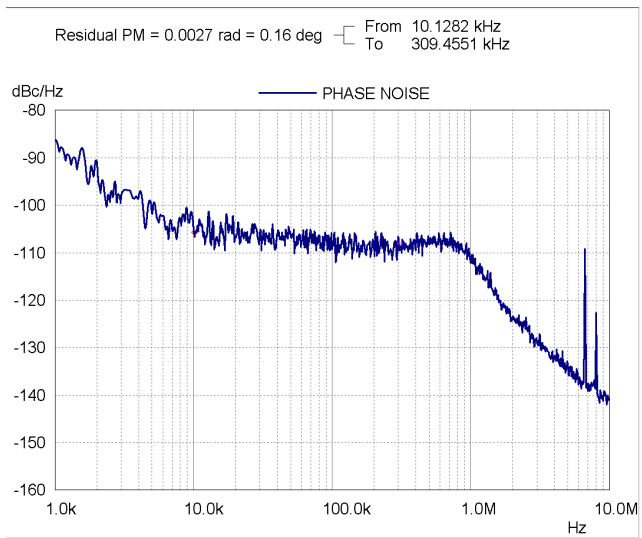

Figure 31.2.4a Measured phase noise at transmitter output (5.24GHz).

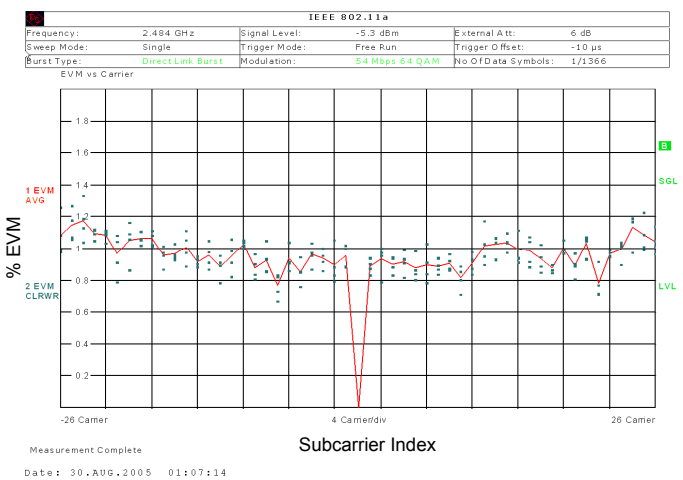

Figure 31.2.4b Measured TX EVM (Po=-2dBm; -41dB @ 2.484GHz).

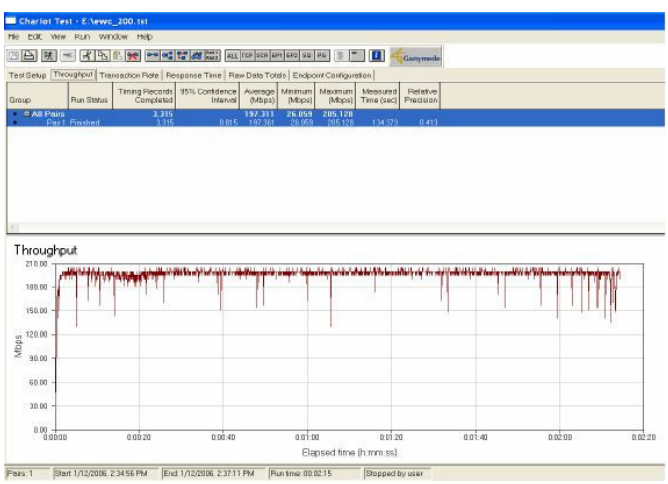

Figure 31.2.5 Chariot results with average throughput of > 200Mb/s.

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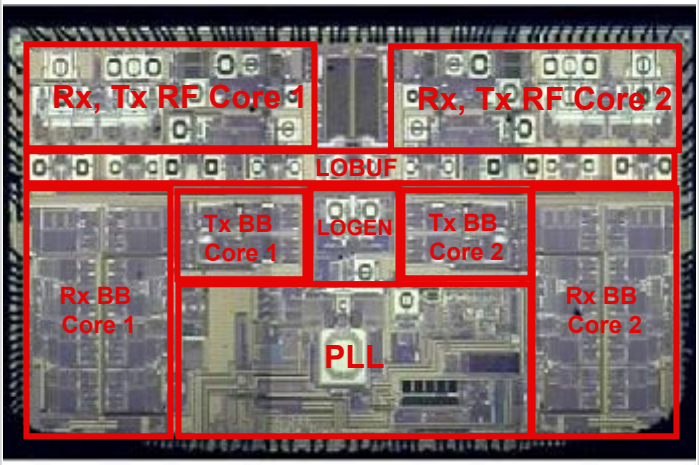

Figure 31.2.6 Die micrograph of the dual-band MIMO transceiver.

	Measured	Requirement	
Frequency band (A/G)	2.4-2.5 / 4.8-5.9		GHz
RX max gain (A/G)	>100 / >100		dB
RX min gain (A/G)	5 / 5		dB
RX NF @ max RF gain (A/G)	4 / 4.5		dB
RX IIP3 @ min RF gain (A/G)	+5 / +6		dBm
RX IIP3 @ max RF gain (A/G)	-12 /-10		dBm
RX-RX Isolation (A/G)	>60 / >60	>30	dB
RX LPF BW	5 / 10 / 20		MHz
TX P-1dB (A/G)	+14 / +16		dBm
TX EVM (A/G)	<-40 / <-41	<-30	dB
TX-TX Isolation (A/G)	>35 / >43	>15	dB
In-band PN @ 150kHz offset (A/G)	-108 / <-109	<-100	dBc/Hz
Legacy 54Mbps, chip-referred MRC enabled sensitivity (A/G)	-79 / -78	-65	dBm
EWC MCS15 40MHz channel, std GI, 270Mb/s, chip-referred sensitivity	-72 / -72		dBm
Vdd	1.8		V
RX mode total current consumption (both cores active)	275		mA
TX mode total current consumption (both cores active)	280		mA
Technology	0.18μm CMOS		
Die size	18		mm2
ESD HBM performance	> ±2		kV

Figure 31.2.7 MIMO transceiver performance summary.

