Optimisation of 100V High Side LDMOS Using Multiple Simulation Techniques

M. Elwin*, P. Holland*, I. Anteney [#], J. Ellis[#], L. Armstrong[+], G. Birchby[+] and P. Igic*

*School of Engineering, Swansea University, Singleton Park, Swansea SA2 8PP, United Kingdom
[#]X-Fab, Tamerton Road, Roborough, Plymouth PL6 7BQ, United Kingdom
[+]Diodes – ZETEX, Chadderton, Oldham OL9 9LL, United Kingdom

Abstract - **A combination of conventional cross sectional process and device simulations combined with top down and 3D device simulations have been used to design and optimise the integration of a 100V Lateral DMOS (LDMOS) device for high side bridge applications. This combined simulation approach can streamline the device design process and gain important information about end effects which are lost from 2D cross sectional simulations. Design solutions to negate detrimental end effects are proposed and optimised by top down and 3D simulations and subsequently proven on tested silicon.**

I. INTRODUCTION

There has been an increasing trend towards adding intelligence to power switching such that power management techniques are made as efficient as possible. This trend can only increase as legislation to control the efficiency of the electronic products and consequently the emission of greenhouse gases is being implemented on a world-wide basis. The best solution for incorporating intelligence into small to medium voltage applications is to use bulk silicon Power IC technologies. Here the analogue or digital control electronics and the power transistors are integrated onto the same chip.

One of the most common power switches used for Power IC technologies is the Lateral Double Diffused Metal Oxide Semiconductor (LDMOS) power transistor. The LDMOS provides many benefits over other power transistor solutions such as ease of control, packing density, unipolar operation, compatibility with foundry design libraries etc. that all lead to cost reductions in design and manufacturing. However, the integration of LDMOS transistor technology with conventional CMOS circuitry presents some manufacturing processing and architecture challenge that must be overcome to ensure correct operation and high manufacturing yields.

LDMOS design optimisation using RESURF [1]-[2] and Super Junction [3]-[4] techniques is well documented. These methods are highly utilized to improve the figure of merit (i.e.

maximize specific on-resistance, Rs, for desired breakdown voltage) of LDMOS devices. Simulation is an essential tool in the optimisation of these devices, and two dimensional cross sectional analysis is a base requirement for effective design. However, termination and end effects are often lost in these two dimensional views. Racetrack type designs can be used to eliminate end effects, and are usually employed for high voltage devices, but this method can present new problems with high voltage cross over and radius of curvature effects which often result in increased device dimensions or more complex designs. High-side devices add another design challenge due to the requirement to isolate the source and body regions from the substrate. Figure 1 shows typical low side and high side n-channel LDMOS devices, with the high side source and p-well isolated from the substrate by a deep n-well.
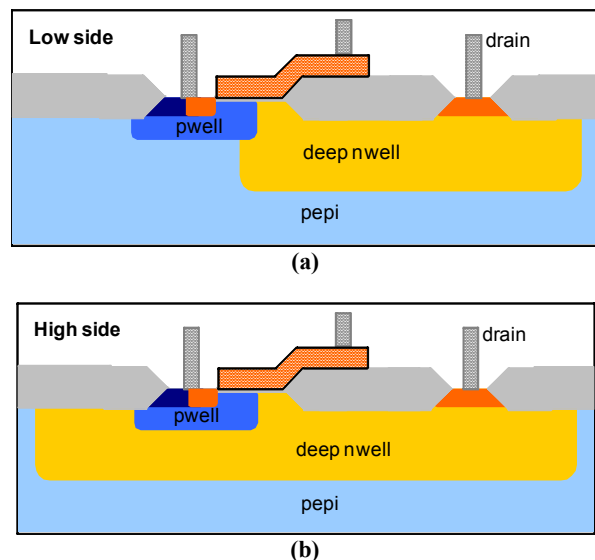

(a)

(b)

Figure 1. N-channel LDMOS (a) Low side topology, and (b) High side topology.

II. 2D SIMULATIONS

The 2D cross sectional simulations of the high side device breakdown, for low side (drain voltage ramped with gate, source and substrate grounded) & high side (drain, gate and source ramped with substrate grounded) bias conditions, are shown in Figure 2. The deep n-well doping has been optimised to achieve minimal $R_{DS\ (ON)}$ for 120V breakdown,
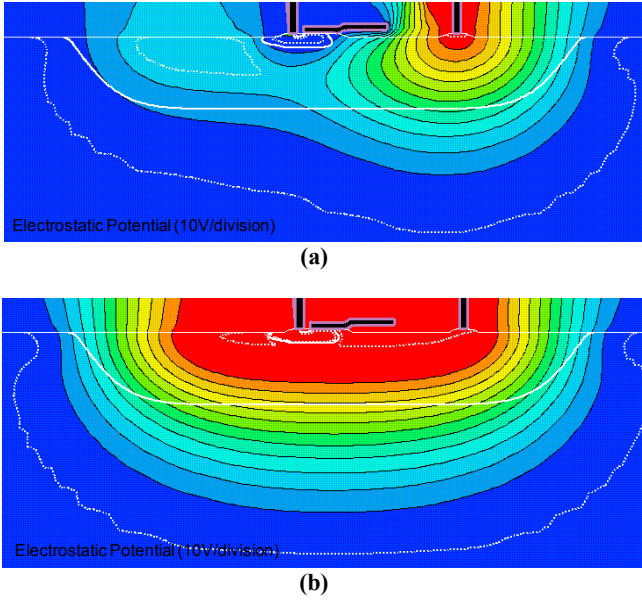
(a)

(b)

Figure 2. High side n-channel LDMOS (a) showing potential lines at breakdown with; (a) gate, source and substrate ground, and drain voltage ramped; (b) substrate grounded and gate, source, drain voltage ramped.

but the real device will not reach this breakdown voltage due to the end effects of the large deep n-well required for high side operation, i.e. the physical result is very different from the one predicted by 2D cross sectional simulation alone. Additional 2D device simulations, as viewed from the top down perspective, have been used to observe and investigate the end effects that can significantly degrade the performance
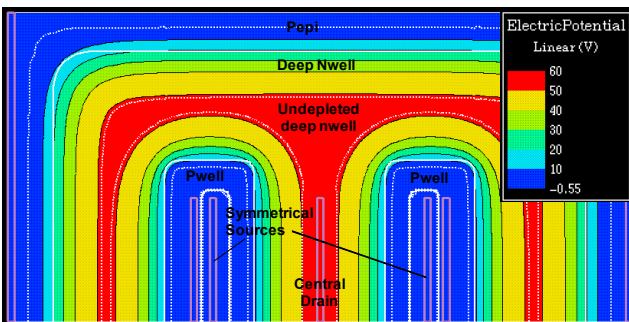
Figure 3. Top down device simulation showing the potential lines at breakdown at the end of the symmetrical high side device shown in figure 1(b), and simulated in cross section in figure 2.
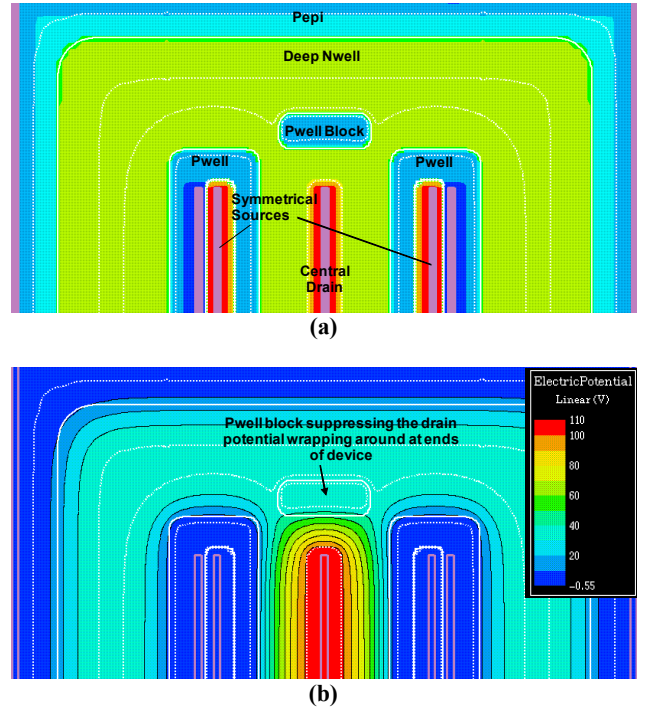
(a)

(b)

Figure 4. Top down view at the end of the symmetrical high side device with an additional p-well 'block' at the drain end showing: (a) the net doping profile and electrodes; (b) the electrostatic potential at breakdown.

of real devices. Figure 3 shows that, with the high side device, the drain potential wraps around to the source via the undepleted deep n-well at the ends of the device, pinning the actual breakdown voltage to less than 50V.

III. DEVICE OPTIMISATION

Design solutions to prevent the drain potential wrap around are proposed using top down and 3D simulations. Figure 4 shows a top down simulation of the same device shown in Figure 3 with the addition of a p-well block at the end of the drain. Top down device simulations have the advantage of providing a quick feedback of potential fixes to the end effects. 3D simulations can then be used to confirm and further optimise the design before committing to silicon. Additionally, 3D simulations can simulate the entire structure, as it is not possible to simulate the gate poly electronically in the top down approach.

Figure 5 shows a 3D simulation using extended poly overlap to suppress the drain potential wrap around. Both these techniques have been tested on silicon to produce an optimised 120V high-side LDMOS device with $R_{DS\ (ON)} = 190m\Omega mm^2$ integrated into an existing 0.35um 60V CMOS process without any additional masks or process steps. The measured output characteristics of the optimised design are shown in Figure 6.
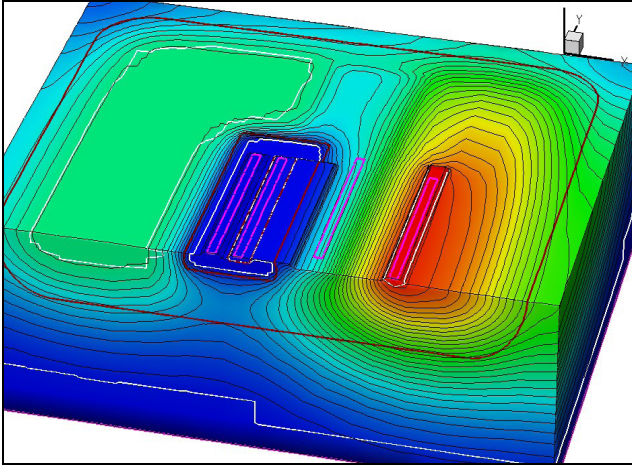
Figure 5. 3D simulation of device from figure 2 with end poly extension (poly removed from picture to show potential in silicon) to suppress the drain voltage wrapping around to the source.
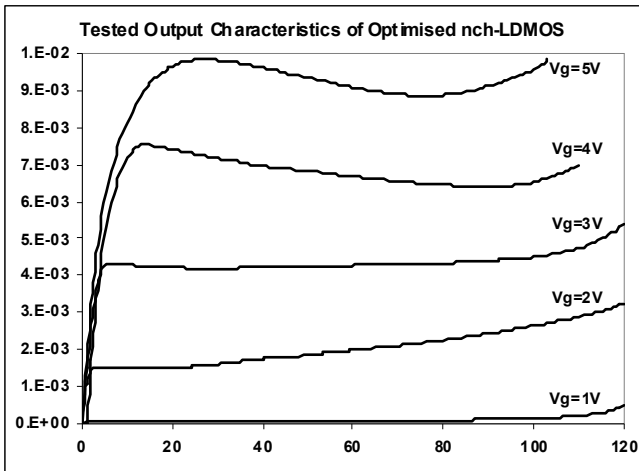

Figure 6. Output characteristics of the optimised device.

The PWM/H-bridge circuit incorporating four power LDMOSFETs has been designed to evaluate this technology. The layout of the circuit is shown in Figure 7. The four power devices are quite visible; however the same types, but obviously smaller area, LDMOSFETs have been used for level shifting. These are the areas of mirrored layout in the lower right and lower left beneath the large power devices. Across the bottom of the chip one can see the Hall-Amp, PWM and commutation control circuitry.
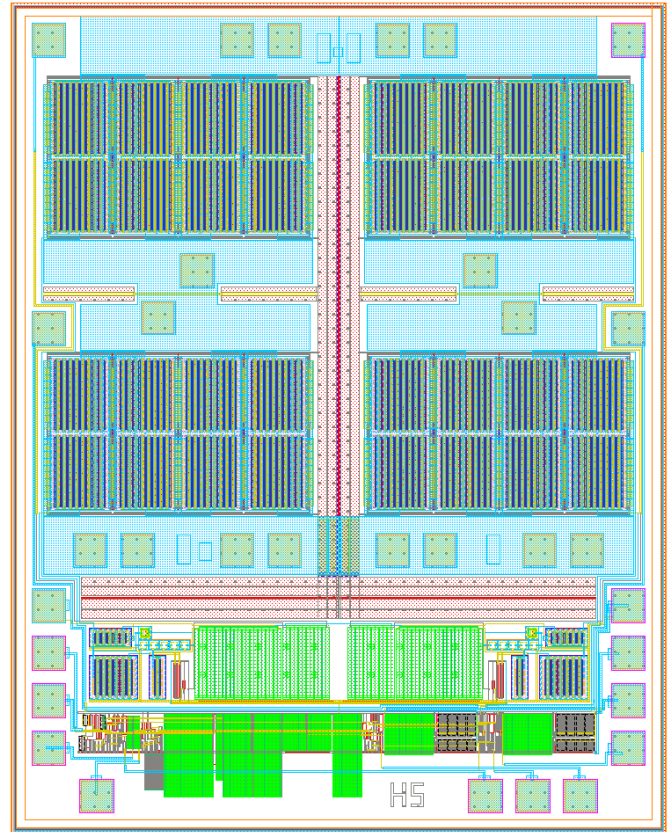

Figure 7. The PWM/H-bridge circuit incorporating four power devices, level shifters, and control circuitry.

IV. SUMMARY

A combination of conventional cross sectional process and device simulation technique combined with top down and 3D device simulations have been used to design and optimise the integration of a 100V Lateral DMOS (LDMOS) device into the standard 0.35 microns CMOS technology. The Synopsis TCAD simulation suit has been employed to achieve this task. As proven on manufactured and tested silicon, this combined simulation approach can streamline the device design process and gain important information about end effects which are lost from 2D cross sectional simulations. Design solutions to negate detrimental end effects have been proposed and optimized.

REFERENCES

[1] T. R. Efland, Integration of Power Devices in Advanced Mixed Signal Analog BiCMOS Technology, *Proc. 13th International Symposium on Power Semiconductor Devices* (ISPSD 2000) 39-44

[2] C.K. Jeon, J.J. Kim, Y.S. Choi, M.H. Kim, S.L. Kim. H.S. Kang and C.S. Song, Analysis of LDMOS Structure With Inclined P-Bottom Region, *International Symposium on Power Semiconductor Devices* (ISPSD 2002) 293-296

[3] F. Udrea, A. Popescu, R. Ng and G.A.J. Amaratunga, Minority carrier injection across the 3D RESURF junction, *International Symposium on Power Semiconductor Devices* (ISPSD 2000) 201-204

[4] S. G. Nassif-Khalil, L. Z. Hou and C. A. T. Salama, SJ / RESURF LDMOST, *IEEE Transactions on Electron Devices* 51 (2004) 1185-1191