Considering Fabrication in Sustainable Computing

Alex K. Jones[1], Yiran Chen[1], William O. Collinge[2], Haifeng Xu[1], Laura A. Schaefer[3], Amy E. Landis[4], and Melissa M. Bilec[2]

[1]Electrical and Computer Engineering, University of Pittsburgh
[2]Civil and Environmental Engineering, University of Pittsburgh
[3]Mechanical Engineering and Material Science, University of Pittsburgh
[4]School of Sustainable Engineering and the Built Environment, Arizona State University

***Abstract*—The term *green* computing has become effectively synonymous with low-power/energy computing. However, for computing to be truly sustainable, all phases of the system life-cycle must be considered. In contrast to the considerable effort that has been applied to address the use-phase energy consumption issue—ranging from battery powered embedded systems to data center servers—there is limited awareness or attention to the considerable energy consumption and environmental impacts from semiconductor fabrication. Current research indicates that fabrication is responsible for a significant factor of the energy utilized by these systems throughout their life-cycle. The trends of technology scaling coupled with developing hybrid fabrication solutions for integration of emerging technologies, while beneficial for use-phase power consumption, exacerbate these increasing environmental impacts from fabrication. *Thus, design for sustainability is a grand challenge that must be addressed over the next decade*.**

I. Introduction

The concept of green computing has become highly correlated to energy consumption of computational devices and their supporting electronics as well as secondary energy consumers (such as climate control) during their *use phase* (i.e., after they are deployed into service). However, there are *other important environmental concerns* about computing that must be taken into account to fully consider the problem of sustainable or green computing. This includes the *environmental impacts of manufacturing computers* and their supporting electronics both from a materials and energy perspective, as well as similar concerns with disposal and recycling of these devices after their term of service is completed. Thus, to effectively consider the entire environmental impact of computing deployments from manufacturing to disposal it is necessary to consider all impacts throughout the life-cycle, which includes, but is not limited to the impacts while in service. For example, in a 2009 study by Gartner, emerging countries must dispose of 30 million computers annually without appropriate mechanisms for environmentally responsible disposal or recycling [1].

In this paper, we discuss some *alarming environmental trends* in the manufacturing phase of computing systems with particular emphasis on integrated circuits (ICs), evaluated using life-cycle assessment (LCA). LCA is a state-of-the-art methodology for determining the environmental impacts of a product or process from a life cycle or "cradle to grave" perspective. A popular application of LCAs is to assess the environmental performance of buildings [2], [3]. Somewhat more recently, LCA has also been successfully applied to manufacturing of computer components [4] including ICs [5]–[8], Liquid Crystal Display (LCD) monitors [9], [10], and full computer systems [10]–[12].

These LCA studies demonstrate that the manufacturing effort has become comparable to the use-phase energy effort of systems. Further, as the technology node size decreases, the trends indicate an increase in fabrication effort per die area as well as an increase in die area. When considered together, these trends indicate a significant challenge to be addressed. Moreover, 3D integration of CMOS and emerging technologies will exacerbate these trends. While these effects have been considered in terms of fabrication cost, they have not been studied in detail for their environmental impacts. To say nothing of the environmental and health concerns for the battery of chemicals employed and waste water generated to build semiconductors the *environmental impacts of semiconductor fabrication*, including the energy consumed and greenhouse gases generated, is a *grand challenge* that must be addressed over the next decade.

The remainder of the paper is organized as follows: Section II provides background on LCA for semiconductor systems and includes a detailed hybrid and EIO- LCA of modern computer systems. Section III provides a discussion of fabrication environmental impact trends including consideration of emerging technologies. Finally, conclusions are related in Section IV.

II. Background and Previous Work

To analyze the environmental impacts of computing technology it is necessary to determine a quantitative relationship between these electronic devices and the environmental impacts they produce. LCA is a powerful and widely used tool for measuring the sustainability of an enterprise or concept and informing decisions with respect to sustainability and environmental considerations. LCA quantifies the environmental impacts of a product or process and can be a helpful tool in identifying the most benign technologies among an array of options. Through use of LCA, it is possible to observe which stages cause the most impact and offer suggestions to minimize impacts throughout a product's life.

LCA alone typically refers to *process* LCA, where the entire cradle to grave analysis of the item or system is conducted to determine the full environmental impact [13]. Another method called *Environmental Input-Output (EIO)* LCA uses the relationship between cost of the process and

This work is supported, in part, by NSF award EFRI-1038139.

978-1-4799-1071-7/13/$31.00 ©2013 IEEE

the environmental impact [14]. EIO-LCA is based on the Economic I-O analysis developed by Wassily Leontief in the 1930s [15]. Leontief developed an interdependency model that quantifies proportional interrelationships among economic sectors in an economy. Finally, *hybrid* LCA combines process LCA when possible with EIO-LCA [16]. This provides a compromise between the accuracy of process LCA and the unavailability of all detailed or proprietary information which is not required for EIO-LCA.

A. Previous Work

LCA is most often applied to material considerations in the design of buildings. Environmental impacts of buildings are typically dominated by the impact of operation of the building (e.g. energy usage, emissions, etc.) rather than impacts from manufacturing, construction, and destruction [2], [3]. In contrast to a building lifetime measured in decades (or centuries), computing equipment has a much shorter lifetime measured in years (and in some cases months) rather than decades. Additionally, the environmental impacts may be much higher for computers due to the specialized nature of the raw materials utilized and the manufacturing conditions and processes required to build components and in particular semiconductor devices.

The environmental impacts of buildings, which are heavily outweighed by use-phase impacts, are still a source of considerable optimization effort. Therefore, at a minimum, environmental impacts from manufacturing of computer systems, which is likely to be a much higher percentage of the life-cycle impacts, should be considered and not ignored.

The fabrication process for semiconductor devices is fairly well understood conceptually and an overview can be found in various places including [17]. Researchers have conducted LCAs of the production of particular ICs [5], [6]. Often, process LCA of a diverse set of ICs is not possible because the details of manufacturing process, from the design of the IC hardware to the implementation technology, are withheld by the chip designer and/or foundry in order to protect their intellectual property.

The environmental impacts of different semiconductor-based devices varies considerably even for devices with similar sizes and shapes that follow a similar manufacturing process. This difference is due to the difference in fabrication processes, which can be difficult to capture in an LCA without detailed and proprietary data.

Consider two "similar" ICs from a size, shape, and manufacturing perspective, an E-PROM and DRAM [5], [6] shown in Table I. From the table it is clear that during fabrication the normalized energy consumption is not the same between the two ICs. In this case, the DRAM consumes about five times more manufacturing energy than the E-PROM.

TABLE I: LCA Comparison [5], [6].

	Total		Normalized	
Phase	**E-PROM**	**DRAM**	**E-PROM**	**DRAM**
Fabrication, Test	2.4 MJ	27.0 MJ	3.0 MJ/cm^2	22.5 MJ/cm^2
Package/Assembly	10.1 MJ	5.8 MJ	1.9 MJ/cm^2	2.2 MJ/cm^2
Total	12.5 MJ	32.8 MJ	4.9 MJ/cm^2	24.7 MJ/cm^2

Thus, Krishnan *et al.* used the hybrid LCA method [7] to study the environmental impact of 130nm CMOS technology fabrication directly, based on ICs constructed from a 300mm wafer. Krishnan used process LCA for the fabrication process, which at 130nm is well understood, and used EIO-LCA for the less clearly defined upstream elements. Based on the work of Krishnan, Boyd *et al.* studied the life-cycle energy demand and greenhouse gas (GHG) emission of computational ICs fabricated using different fabrication technologies ranging from 350nm to 45nm [8], which spans an approximately 15-year period of semiconductor fabrication development. Thus, they demonstrated the trends of environmental impact of the semiconductor industry during this time.

Based on the assumption that the effort and environmental impact to construct computer systems is dominated by the fabrication of the ICs contained within that computer, Intel conducted a study, which in part determined the total IC area of different generation computer systems [18]. Additionally, two other available studies examine the LCA of full computer systems [10], [11]. One additional required computer component that is often segregated from the computer system is the display. There have been several LCAs conducted of liquid-crystal displays (LCDs) [9], [10].

When a holistic view of many systems is considered, including additional impacts beyond ICs, including PCBs and displays these impacts can be staggering. In our previous work we compared the manufacturing effort for computing systems against the manufacturing effort of building construction [4]. In this work we demonstrate that the use phase may not dominate the fabrication phase to the same degree as is commonly assumed in sustainable computing research or as is true for other LCA categories such as building components. This underscores the difference in life-cycle thinking required for computer systems.

B. Hybrid LCA of Computer Systems

In this section we use a hybrid LCA of computer systems, using semiconductor LCA data published in the literature to examine two computer generations: circa 2001 and circa 2010. This LCA approach is based on a hybrid LCA for the manufacturing process of ICs and printed circuit boards (PCBs) and determines impact based on the areas these items consume in a system. These numbers are benchmarked against existing full system LCAs of computers.

In a recent study by Intel, the die area of all the ICs and PCB area of all PCBs in the system were determined using X-rays. Hybrid LCA results for PCB manufacturing energy were reported [18] and the trends are summarized in Table II. As expected the IC is the dominant component of the manufacturing energy in relation to the PCB. The reported global warming potential (GWP) is much closer between the two components (e.g. nearly identical in 2001). GWP is presented as CO_2 equivalent (CO_2e), which is the typical measure used in the field.

1) Full System EIO-LCA: As indicated in the literature, IC and PCB fabrication have the dominant environmental impacts of the entire computer system [18]. To put that perception into perspective, we conducted a study with EIO LCA, which contains data categorized into a computer/electronics sector and a category specifically for the semiconductor sector.

TABLE II: Area, Production Effort (Energy), and GWP of ICs and PCBs in two generations of computer systems [8], [18].

Year	2001		2010	
Technology	**IC**	**PCB**	**IC**	**PCB**
Area (cm^2)	7.5	500	12	700
Energy/cm^2 (MJ)	55.7	$2.37 \cdot 10^{-2}$	79.6	$2.37 \cdot 10^{-2}$
Energy (MJ)	417.9	11.9	955.7	16.6
Total Energy (MJ)	429.8		972.3	
GWP/cm^2 (kg CO_2e)	3.57	0.044	5.41	0.044
GWP (kg CO_2e)	27	22	65	31
Total GWP (kg CO_2e)	58		96	

Breaking down a typical computer system approximately 75% of the cost of a machine is dictated by semiconductor components and the remainder is from computer/electronics components as dictated by EIO-LCA categorization [4]. This supports the assertion that the IC components tend to dominate the environmental impact. This breakdown resulted in 6250 MJ of energy and 487 kg CO_2e of GWP for a typical system. The energy number is similar to 6400 MJ reported by Williams [11]. In a third hybrid LCA published by European Commission in 2005 the energy and GWP of 2627 MJ and 166 kg CO_2e, respectively for a computer [10] were also within this range. A study by Fujitsu in 2011[1] on its Esprimo E9900 desktop (which only reported GWP) reported 305 kg CO_2e for manufacturing [12], which also matches this range. For comparisons with use-phase impacts we can use the data from Table II as a lower bound and the EIO-LCA numbers as an upper bound of the system manufacturing impact.

2) LCD Monitors: A significant component of a computer system's environmental impact is the LCD monitor. Two groups completed hybrid LCAs of the construction of a 17" LCD monitor. In 2001 energy and GWP were reported as 2352 MJ and 910 kg CO_2e [9] and in 2005 these numbers were 1177 and 70, respectively [10]. These studies may contain different LCA system boundaries due to different intended audiences (e.g. academic audience [9] versus governmental report [10]) leading to the reported discrepancy. However, this discrepancy may be in part due to improvement in manufacturing processes. In 2001, LCDs were still relatively new and their manufacturing had significant opportunity for optimization. By 2005 LCDs were more widely adopted, were more efficient to manufacture, and their cost had dropped significantly. Thus, we utilize both numbers as lower- and upper-bounds. Finally, conclusions for full system environmental impact are summarized in Table III.

TABLE III: Life cycle energy and global warming potential of full computer systems.

	Lower bound		**Upper bound**	
	Energy (MJ)	GWP (kg CO_2e)	Energy (MJ)	GWP (kg CO_2e)
Computer	972	96	6250	487
Monitor	1177	70	2352	910
Total System	2149	166	8602	1397

C. Manufacturing versus Use Phase Analysis

Different studies to estimate the energy and GWP impacts required to operate a computer system are shown in Table IV. Energy numbers are estimated from machines in 2004 [11], 2005 [10], and 2010 [18].

TABLE IV: Use phase analysis of computer systems (one year period). Energy is in MJ and GWP is in kg CO_2e.

Component	**Intel (2010) [18]**	**EuP (2005) [10]**	**Williams (2004) [11]**
Computer	1051^{+}	699	500^{*}
Monitor	311^{*}	359^{+}	–
Total	1362	1058	–
	Lower Bound*		**Upper Bound+**
Total	811		1410

* Number used to calculate the lower bound.
+ Number used to calculate the upper bound.

We compare several manufacturing scenarios with the lower and upper bound values from Table IV and show these results in Fig. 1. All scenarios include the computer system and monitor (C+M), and each of four manufacturing scenarios are clustered into lower bound (LB) and upper bound (UB) use scenarios. We also consider 3-year and 5-year replacement cycles common in computer equipment. Each bar shows percentage of impact due to manufacturing (MF) on the bottom and use on top. The results indicate that either manufacturing or use could dominate centering around a nearly 50% split between the factors. These results are supported by the breakdown reported on the E9900 reporting 305 kg CO_2e for manufacturing and 373 kg CO_2e for the use phase over a five year period (45% manufacturing to 55% use-phase GWP). Given the efforts to reduce use-phase energy consumption of computing equipment, we will soon be left with a dominant impact from manufacturing. *Considering Amdahl's Law, it is time to invest in sustainable manufacturing for computing equipment.*

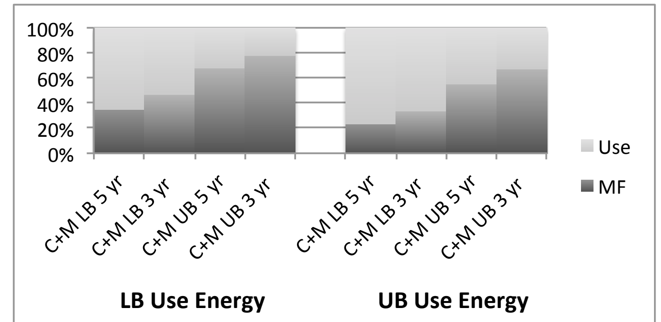

Fig. 1: Impact of computer system manufacturing versus use.

III. IC Fabrication Environmental Trends

Unfortunately, the environmental impact trends for computer manufacturing are disconcerting. As related earlier, IC fabrication impacts dominate the overall system impacts. To further examine the trends the Boyd *et al.* of different fabrication generations and feature sizes of ICs used in computer systems [8] is revisited. Boyd *et al.* conducted a hybrid LCA using process LCA to analyze the actual manufacturing of the basic silicon wafer and the ICs from the wafer and using EIO-LCA to evaluate the impact from the actual fabrication equipment used in the manufacturing process. Further upstream, hybrid LCA was also used to study the environmental impact from the manufacturing process for the chemicals used in IC manufacturing.

[1]verified by the Fraunhofer ISM institute.

The results for energy consumption and GWP are summarized in Table V. Of particular interest is the energy normalized to die area. Throughout the late 1990's the energy requirements fell by about 40%. However, during the last decade this trend has reversed and the energy usage has increased by 30% and could continue to rise with new technologies. Unlike ICs, the PCB effort has been fairly constant for the last 10 years as shown in Table II. However, we see an increase in area for both the ICs and PCBs within the system from 2001 to 2010. A significant component of this increase appears to be from the addition of solid state drives (SSDs) [18]. Thus, this further supports that IC manufacturing methodologies must drive how environmental impacts are addressed in future computing systems.

TABLE V: Environmental impact from manufacturing ICs for a computer system [8].

Year	1995	1998	1999	2001	2004	2007	2010
Feature size (nm)	350	250	180	130	90	65	45
Energy (MJ/die)	184.8	111.9	89.3	78	79.4	89.4	88.4
GWP (kg CO_2e/die)	13	7	6	5	6	6	6
Area (mm^2)	196	150	125	140	140	140	111
Energy/mm^2 (MJ)	0.94	0.75	0.71	0.56	0.57	0.64	0.80
GWP/mm^2 (kg CO_2e)	0.066	0.047	0.048	0.036	0.043	0.043	0.054

These trends are highlighted in Fig. 2 that compare fabrication effort and impacts with technology feature size for ICs. What these trends show is that environmental impacts from fabrication appears to have reached a minimum point at 130nm. Unfortunately, as we descend below 90nm the environmental impacts per die area appears to increase sharply and non-linearly with feature-size. This trend is somewhat expected as the amount of sophistication in the fabrication process continues to increase as smaller technologies become ever closer to the physical limits of the materials.

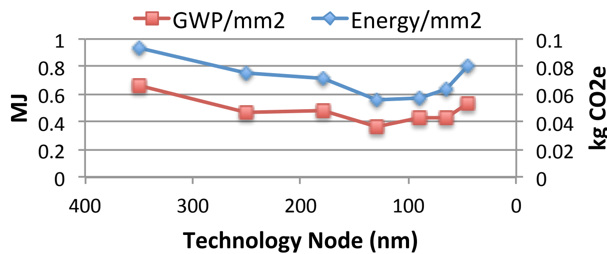

Fig. 2: IC fabrication energy and GWP usage trends.

A. Impacts of Emerging Technologies

These increasingly complex processes when combined with emerging technologies are expected to further exacerbate the environmental impacts per area of fabricated ICs. Examples of particular culprits include 3D integration for silicon and hybrid processes that integrate non-volatile memories. Additionally, the trend towards multi-and many-core and systems with "dark silicon" attempt to increase IC area to combat the use-phase (energy) costs of the system. *These trends increase manufacturing costs and environmental impacts.*

The introduction of hybrid CMOS methods to integrate new emerging devices on the chip, e.g., non-conventional non-volatile storage, in order to further reduce power consumption is a particularly troublesome trend from an environmental perspective. A significant component to the increase of IC area in workstation systems over the last decade can be attributed to tight integration of non-volatile storage [18].

The development of emerging technologies often introduce new materials that do not exist in the conventional CMOS process. Considering an example from magnetic storage, data is stored as the resistance of the magnetic tunneling junction (MTJ) device in magnetic memory cells. Fig. 3 shows the cross-section of a typical MTJ structure. Many elements, including Co, Fe, B, etc. do not commonly exist in conventional CMOS processes, though they are very popular materials in the fabrication of magnetic devices, e.g., recording heads.

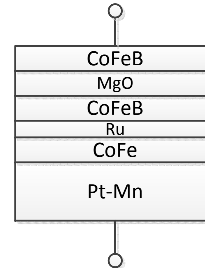

Fig. 3: Cross-section of a typical MTJ structure.

Our experience with a leading foundry shows that the contamination qualification process alone may require between nine and 12 months for hybrid integration processes that include magnetic memory. The required fabrication effort will also be significantly increased in the most popular low-cost design cycles for these technologies as follows: first, the back-end CMOS devices are fabricated in the foundry; second, the preparation of the magnetic device is conducted at a third party facility and integrated atop the back-end CMOS devices; and finally, the wafer is sent back to the original foundry to complete top-level interconnects and pads. To complicate the process, protective cover layers are required whenever the wafer is transferred between the CMOS foundry and magnetic foundry. The foundry reports that the cleaning process alone for each of the required additional layers in a hybrid process, including 3D CMOS, increases the disbursed gases (CO_2 and volatile organic compounds) as well as waste water generation.

The mechanics and potential complexity of the non-CMOS fabrication stages can further exacerbate environmental impacts. Recent device studies show that nano-ring structures have the potential to offer the lowest programming current density and thermal stability for magnetic devices in a highly scaled geometry [19]. Fig. 4 shows a nano-ring MTJ structure and the corresponding layout implementation from a leading foundry. To achieve the round shape of the MTJ cell, the layout is plotted as an octagon. The resulting diagonal orientation, however, goes against the preferred rules of the process. This special technology development increases contamination of the doped regions requiring additional protection (e.g., a SiN or SiO_2 cover) as well as additional surface cleaning, which increases energy consumption and waste water generation. Diagonal structures in traditional CMOS processes suffer from

similar concerns including a more complicated lithography process which reduces yield. A reduced yield also increases environmental impact by requiring additional units to be fabricated (including their impacts) to meet the need.

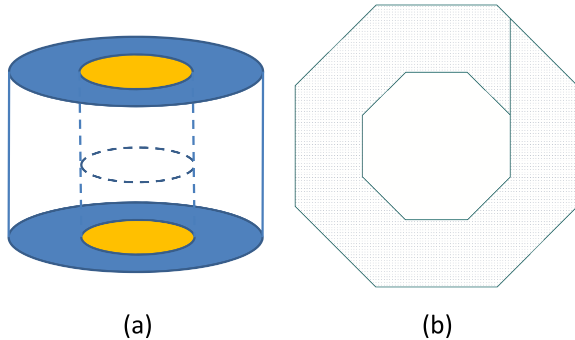

Fig. 4: Nano-ring MTJ. a) Structure. b) Layout.

IV. Conclusion

Increased attention must be paid to sustainability measures for computer systems, in particular ICs, beyond the use phase energy consumption. All of the phases of the life-cycle are impactful and must be considered in the overall environmental impact of the computer system. Towards this goal, we believe that sustainability of manufacturing for computer systems, and in particular their ICs, should become a *critical new measure* for future generation systems.

Using an LCA approach, which analyzes the impacts of a process or product from cradle to grave along with data published in the literature we provide evidence that manufacturing energy may equal or exceed the energy from the use phase. Relevant industry trends for IC fabrication include: (1) for smaller technology nodes, fabrication effort and environmental impact increases, as supported by data reported by Intel [18]; (2) more complicated fabrication including 3D integration and hybrid processes such as those integrating non-volatile memories on chip, will further increase the environmental impact per area; and (3) trends to increase chip area through multi-, many-, and highly heterogeneous core (e.g., dark silicon) will increase the size of ICs and consequently, their environmental impacts. Given these factors, *sustainability metrics are trending in the wrong direction.*

The tradeoff between manufacturing and use energy suggests that a pareto optimal point may exist for sustainability metrics of ICs. However, the current industry trends coupled with efforts on reducing use phase power consumption will exacerbate the environmental impacts of IC manufacturing. Thus, for truly green computing, *manufacturing energy and environmental impacts must be addressed in future systems.*

To address this problem, *design for sustainability* (DFS) of semiconductor fabrication must become a *new design methodology* for future generation ICs. Certain coarse grain measures have already been identified and can be leveraged in system design, some of which can be captured in cost metrics such as die area, semiconductor layers, metal layers, etc. However, as seen in Fig. 4, features of the process also have an impact and design rules can have an impact on the environmental impact. Unfortunately, the goal of reducing environmental impact, while related, is not directly in line with increasing yields through design for manufacturing (DFM).

Much work remains to be done just to improve the accuracy and availability of semiconductor LCA [18]. Further, to significantly address the issue of DFS in future IC design will require a significant investment from the foundries themselves to provide information on the impact of different design features on environmental impact parameters of energy, GWP, and waste-water generation.

References

[1] T. Wailgum, “Used pc strategy: Pass the ’toxic buck’ to developing countries,” *CIO Magazine*, July 2009.

[2] C. Scheuer, G. A. Keoleian, and P. Reppe, “Life cycle energy and environmental performance of a new university building: modeling challenges and design implications,” *Energy and Buildings*, vol. 2003, no. 35, pp. 1049–1064, 2003.

[3] S. Junnila and A. Horvath, “Life-Cycle Environmental Effects of an Office Building,” *J. of Infrastructure Systems*, pp. 157–166, Dec. 2003.

[4] A. K. Jones, L. Liao, W. O. Colling, H. Xu, L. A. Schaefer, A. E. Landis, and M. M. Bilec, “Green computing: A life-cycle perspective,” in *Proc. of the IEEE International Green Computing Conference*, June 2013.

[5] F. Taiariol, P. Fea, C. Papuzza, R. Casalino, E. Galbiati, and S. Zappa, “Life Cycle Assessment of an Integrated Circuit Product,” in *Proc. IEEE Intl. Symp. on Elec. and the Env.*, vol. 45, no. 6, Mar. 2001, pp. 128–133.

[6] E. D. Williams, R. U. Ayres, and M. Heller, “The 1.7 kilogram microchip: energy and material use in the production of semiconductor devices.” *Env. Sci. & Tech.*, vol. 36, no. 24, pp. 5504–10, Dec. 2002.

[7] N. Krishnan, S. Boyd, A. Somani, S. Raoux, D. Clark, and D. Dornfeld, “A hybrid life cycle inventory of nano-scale semiconductor manufacturing.” *Env. Sci. & Tech.*, vol. 42, no. 8, pp. 3069–75, Apr. 2008.

[8] S. Boyd, A. Horvath, and D. Dornfeld, “Life-cycle energy demand and global warming potential of computational logic,” *Env. Sci. & Tech.*, vol. 43, no. 19, pp. 7303–7309, 2009.

[9] M. Socolof, J. Overly, L. Kincaid, R. Dhingra, D. Singh, and K. Hart, “Life-cycle environmental impacts of CRT and LCD desktop monitors,” *Proc. IEEE Intl. Symp. on Elec. and the Env.*, pp. 119–127, 2001.

[10] A. K. Jönbrink, “Preparatory studies for Eco-design Requirements of EuPs: Lot 3 Personal Computers (desktops and laptops) and Computer Monitors,” IVF Ind. Research and Development Corp., Tech. Rep., 2005.

[11] E. Williams, “Energy intensity of computer manufacturing: hybrid assessment combining process and economic input-output methods.” *Env. Sci. & Tech.*, vol. 38, no. 22, pp. 6166–74, Nov. 2004.

[12] F. Curling, “Quelle est l’empreinte carbone d’un ordinateur?” February 2011.

[13] ISO, “Environmental management – life cycle assessment – requirements and guidelines,” International Organization for Standardization, Switzerland, Tech. Rep., 2006.

[14] C. Hendrickson, A. Horvath, S. Joshi, and L. Lave, “Economic Input-Output Models for Environmental Life-Cycle Assessment,” *Env. Sci. & Tech. Policy Analysis*, vol. 32, no. 7, pp. 184–191, 1998.

[15] W. Leontief, “Quantitative input and output relations in the economic systems of the united states,” *The Review of Economic Statistics*, vol. 18, no. 3, pp. 105–125, 1936.

[16] M. Bilec, R. Ries, H. S. Matthews, and A. L. Sharrard, “Example of a hybrid life-cycle assessment of construction processes,” *J. of Infrastructure Systems*, vol. 12, no. December, p. 207, 2006.

[17] R. A. Levy, Ed., *Microelectronic Materials and Processes*. Springer, 1989.

[18] M. A. Yao, T. G. Higgs, M. J. Cullen, S. Stewart, and T. A. Brady, “Comparative assessment of life cycle assessment methods used for personal computers.” *Env. Sci. & Tech.*, vol. 44, no. 19, pp. 7335–46, Oct. 2010.

[19] H. X. Wei, F. Q. Zhu, X. F. Han, Z. C. Wen, and C. L. Chien, “Current-induced multiple spin structure in 100nm ring magnetic tunnel junction,” *Phys. Rev. B.*, no. 77, p. 224432, 2008.