A 201mV/pH, 375 fps and 512×576 CMOS ISFET Sensor in 65nm CMOS Technology

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***Abstract* — This paper presents a high-gain and large-scale CMOS ion-sensitive field effect transistor (ISFET) sensor. The high-gain readout is achieved by a novel pH-to-Time-to-Voltage conversion (pH-TVC), which can greatly increase pixel density (small pixel size) with a high sensitivity. The proposed pH sensor consists of 512×576 pixel array with 3.9um×3.9um chemical sensing area, and is integrated with column-paralleled 10-bit single-slope ADCs to speed up data readout. It is fabricated in traditional TSMC 65nm process with 201mV/pH sensitivity and 375 fps readout speed, targeted for DNA sequencing.**

I. Introduction

ISFET sensor has been recently exploited from neuronal sensing, blood pH detection, to DNA sequencing [1-3]. It builds connection between aqueous solution and solid-state circuits by converting biochemical reaction to electrical signal. Traditional ISFETs are built with expensive specialized processes, since gate oxide is utilized as ion sensing membrane [1]. Improved structure proposed by J. Bausells *et al*, in which Si_3N_4 passivation layer is employed as the sensing membrane, makes ISFET sensors compatible and scalable with commercial CMOS technology [2]. Consequently, CMOS-based ISFET sensors have shown a great promise in Next Generation Sequencing (NGS) of DNA, due to its low-cost, high-speed, and large-scale characters [3].

The introduction of passivation layer, however, leads to several ISFET performance deteriorations. The first is the reduction of ISFET pH sensitivity due to the capacitive division effect. Besides, trapped charge and drift issues need to be considered for a robust ion sensor design [4]. Various solutions have been proposed to compensate the pH attenuating effect by coupling a smaller capacitance compared to the passivation capacitance [5], [6]. However, these methods are not feasible for a denser array, because when there is a small sensing area, an even smaller coupled capacitance will suffer from a larger process variation.

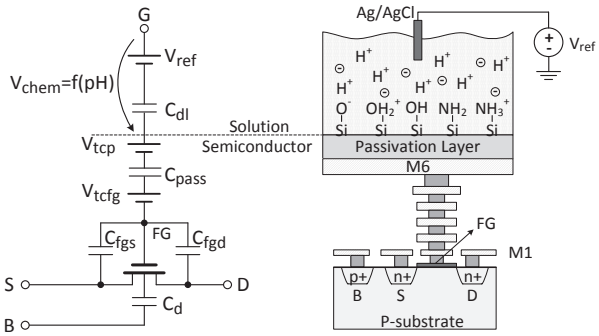

Fig.1. A capacitance-dependent ISFET model

In this paper, we propose a novel pH-TVC readout scheme to compensate the capacitive attenuation. Besides, we introduce a reset device to alleviate drift and trapped charge influence. In addition, column-paralleled ADCs are applied for high-speed readout. As validated in TSMC 65nm process, one can observe a 201mV/pH sensibility with a 375 fps readout speed for a 512×576 pixel array.

II. ISFET High-Gain Readout

A. ISFET Model

A capacitance-dependent ISFET model working in weak inversion is illustrated in Fig. 1. A stable reference electrode (Ag/AgCl) is applied as a remote ISFET gate. C_{dl} is the double layer capacitance formed at the solution and passivation interface [7]. In addition, trapped charge accumulated during fabrication is also depicted.

According to [4], ISFET V_{th} can be expressed as:

$$V_{th(ISFET)} = V_{chem} + V_{tc} + V_{th(MOSFET)}/A \qquad (1)$$

where V_{chem} is the grouped chemical-related potential; V_{tc} is the combined trapped charge potential in the passivation V_{tcp} and the floating gate V_{tcfg}; and A is the capacitive division factor caused by passivation capacitance.

V_{chem}, V_{tc}, and A are further summarized as follows:

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$$V_{chem} = \gamma + 2.303\alpha U_T pH \quad (2)$$

$$V_{tc} = V_{tcp} + V_{tcfg}/A \quad (3)$$

$$A = \frac{C_{pass}}{(C_{pass}+C_{ox}//C_d+C_{fgd}+C_{fgs})} \quad (4)$$

where γ represents all non-pH related potential; C_{pass}, C_{ox}, and C_d are the passivation, oxide, and depletion capacitances respectively; C_{fgd}, and C_{fgs} are the parasitic capacitances associated with the floating gate.

For a weak inversion ISFET, where $V_{GS}<V_{th(ISFET)}$, the drain current I_D can be expressed as [8]:

$$I_D = I_0 \cdot K \cdot \exp \frac{-A \cdot 2.303\alpha U_T pH}{nU_T} \quad (5)$$

where K represents all the non-pH related terms, and $n = 1+C_d/C_{ox}$ is the non-ideal slope factor. According to (5), ISFET drain current is reduced by A. This division effect can degrade the ISFET sensor sensitivity.

B. pH-TVC Readout Scheme

For large ISFET sensor array in scaled-down CMOS process, the division effect becomes significant. This paper proposes a new ISFET readout structure illustrated in Fig. 2. Three-transistor per pixel is used: MN_0 is the ISFET device, MN_1 is the row-selected device, and MN_2 is a reset device. MN_2 can remove the trapped charge by providing a discharge path to the substrate. Besides, drift can be also alleviated by resetting note "FG" to a given voltage, regardless of variation in solution.

Here is the working principle. The capacitance C_0 is first pre-charged to VDD by MP_0. During the pH sensing phase, a discharge path will be formed by turning off MP_0 and tuning on MN_1. From the previous discussion, a change in pH will modify ISFET V_{th} value, so does the ISFET drain current, which in turn affects the discharging time at node "N_0". Following this pH-to-time conversion is another time-to-voltage conversion, in which voltage difference will be observed at node "N_1" when switch S_0 is turned off at a given time. Note that MN_3 is the source follower (SF) device to avoid charge redistribution between C_0 and the input capacitance of the following column ADC. I_0 is the current bias of MN_3.

For the solution with an initial H^+ concentration of pH_1, the local DNA slice at one micro-well above one ISFET pixel will cause a shift in pH value, which results in a new concentration of pH_2. As a result, the pH-related voltage change at node "N_1", ΔV_{pH}, can be defined as:

$$\Delta V_{pH1} = V_{DD} - V_{pH1} = I_{pH1} \cdot \frac{\Delta t}{C_0} \quad (6)$$

$$\Delta V_{pH2} = V_{DD} - V_{pH2} = I_{pH2} \cdot \frac{\Delta t}{C_0} \quad (7)$$

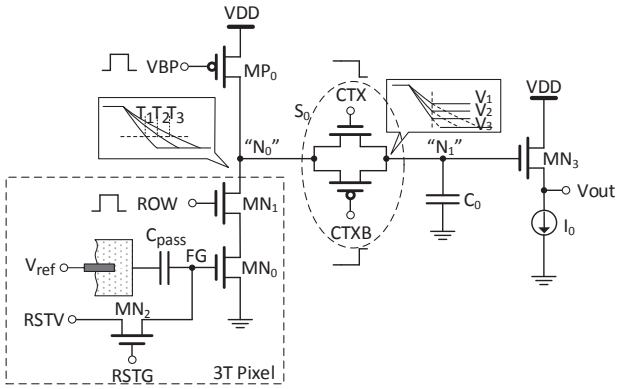

Fig.2. The proposed pH-TVC readout structure

$$\Delta V_{pH} = V_{pH1} - V_{pH2} = \Delta V_{pH1} \cdot (\frac{I_{pH2}}{I_{pH1}} - 1) \quad (8)$$

where I_{pH1} and I_{pH2} are the ISFET currents related to pH_1 and pH_2, respectively. V_{pH1}, and V_{pH2} are the relative output voltages at node "N_1" after a given sensing time Δt. ΔV_{pH} can be improved by increasing the ratio between I_{pH2} and I_{pH1}. Therefore, the small ISFET input signal is amplified in pixel level instead of using external amplifier [3], which can greatly increase readout signal to noise ratio.

Based on (5), the pH sensitivity to ΔV_{pH} of ISFETs working in subthreshold region is given by:

$$\Delta V_{pH} = \Delta V_{pH1} \cdot [\exp \frac{A \cdot 2.303\alpha U_T \cdot (pH_1 - pH_2)}{nU_T} - 1] \quad (9)$$

Since ΔV_{pH} is exponential to pH change, the capacitive division effect is compensated. As a result, a denser ISFET array with a smaller pixel pitch can be realized.

III. LARGE-ARRAYED SENSOR ARCHITECTURE

A large-scale 512×576 ISFET sensor top architecture is shown in Fig. 3, including pH-TVC readout circuits, 10-bit column-paralleled single-slope ADCs, SRAM groups, row decoder and column decoder. For large pixel array, the column readout circuit should be as simple as possible to be aligned with the pixel size.

The pH change is first converted to voltage difference by pH-TVC circuit, and then is turned into 10-bit digital data by ADC, following which the data is stored in the SRAM groups and read out column by column controlled by external clock.

The sensor timing diagram is illustrated in Fig 4. Before each pH sensing phase, a reset phase will be first conducted to alleviate drift and trapped charge effect. Compared to circuit operation time, chemical reaction on the passivation surface is much slower [7]. Consequently, the sensor should continuously detect the solution to track the surface potential trends.

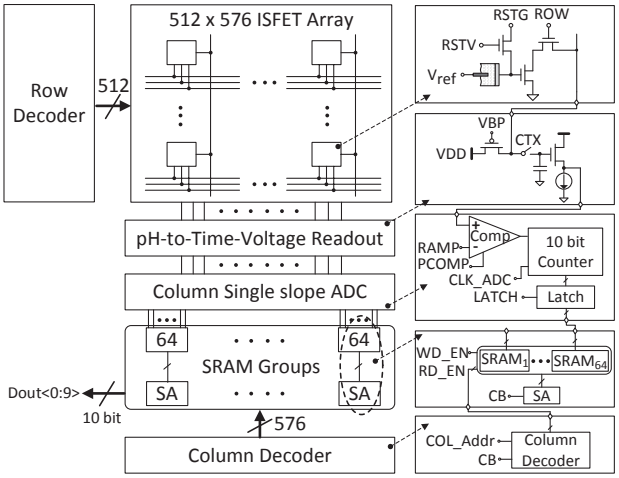

Fig 3. CMOS ISFET sensor top architecture

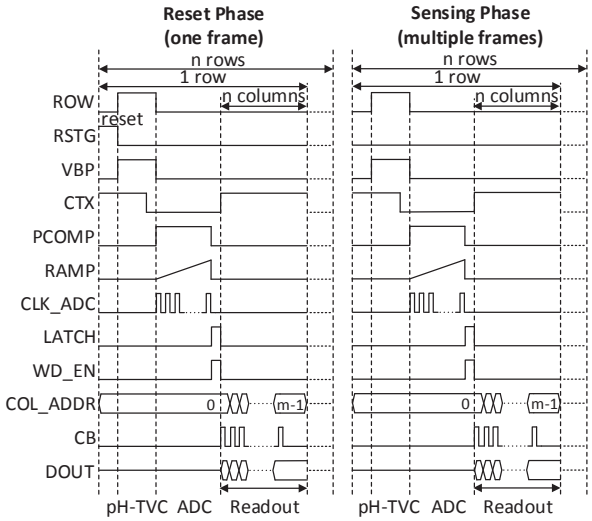

Fig 4. CMOS ISFET sensor timing diagram

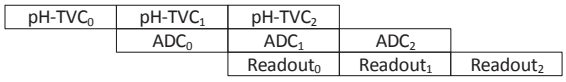

Fig 5. ISFET sensor pipelined operation diagram

Accordingly, there are three independent operations: pH-TVC, ADC, and readout, which are implemented in SoC. Pipelined operations is applied to improve readout speed, which is depicted in Fig. 5. As such, row time is determined by the longest operation. The simulation result has shown a speed of 375 fps to be achieved.

IV. Results and Discussion

The ISFET sensor is implemented in unmodified TSMC 65nm process thanks TSMC contribution. The chip occupies an area of 5mm×5mm as shown in Fig. 6.

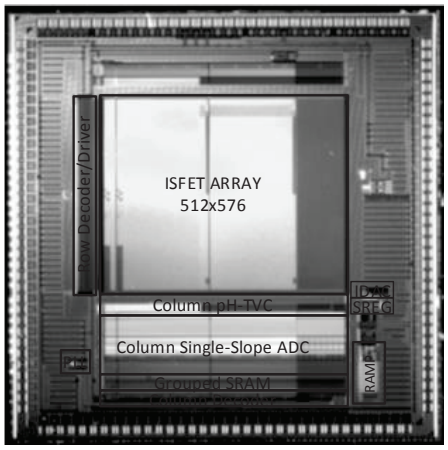

Fig 6. CMOS 512×576 ISFET sensor chip in 65nm process

TABLE I
SUMMARY OF 65NM CMOS ISFET SENSOR

Pixel pitch	4.4 μm
ISFET size (*W/L*)	0.4 μm /0.28 μm
Chemical sensing area	3.9 μm × 3.9 μm
C_{pass}	0.39 fF
C_{ox}	0.69 fF
A	0.308
Passivation surface pH sensitivity	46 mV/pH
pH to node "N_1" voltage sensitivity	201mV/pH
Total Pixel array size	512 × 576
ADC	10 bit
Readout clock	200 MHz
Frame rate	375 fps

The passivation layer is comprised of series of Si_3N_4 and SiO_2 layers, and the overall passivation capacitance per area is 0.026fF/μm^2. The oxide capacitance per area is 6.16fF/μm^2. The depletion region capacitance C_d, and parasitic capacitances are dependent on ISFET gate voltage. The parameters of ISFET pixel and specifications of ISFET sensor are summarized in Table I.

Firstly, as shown in Fig. 7, we can observe the system pH-TVC output voltages with various pH values, from pH_0 to pH_4 with 1 pH step increase. H^+ reaction on the passivation surface will charge the ISFET floating gate, which is first accumulated and then amplified by the pH-TVC readout circuit. A maximum of 201mV/pH sensitivity at node "N_1" can be obtained, indicating a nearly 14-fold of electrical amplification considering the capacitive division factor *A*.

Additionally, the system is immune to drift and trapped charge effects as shown in Fig. 8. Drift and trapped charge may lead to large and unpredictable voltage deviation [4], nevertheless the system can still identify the pH change. It is attributed to the reset device in each pixel, since trapped charge can be removed and drift can be eliminated.

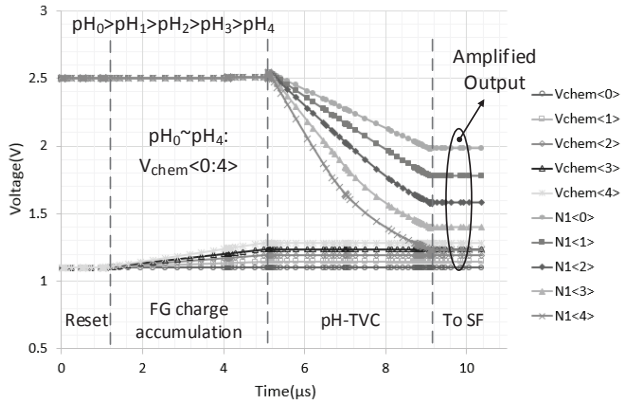

Fig 7. System pH-TVC results from pH_0 to pH_4

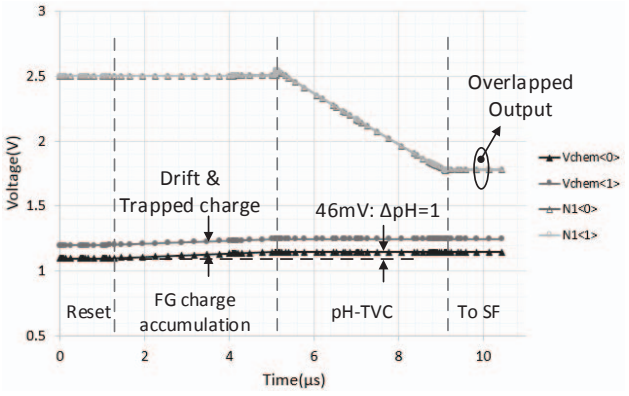

Fig 8. System pH-TVC results with reduced drift and trapped charge effects

What is more, the employment of column-paralleled ADCs, grouped SRAM structure and pipelined readout strategy can greatly improve system readout speed. The comparison with ISFET sensors reported in literatures [3, 9-10] is summarized in Table II. The proposed ISFET sensor is thereby applicable for large-array pixel design with high sensitivity and high readout speed.

V. Conclusion

This paper has proposed a high-gain and large-arrayed CMOS ISFET sensor. By employing a novel pH-to-time-to-voltage conversion scheme, the ISFET output voltage to pH sensitivity can be largely improved, regardless of capacitive division effect introduced by the passivation capacitance in CMOS process. Validated in TSMC 65nm process, a 512×576 pixel array with 3.9um×3.9um chemical sensing area is integrated with column-paralleled 10-bit single-slope ADCs to speed up data readout. One can observe 201mV/pH sensitivity and 375 fps readout speed, which can be promising towards DNA sequencing.

TABLE II
Comparison of ISFET Sensors

Ref.	[9]	[10]	[3]	**This paper**
Process	0.35µm CMOS	0.35µm CMOS	0.18µm CMOS	**65nm CMOS**
ISFET size (µm/µm)	-	5/0.35	4.8/0.3	**0.4/0.28**
Pixel pitch (µm×µm)	14×14	11.2×11.2	10×10	**4.4×4.4**
Array size	16×16	64×64	64×64	**512×576**
Sensitivity (mV/pH)	17	20	26.2	**201**
Frame rate (fps)	333	100	1200	**375**

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