9.3 A 60GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications

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Recent advances in silicon technology, mm-Wave integrated circuit/antenna/package design, and beam-forming techniques at 60GHz, together with the emergence of suitable wireless standards, have enabled consumer electronics products to support wireless transmission of multi-Gb/s data such as high-definition (HD) audio/video content [1,2]. Further expansion into portable and mobile platforms will require lower power consumption, smaller form factor, and lower cost. This paper describes a fully integrated, low-cost 60GHz phased-array transceiver pair, implemented in 65nm standard digital CMOS and packaged with an embedded antenna array, capable of robust 10m non-line of sight (NLOS) communication. The array is configurable from 32 elements to 8 or fewer elements, making the transceiver pair suitable for both fixed, high-data-rate and portable, low-power applications. To enhance the robustness of the multi-element design, dynamic phase shifters allow the beam direction to be changed in real time to adapt to changing environments without interruption of the multi-Gb/s data stream. The transceiver pair supports the WirelessHD and draft 802.11ad (WiGig) standards at maximum data rates of 7.14Gb/s and 6.76Gb/s, respectively.

Figure 9.3.1 shows the block diagram of the Source and Sink transceivers along with the frequency plan. The baseband (BB) and IF circuit blocks are fully differential while the RF/mm-Wave blocks are single-ended. The design methodology for the mm-Wave circuit blocks relies on accurate high-frequency device models and the use of coplanar waveguide transmission lines for power matching [3]. The Source and Sink transceivers share common circuit blocks in the BB to RF signal paths, and in the LO generation. However, the 60GHz signal distribution and number of RF transmit (TX) and receive (RX) elements for the two chips are different to allow for an asymmetrical link. In the high-data-rate direction, the Source uses 32 TX elements to transmit to 32 RX elements on the Sink. For the reverse lower-data-rate direction, the Sink uses 8 TX elements to transmit to 4 RX elements on the Source. The number of active elements can be configured on both transceivers allowing a trade-off between power dissipation and performance.

The BB I/Q channels in the TX path include a VGA and a 1GHz low-pass filter. Upconversion from BB to IF is performed by a double-balanced I/Q mixer. The upconversion to RF is performed by a double-balanced mixer power matched to the first splitter stage. The RF signal is distributed to the *M* TX elements via a tree of active 1:2 3dB splitters. Each RF TX element consists of an active phase shifter (PS) and power amplifier (PA). The PA provides more than 22dB of gain over 8GHz of bandwidth to ease linearity requirements of the preceding stages. Programmable bias of the PA allows for a trade-off between power consumption and linearity. The OP_{1dB} can be varied from 0dBm to +9dBm with a peak power-added efficiency of 22%. A power detector (PD) at the PA output allows the transmitted power to be controlled.

The RX path consists of *N* elements, each containing a low-noise amplifier (LNA) and PS, followed by passive 2:1 power combiners. The 3-stage LNA provides more than 20dB of gain, with two coarse gain steps to ease linearity requirements of subsequent stages. After power combining, the downconversion to IF is performed by a single-gate mixer loaded by an IF VGA. A double-balanced I/Q mixer downconverts to BB and is followed by the BB VGA and filter. The BB and IF VGAs provide fine gain control in addition to the gain steps available at RF.

The transceivers use a dual-conversion sliding IF architecture with local oscillator (LO) frequencies at $f_{RF}/5$ and $4f_{RF}/5$. The synthesizer generates the $f_{RF}/5$ LO centered at one of two channels, 12.096GHz or 12.528GHz. Spot phase noise of the carrier at 75kHz and 1MHz offsets when centered at 60.48GHz was measured at the TX output to be -66dBc/Hz and -96dBc/Hz, respectively. The phase-noise profile satisfies both WirelessHD and WiGig requirements for 64-QAM transmissions. The $4f_{RF}/5$ LO is generated by a frequency quadrupler. The LO path for the TX RF mixer and simplified circuit schematic of the quadrupler are shown in Fig. 9.3.2. The quadrupler consists of two stages of frequency doubling and a cascoded output buffer. Cascodes M_{1A} and M_{1B} are biased at subthreshold and form a push-push doubling stage that sums the drain currents to select even-order harmonics. M_2 is also biased at subthreshold and performs another frequency doubling. Explicit filtering of unwanted harmonics at the output of the second doubler is not required due to the selectivity provided by subsequent matching networks along the LO chain. The quadrupler output buffer, M_3, improves reverse isolation and provides a match to the directional coupler. The amplitude of the $4f_{RF}/5$ LO is monitored by the LO PD and controlled by a feedback loop. At the mixer LO port, a dual transformer architecture is used to convert the single-ended LO to a well-balanced differential signal. The 50Ω damping resistor at the virtual ground of the second transformer stabilizes the mixer. The mixer achieves better than 40dBc of LO suppression.

Bare die were tested at RF frequencies on a probe station, and packaged die were tested over-the-air paired with digital BB chips designed for the WirelessHD 1.0 standard. The CMOS ICs are flip-chip bonded to a multiple-metal-layer interconnected ceramic package with integrated antennas. Full ESD protection is provided on all I/Os. Fig. 9.3.3 shows the received constellation achieving an EVM of -19.2dB for a 16-QAM 512 carrier OFDM signal with channel bandwidth of 1.76GHz and PHY rate of 3.8Gbps. In this mode the system is transmitting 3.0Gb/s of uncompressed 1080p/60Hz video in a 10m NLOS scenario. The transmitted spectrum and WirelessHD spectral mask [4] shown in Fig. 9.3.3 exhibits minimal spectral regrowth at an EIRP of +28dBm.

Figure 9.3.4 shows a computed array factor for the Source and Sink arrays for a typical operating link. Paired with the WirelessHD BB chip, whenever an interferer blocks the current path the system performs a dynamic beam search to find the new optimal path using the electronically steerable phased array. Beam search takes less than 1ms. The system also allows for adaptation of the PHY data rate to accommodate for difficult wireless environments. Figure 9.3.5 shows the trade-off between the PHY rate and range for different Source and Sink configurations in both the LOS and typical NLOS cases. A further trade-off between power consumption and data rate/range can be made by adjusting the number of active elements. For example, dropping the number of active Source TX elements from 32 to 8 reduces the power consumption by more than half, at the cost of a 4x decrease in range. In this scenario, the link still supports multi-Gb/s data rate in both directions.

Performance of the transceivers is summarized in Fig. 9.3.6, and die micrographs are shown in Fig. 9.3.7. The areas of the Source and Sink die are 72.7mm^2 and 77.2mm^2 respectively including pads. Both transceivers meet worldwide in-band and spurious emission regulatory limits. The presented transceiver pair achieves the required low-cost, robust performance, and low-power configurations to extend multi-Gb/s data-rate capabilities to both fixed and portable applications.

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References:
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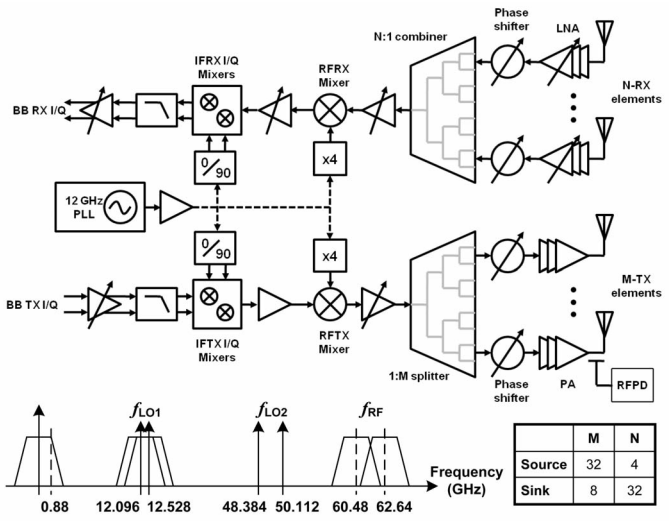

	M	N
Source	32	4
Sink	8	32

Figure 9.3.1: System block diagram and frequency plan.

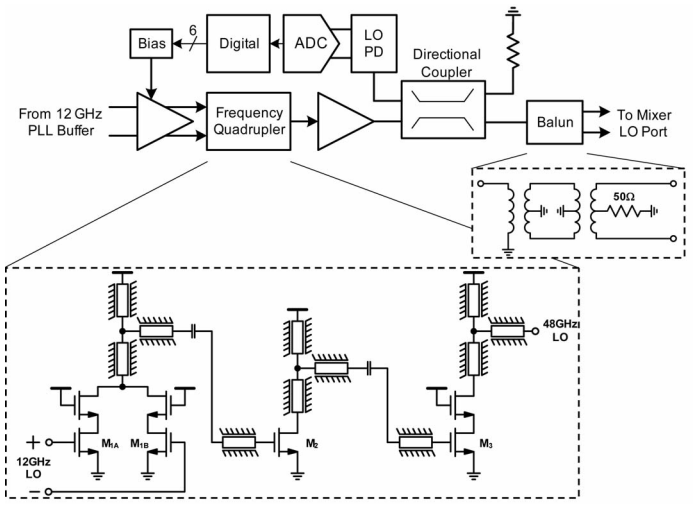

Figure 9.3.2: Block diagram of LO distribution and schematics of the frequency quadrupler and double-transformer balun.

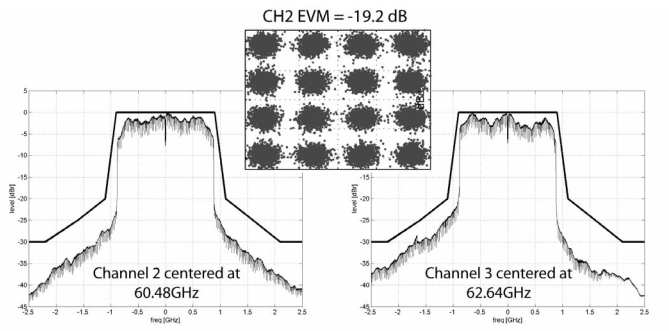

Figure 9.3.3: Transmit spectrum and WirelessHD spectral mask for Channels 2 and 3, and the received constellation for Channel 2.

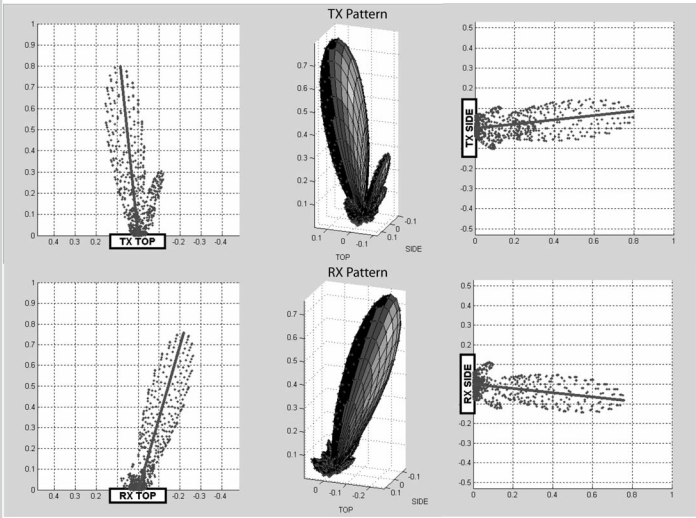

Figure 9.3.4: Computed amplitude patterns for the Source and Sink transceivers.

	Data Rate	Forward Channel Range† (m)	
		32 Element Source To 32 Element Sink	8 Element Source To 32 Element Sink
LOS	3.8 Gb/s	50	13
	1.9 Gb/s	184	47
	0.95 Gb/s	390	101
NLOS*	3.8 Gb/s	16	4
	1.9 Gb/s	58	15
	0.95 Gb/s	123	32

* NLOS distances are dependent on the quality of any reflection in the signal path. NLOS range here assumes a reflection with 11 dB loss exists between Source and Sink.

† Range is the distance at which the packet error rate exceeds 10^{-3}

Figure 9.3.5: Range of the system for various PHY rates for both LOS and NLOS cases.

Technology	65nm Digital CMOS			
Supply Voltage	1.0V, 2.5V(PLL, I/O)			
Supported Channels	59.40GHz ~ 61.56GHz, 61.56~63.72GHz			
Data Transfer Rate	4 Gb/s			
Link Margin	14dB, operating at 10m, 1080p/60Hz 4:4:4 video with BER≤10^{-11}			
Source Chip Performance				
Die Size	8.95mm x 8.12mm			
Number of RF Elements	32 TX, 4 RX			
EIRP	+28 dBm			
EVM	<-19 dB @ +28 dBm EIRP			
Mode	32 TX elements on		8 TX elements on	
Temperature	25°C	75°C	25°C	75°C
Tx Power Consumption	1.82W	2.16W	895mW	1.03W
Sink Chip Performance				
Die Size	8.64mm x 8.93mm			
Number of RF Elements	32 RX, 8 TX			
RX Sensitivity	-72 dBm at each antenna element, HRP full rate			
RX Max Signal (all RX antenna on)	-32 dBm at each antenna element			
RX Noise Figure	< 10dB			
Mode	32 RX elements on		4 RX elements on	
Temperature	25°C	75°C	25°C	75°C
Rx Power Consumption	1.25W	1.54W	711mW	786mW

Figure 9.3.6: Summary table of the transceiver performances.

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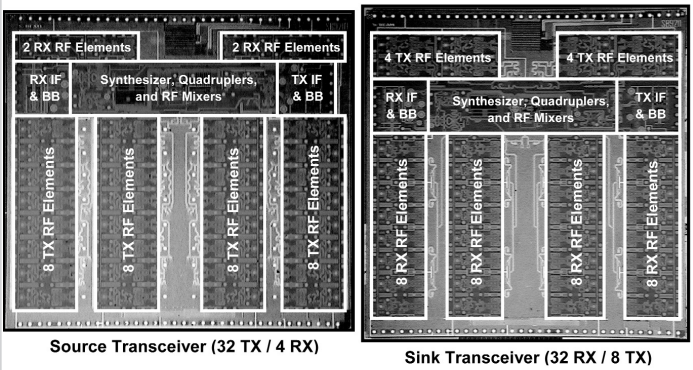

Figure 9.3.7: Die micrographs for the Source and Sink transceivers.

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