A 42 to 47-GHz, 8-bit I/Q Digital-to-RF Converter with 21-dBm P_{sat} and 16% PAE in 45-nm SOI CMOS

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***Abstract*— A novel stacked FET digital-to-RF converter is implemented in 45-nm SOI CMOS, which shares DC current through an I/Q digital-to-analog converter (DAC), I/Q mixer, and stacked-FET PA to provide high output power. The proposed architecture transmits at 1.25 Gbps for QPSK at 45GHz. This transmitter exhibits a 21.3-dBm saturated output power, while achieving a peak PAE of 16%. The circuit occupies 0.3mm^2 including pads, while the PAE and P_{sat} remains above 13% and 18 dBm from 42 to 47 GHz.**

***Index Terms* — CMOS SOI, Power amplifier, Direct Conversion, Power DAC, Stacked FET, Digital-to-RF Converter.**

I. Introduction

High-power, high-efficiency RF modulators are needed to keep pace with the growth in communication at millimeter-wave bands. Higher spectral efficiency motivates the application of complex QAM modulations rather than ASK or BPSK [1]. Traditionally, III-V technologies have been preferred for power amplification at millimeter-wave bands. However, CMOS technology lowers costs and allows for higher system integration. In this paper, an entire I/Q transmitter is integrated including DAC, mixers, and power amplifier stages. Highly-scaled CMOS suffers from low breakdown voltage and low Q of the passive circuit elements, which lowers reliability as well as amplifier efficiency and linearity. Recent work at 45 GHz in 45-nm SOI CMOS has demonstrated a stacked-FET PA with 18.6-dBm Psat and 34% PAE and indicates that SOI CMOS is a feasible alternative to III-V technology for these applications [2][3]. New architectures and approaches are required to enable CMOS-based mm-wave transmitters to have comparable efficiency and output power to III-V implementations.

To achieve high output power and high efficiency with the high peak-to-average power ratios of QAM modulation, this paper proposes a new stacked-FET transmitter in 45-nm SOI CMOS at 45 GHz shown in Fig. 1, which shares a common DC current through an I/Q digital-to-analog converter (DAC), I/Q mixer, and stacked-FET PA to provide high voltage swing without exceeding the breakdown voltage of the transistors in the stack. Whereas earlier work has demonstrated high supply voltages to generate high-power swings, these designs have supported low resolution and were only capable of providing ASK or BPSK signals [1][4]. The circuit approach proposed here provides high RF output power at high efficiency along with a high-resolution DAC control to transmit complex modulation schemes. The use of high-resolution DACs enables the use of digital predistortion (DPD) to improve the error vector magnitude (EVM) [1][4].

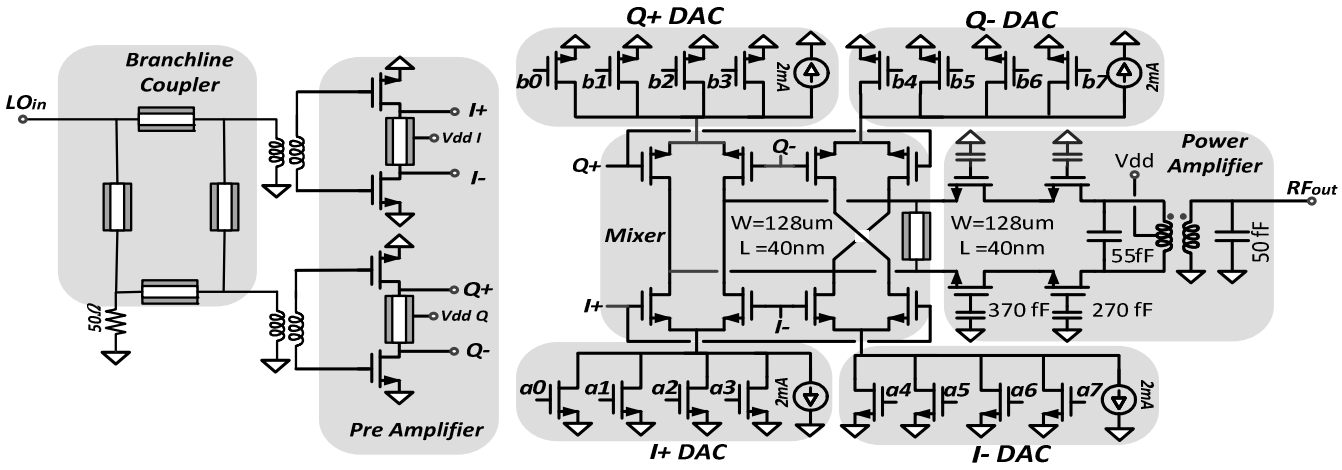

Fig. 1. Schematic of the high power digital-to-RF converter implemented in 45-nm SOI CMOS process.

II. DIGITAL-TO-RF CONVERTER DESIGN

The proposed digital-to-RF converter (DRFC) is based on a stacked-FET amplifier shown in Fig. 1. High RF voltage swings are possible through stacking of transistors. The stack resembles a cascode, but the gate capacitors allow the gate voltage to vary with the drain and source. This allows the voltage supply to be shared across multiple transistors biased with the same d.c. current. The bottom (common-source) FET provides the DAC current. The second (common-gate) FET is part of the I / Q mixer. The mixer is implemented as a differential homodyne upconverter with four DACs. Finally, the two top (stacked) FETs form a current buffer that allows a high output voltage swing.

The gate biases of the FETs are selected so that the drain-source voltages of all the power devices are identical and below the breakdown voltage of the technology, which is approximately 1.3 V [2][3]. The geometry of the FETs in the PA and their gate capacitors are each designed to provide the optimal load for the previous stage as well as keeping the gate-drain voltage below the breakdown voltage [2][3].

In traditional class-A, class-AB and class-B PAs, the RF output power is roughly proportional to the input power, and the efficiency of the PA biased in class-A and class-B is respectively proportional to the output power and the square root of the output power [4]. Therefore, the best efficiency achievable at 6 dB back-off output power is respectively one half and one quarter of the peak efficiency for the class-B and class-A PAs.

The proposed circuit controls the output power by changing the DAC current as well as the input LO power. Simulations indicate that improved back-off efficiency is achieved from the DRFC by changing the DAC current rather than changing the input LO power. Fig. 2 shows the simulated drain efficiency (DE) and the power gain of the transmitter for 185 mA and 145 mA of DAC DC currents while changing the LO power, where the power gain is defined as

$$Gain = \frac{P_{out-RF}}{P_{in-LO}}. \quad (1)$$

A branchline coupler and two baluns are used to generate LO_{I+}, LO_{I-}, LO_{Q+} and LO_{Q-} as shown in Fig. 1. The generation of the quadrature signals from the input LO and the losses associated with this circuitry are included in the DRFC performance characterization.

Fig. 2 shows that the DRFC operates at the highest efficiency as the gain – defined by (1) – compresses. Note that similar efficiency can be achieved at different output powers through adjusting the DAC DC current and LO power.

Two pseudo-differential common-source amplifiers amplify the I_{LO} and Q_{LO} before applying them to the DRFC to improve the gain of the system and operate with 1.1 V supply to minimize the effect of their power consumption on the overall efficiency of the system. The biases and power supplies of these amplifiers are provided from separate pads to enable the correction of the phase and gain mismatches of the I and Q channels.

The DRFC is operated in class-B mode to achieve the highest efficiency. To operate in class-B, the I+ DAC – shown in Fig. 1 - is turned *off* when the I- DAC is *on*, or vice versa. This maximizes the efficiency without degrading the output power. A 2 mA keep-alive current is utilized with each DAC to improve linearity and control the voltage swing across each FET, which might compromise reliability if the current drops to zero with a 4 V supply. A shunt 50Ω CPW is utilized for inter-stage matching [2] between the mixer and the PA shown in Fig. 1. Simulations indicate that this inter-stack matching network improves the efficiency by approximately 3%. It is possible to use the inter-stack matching between the sources of the last FETs in the stack. However, simulations indicate an insignificant efficiency improvement that does not justify the required layout area and complexity.

To minimize pad area limitations, a serial-to-parallel converter demuxes high-speed input data. Current mode logic (CML) is used to maximize the speed of these blocks. Measurements indicate proper operation to 13.5 Gbps.

The output amplitude of the DRFC is constant for BPSK and QPSK constellations ignoring the transition periods between different points in constellation. However, to generate a 16-QAM signal, the output amplitude and phase change simultaneously. As shown in Fig. 1, cascode transistors are avoided in the design for efficiency considerations. Varying current through the DAC transistors, the drain voltage of these devices are modulated, which results in current nonlinearity. These nonlinearities are not critical in BPSK or QPSK modulations, however in a QAM signal they cause high EVM even at low data rates. These errors can be corrected to some extent using digital predistortion; however the other solution would be to use cascode devices to provide better isolation, at an efficiency penalty of approximately 2%.

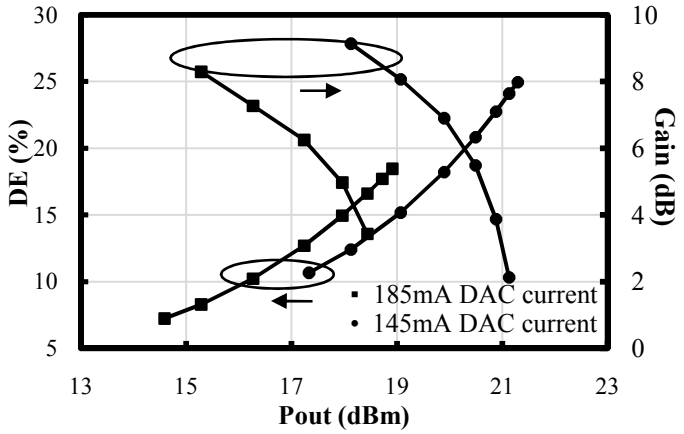

Fig. 2. Simulated DE and gain of DRFC for two different DAC currents, while sweeping the LO power.

III. MEASUREMENT RESULTS

The microphotograph of the DRFC is shown in Fig. 3. The area of the circuit is 1.15mm^2 with a significant area overhead for the branchline coupler and baluns that generate differential quadrature signals from the input LO. The tested chip also contains a serial-to-parallel converter.

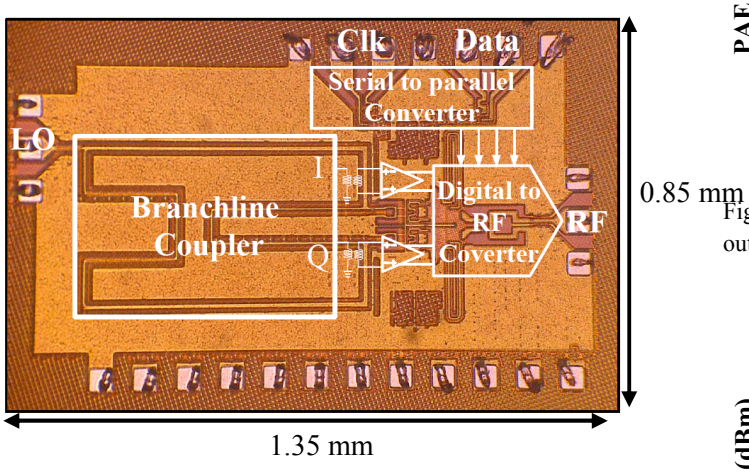

Fig. 3. Photomicrograph of digital-to-RF converter.

As shown in Fig. 1, three on-chip baluns are used in the design of the DRFC. Two of these baluns generate differential *I* and *Q* LO signals and an output balun converts differential signal to single-ended for the purpose of measurement and calibration. The loss of the output balun is calculated by measuring the *S*-parameters of two back-to-back baluns and each balun is found to have approximately 1.45 dB loss at 45-GHz. This loss is de-embedded from the power measurement.

Fig. 4 shows the simulated and measured PAE, DE and gain as a function of output power, i.e. the LO power is varied, at the highest DAC current level, e.g. I+ = 1111, I- = 0000, Q+ = 1111 and Q- = 0000. The DRFC achieves a saturated output power of 21 dBm at 45 GHz with peak PAE of 16% and peak gain of 7.1dB. The peak drain efficiency is 24%

The maximum output power and maximum PAE of the DRFC are measured as a function of frequency in Fig. 5. The circuit exhibits more than 18 dBm saturated output power from 42 to 47 GHz, while the PAE remains above 13% over the same range.

To illustrate the ability of the DRFC to generate complex constellations such as 16-QAM, the output power is measured for various points of a QAM constellation. Fig. 6 shows the measured drain efficiency as a function of output power (input LO power sweep) at five digital *I* / *Q* pairs. The measurement indicates a 0.3 dB amplitude mismatch between *I* and *Q* channels. The error is corrected by increasing the power supply of the *I* or *Q* preamplifier.

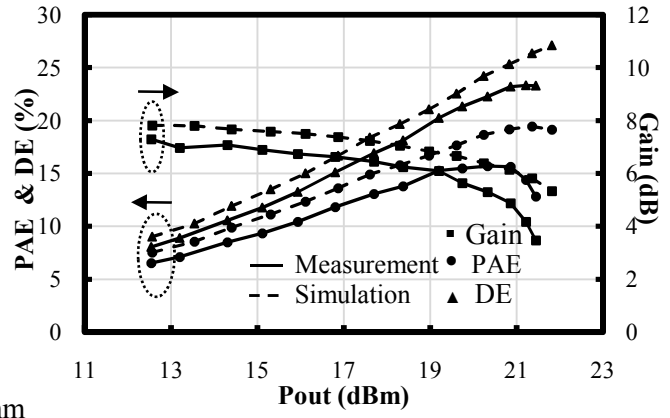

Fig. 4. Measured and simulated gain, PAE and DE as a function of output power.

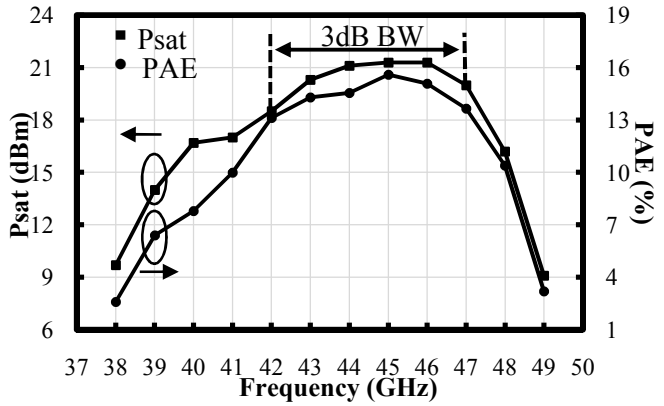

Fig. 5. Measured peak PAE and saturated output power as a function of frequency.

The error vector magnitude (EVM) is measured by downconverting the RF output from 45GHz to 3GHz and sampling the signal for digital demodulation. The measurement shows that the DRFC is capable of generating BPSK, QPSK and 16QAM signals with a 45GHz carrier at data rates in excess of 1 Gb/s. The uncalibrated measurement shows a BPSK signal to a maximum 735 Mbps and a QPSK signal at 1.2 Gbps at less than 4% and 7% EVM, respectively. According to [5], these EVM results correspond to BERs lower than 10^{-7} and 10^{-4} for BPSK and QPSK signals. A 16-QAM signal at 40 Mb/s showed an EVM of 9% and the data rate was limited by interfaces with the test equipment at this time. The EVM of the modulated signal as a function of the symbol rate is shown in Fig. 7 for BPSK, QPSK and 16QAM modulations.

The 4-bit DACs in the *I* and *Q* channels support the use of digital predistortion on low-order constellations. The use of predistortion improves the errors due to circuit mismatch. Fig. 8 shows how the EVM of QPSK signal improves using predistortion at different symbol rates.

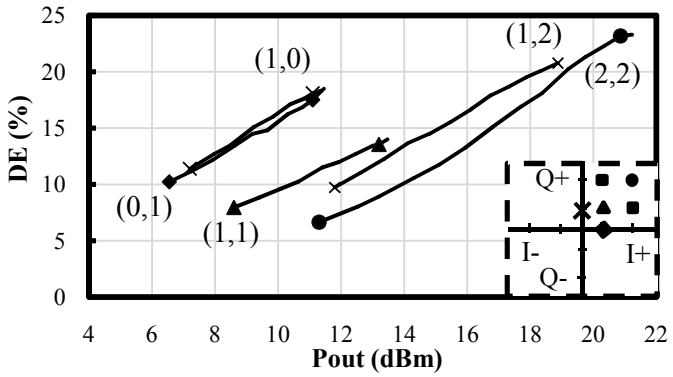

Fig.6. Measured DE as a function of output power for different points in constellation, while sweeping the LO power.

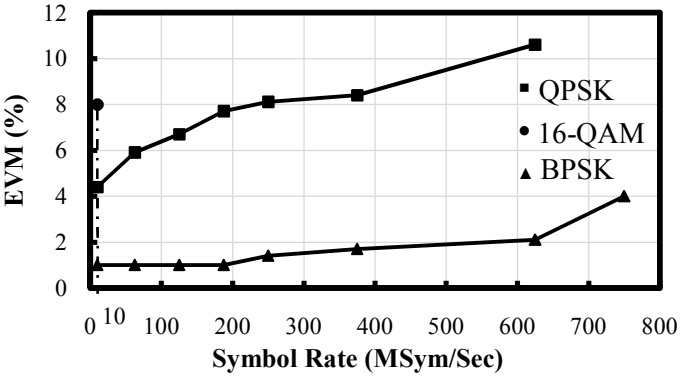

Fig.7. Measured EVM for BPSK, QPSK and 16QAM as a function of symbol rate.

Table I summarizes the measured performance and compares the results with recently published mm-wave modulators. This work demonstrates extremely high-power and efficiency, while generated higher-order complex modulation.

Table I

Comparison of millimeter-wave modulators

Technology	**45nm CMOS SOI**	120nm SiGe BiCMOS	45nm CMOS SOI
References	**This Work**	[7]	[6]
Freq (GHz)	**42-48**	40-45	40-50
Supply (V)	**4**	2.5	4.2-5.1
Modulation/ Symbol Rate/EVM	**BPSK/ 750Mbps/4%** **QPSK/ 1.25Gbps/5.5%** **16QAM/ 40Mbps/8%**	64QAM/ 48Mbps/2.1%	ASK/ 1.25Gbps/- BPSK/ 2.5Gbps/ -
Psat (dBm)	**21.3**	1	23.5-24.3
Peak PAE (%)	**16**	-	22-14.6
Area (mm^2)	**1.15**	5	0.77

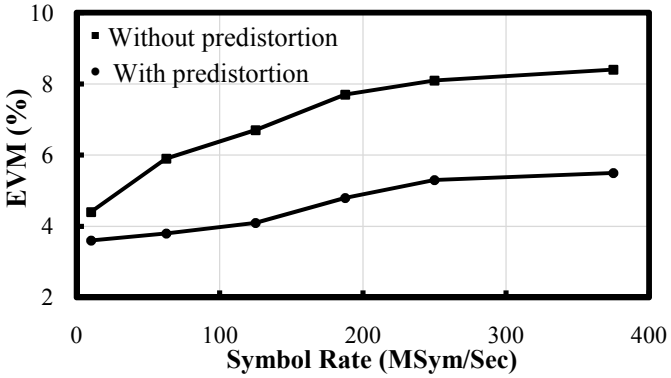

Fig.8. Measured EVM for QPSK with and without predistortion as a function of symbol rate.

VII. Conclusion

A novel 42-47GHz stacked-FET digital-to-RF converter is implemented in 45-nm SOI CMOS. Sharing current through a FET stack, DRFC provides 21.3 dBm saturated output power at a peak PAE of 16% into a 50 Ohms load impedances at 45 GHz. The proposed architecture generates a 1.25-Gbps QPSK at an EVM of 5.5% using digital predistortion.

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