4 GHz Locking Range and 0.19 pJ Low-Energy Differential Dual-Modulus 10/11 Prescaler

Takeshi MITSUNAKA
SHARP Corporation
Fukuyama, Japan

Masafumi YAMANOUE
SHARP Corporation
Fukuyama, Japan

Kunihiko IIZUKA
SHARP Corporation
Fukuyama, Japan

Minoru FUJISHIMA
Hiroshima University
Higashi-Hiroshima, Japan

***Abstract*—In this paper, we present a differential dual-modulus prescaler based on an injection-locked frequency divider (ILFD) for a satellite low noise block (LNB) down converter. Three stage differential latches using ILFD and a cascaded differential divider can achieve divide-by-10/11 operations with a lock range of 2.1 GHz – 10 GHz at a supply voltage of 1.4 V and an operating frequency range of 2.1 GHz – 6.1 GHz at a supply voltage of 1 V. At our target frequency, 5 GHz, a minimum energy of 0.19 pJ (=mW/GHz) at the maximum input frequency can be achieved. Our proposed circuit is fabricated by a 130 nm CMOS process, and the prototype chip core area is 40 × 20 μm^2**

I. INTRODUCTION

In many parts of the world, satellite television broadcasts provide a wide range of channels and services. A low noise block (LNB) down converter in a satellite dish translates the RF satellite signal in the Ku-band (10.7 – 12.75 GHz) to an IF signal in the L-band (950 – 2150 MHz). Generally, the LNB down converter has 9.75 GHz, 10.6 GHz and 11.3 GHz local oscillator (LO) signal frequencies. The integrated phase lock loop (PLL) in an LNB down-converter IC must generate these three LO signal frequencies. An integer-N-type PLL using a 25 MHz crystal oscillator as a reference can serve the purpose.

In the integer-N-type PLL, a dual-modulus prescaler is the most important circuit. The prescaler should be energy-efficient and should have a high speed so that it is capable of modulus control from the fixed input frequency. In addition, it should have a wide locking range to cover the PVT variation. A dual-modulus prescaler based on the current-mode logic (CML) has been widely used in PLLs owing to its wide locking range and high frequency capability [1]-[3]. However, it is difficult for the CML to meet the increasing demand for lower power consumption. To reduce the power consumption of frequency dividers, modulus-controlled prescalers using injection locked frequency dividers (ILFDs) have been proposed recently [4]-[9]. Although they consume less power than CML dividers, single-phase clock prescalers [5]-[9] cannot take differential input signals, therefore, they are affected by supply voltage noise resulting in an incorrect operation. A voltage control oscillator (VCO) output is also differential circuit. Therefore, it is desirable for a prescaler of the integrated PLL to use differential circuits. In this paper, a digitally controlled differential dual-modulus 10/11 prescaler using ILFD is presented to achieve a smaller die area, a lower power consumption, and a wider locking range.

II. DESCRIPTION OF THE PROPOSED DUAL-MODULUS PRESCALER

Fig. 1 shows a block diagram of PLL with the pulse swallow architecture. The dual-modulus prescaler, enclosed by a thick line, is the focus of this article. To alleviate the required operation speed of a prescaler, we insert a divider between VCO and the dual-modulus prescaler.

Fig. 2 shows our proposed latch block of the dual-modulus prescaler based on ILFD. An NMOS switch (M1 or M2) is inserted between a differential pair of NMOSs (M3 and M5 or M4 and M6) and between a cross-coupled pair of NMOSs (M7 and M9 or M8 and M10) to inject an input differential signal into ILFD. In the case of high-speed and low-power ILFDs, it is a common practice to design them with a single ended input [5]-[9]. However, they are affected by supply voltage noise resulting in an incorrect operation, and they can operate only around the self-resonant frequency, therefore, their locking range tends to be narrow. To tolerate supply voltage noise and broaden the lock range, we proposed differential signal switches based on ILFD.

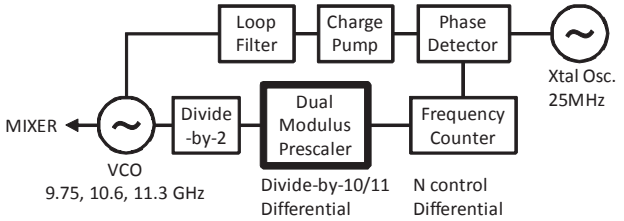

Figure 1. Block diagram of PLL with pulse swallow architecture.

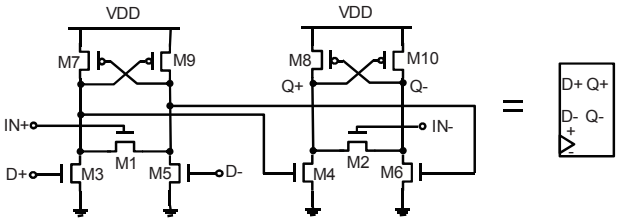

Figure 2. Proposed latch block of differential dual-modulus prescaler based on ILFD.

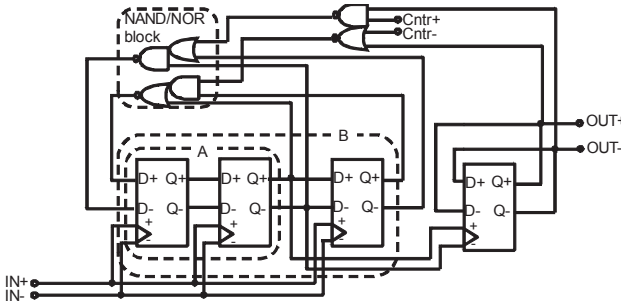

Figure 3. Dual-modulus prescaler designed using latch blocks.

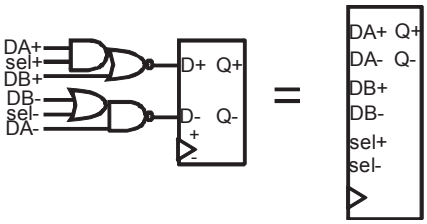

Figure 4(a). Latch block merged with NAND/NOR block.

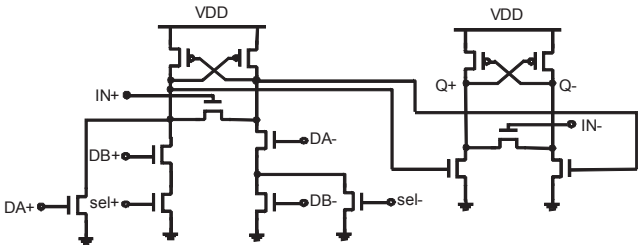

Figure 4(b). Schematic of latch block merged with NAND/NOR block.

Fig. 3 shows the dual-modulus prescaler designed using the latch blocks in Fig. 2. The divide-by-4 block is created by two-stage differential latch blocks (dashed line A) and the divide-by-6 block is created by three-stage differential latch blocks (dashed line B). Then, the divide-by-5 output is

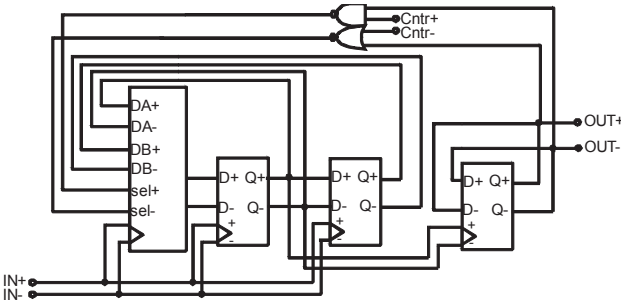

Figure 5. Dual-modulus prescaler designed using latch blocks.

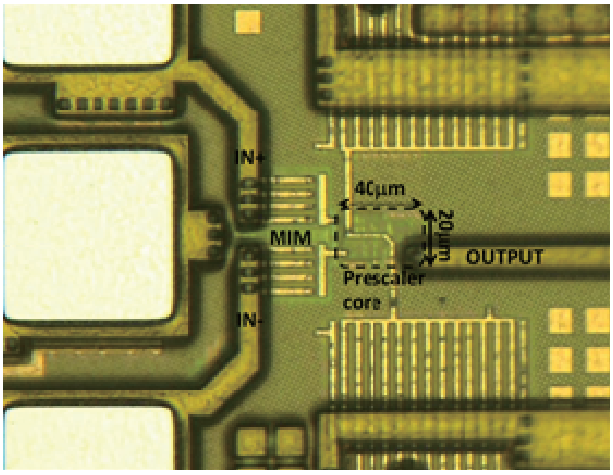

Figure 6. Die photograph.

generated by the NAND/NOR block with divide-by-4 and divide-by-6 blocks. The divide-by-10 output is generated by using the divide-by-5 output as the input to the cascaded divide-by-2 block. On the other hand, the divide-by-11 output is generated by using the divide-by-5 and divide-by-6 outputs alternately. The division ratio is controlled by the modulus control signal "Cntr+/-" from the latter frequency counter. To avoid the delay time of the NAND/NOR block, the latch circuit is merged with the NAND/NOR block, which realizes a high-speed latch through modulus control as shown in the Fig. 4 (a). Fig. 4 (b) shows a schematic of the latch circuit merged with the NAND/NOR block. Fig. 5 shows a complete schematic of the proposed differential dual-modulus 10/11 prescaler, which consists of the three-stage latches in Fig. 2 and Fig. 4 and the cascaded divider with a division ratio of 2.

III. Measurement Results

The proposed dual-modulus prescaler is implemented in 130 nm CMOS process. A die photograph of the dual-modulus prescaler is shown in Fig. 6. The core size is 40 × 20 μm^2, excluding the pads and the input DC-cut MIM capacitors. Fig. 7 shows the measurement system. For the

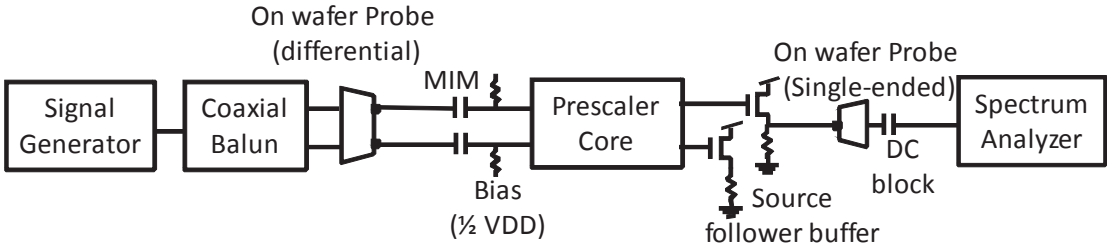

Figure 7. Measurement system

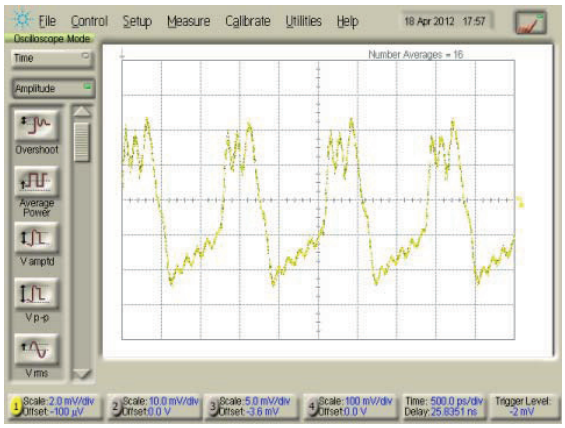

Figure 8(a). Divided-by-10 output signal.

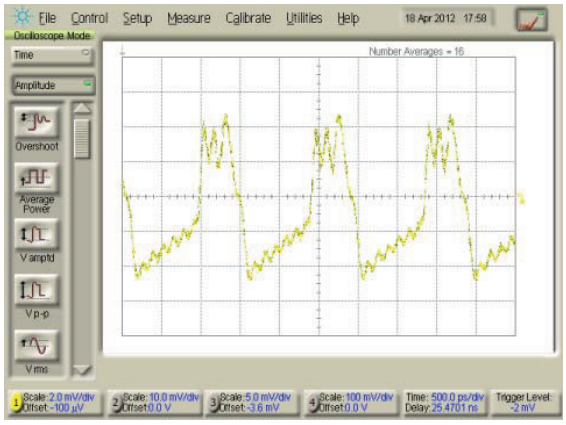

Figure 8(b). Divided-by-11 output signal.

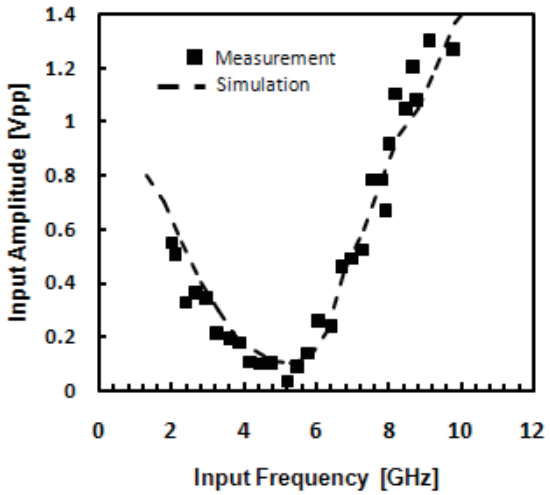

Figure 9(a). Divided-by-10 sensitivity.

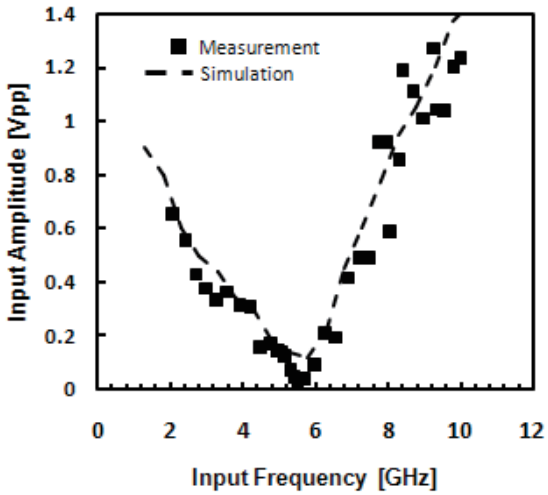

Figure 9(b). Divided-by-11 sensitivity

differential input, a coaxial balun is used without impedance matching. To measure the output signal, a simple differential source follower buffer with 50 Ω impedance matching is used. To measure only the output frequency, one of the differential outputs is used. Fig. 8 shows the output signal waveform of the dual-modulus prescaler obtained through the source follower buffer for (a) divide-by-10 and (b) divide-by-11 operations at an input frequency of 5 GHz. Plots of simulated and measured input sensitivities as a function of operating frequency at the supply voltage of 1.4 V are shown in Fig. 9 (a) for divide-by-10 operation and in Fig. 9 (b) for divide-by-11 operation. Although the cascade divider limits the minimum operating frequency to 2.1 GHz, measurement results show good agreement with simulation results for both the division ratios of 10 and 11.

The locking range as a function of center frequency is shown in Fig. 10 for various supply voltages and various prescalers of differential circuits. The locking range of the proposed dual-modulus prescaler is from 2.1 GHz to 10.1

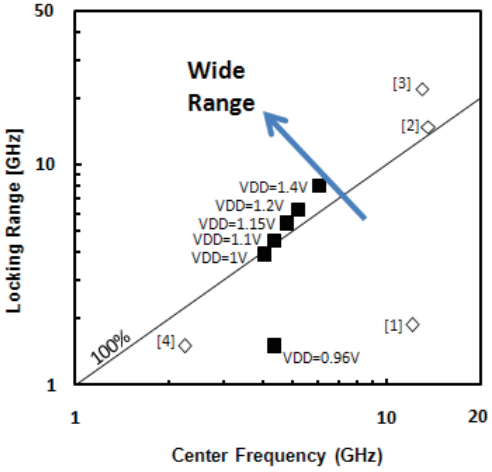

Figure 10. Locking range as a function of center frequency.

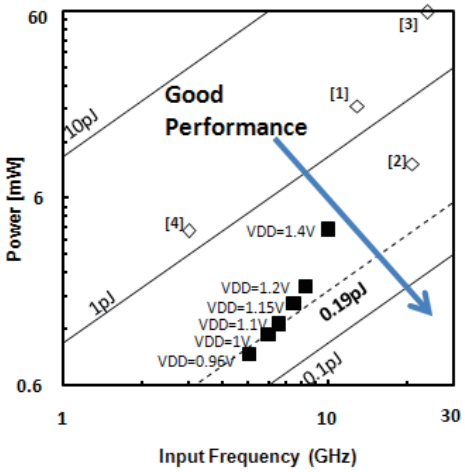

Figure 11. Energy of maximum operating frequency.

GHz therefore, the locking range per center frequency (=$\Delta f/f_{Center}$) is 131 % at the supply voltage of 1.4 V. $\Delta f/f_{Center}$ decreases with supply voltage, but it is 100 % at the supply voltage of 1 V. To cover the PVT variation, the dual-prescaler should operate up to 100 % as $\Delta f/f_{Center}$. In particular, the LNB down converter should be used in the open, and the locking range should be wide per center frequency.

The energy of maximum operating frequency, which is defined as the unit power consumption per maximum operating frequency (= mW/GHz, pJ), is shown in Fig. 11 for various supply voltages. In this figure, various prescalers of differential circuits are also compared. In the dual-modulus 10/11 prescaler operation, the energy decreases as the supply voltage decreases. The operating frequency is 6.1 GHz at the supply voltage of 1 V with the power consumption of 1.11 mW. In this case, the energy is 0.19 pJ. As shown in Fig. 11, the proposed dual-modulus prescaler achieved the minimum energy of operating frequency with a high locking frequency such as 100 % of $\Delta f/f_{Center}$. The proposed dual-modulus prescaler achieved a low operation energy in terms of the maximum input frequency in comparison with conventional prescalers.

IV. Conclusion

A dual-modulus prescaler based on ILFD that realizes a low power consumption and a wide locking range was proposed. It was fabricated by a 0.13 µm CMOS process. The energy of maximum operating frequency is 0.19 pJ with the up to a locking frequency that is 100 % of the $\Delta f/f_{Center}$. The energy of maximum operating frequency at our target frequency, 5GHz, was compared with that of conventional modulus prescalers. The comparison showed that the proposed dual-modulus prescaler achieves a smaller energy of maximum operating frequency.

References

[1] Evan Eschenk and Kamran Entesari, "A Low Noise 13 GHz Power Efficient 16/17 Prescaler with Rail to Rail Output Amplitude" Proceeding of Circuit and Systems, 2007. MWSCAS 2007. 50th Midwest Symposium on, pp. 427 – 430.

[2] Yanping Ding and Kenneth K. O, "A 21-GHz 8-Modulus Prescaler and a 20-GHz Phase-Locked Loop Fabricated in 130-nm CMOS", IEEE J. Solid-State Circuits, vol. 42, no. 6, JUNE 2007, pp 1240 – 1249..

[3] Hans-Dieter Wohlmuth and Daniel Kehrer, "24GHz Dual-Modulus Prescaler in 90 nm CMOS", Proceeding of Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on, pp 3227 - 3230.

[4] Ahmdd MlRael, "A 5 GHz, 1.5 Volt and very low-power CMOS frequency synthesizer for wireless communications" , Proceeding of Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on, pp III-536 –539.

[5] Ram Singh Rana, "Dual-Modulus 127/128 FOM Enhanced Prescaler Design in 0.35-µm CMOS Technology", IEEE J. Solid-State Circuits, vol. 40, no. 8,AUGUST 2005, pp 1662 – 1670.

[6] M.Vamshi Krishna, et.al., "A 1.8-V 6.5-GHz Low Power Wide Band Single-Phase Clock CMOS 2/3 Prescaler", Proceeding of Circuit and Systems, 2010. MWSCAS 2010. 53th Midwest Symposium on, pp. 149 – 152.

[7] Joonhee Lee and Seonghwan Cho, "A 470-µW Multi-Modulus Injection-Locked Frequency Divider with Division Ratio of 2, 3, 4, 5 and 6 in 0.13-µm CMOS", IEEE Asian Solid-State Circuits Conference, 12-3, November, 2007, pp. 332 – 335

[8] Zhiming Deng and Ali M. Niknejad, "The Speed–Power Trade-Off in the Design of CMOS True-Single-Phase-Clock Dividers", IEEE J. Solid-State Circuits, vol. 40, no. 11,NOVEMBER 2010, pp 1662 – 1670

[9] Xiaopeng Yu et. al, "Sub-mW Multi-GHz CMOS Dual-Modulus Prescalers Based on Programmable Injection-Locked Frequency Dividers", Radio Frequency Integrated Circuits Symposium 2008, RTU1D-3, pp.431-434.