A Quadrature Class-G Complex-Domain Doherty Digital Power Amplifier

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***Abstract*—An efficient digital quadrature power amplifier is presented. It shows a good system efficiency (SE) at back-off, demonstrating four efficiency peaks with the combination of a dual-supply Class-G and complex-domain Doherty (CDD) in the IQ plane. The proposed digital quadrature transmitter in 65-nm CMOS demonstrates 27.8-dBm peak output power (P_{out}) with a peak SE of 32.1%. For an 802.11ax 40-MHz (20-MHz) 1024-QAM OFDM signal with 13.1-dB (12.4-dB) peak-to-average power ratio (PAPR), it demonstrates an error vector magnitude (EVM) of -42.0 dB (-43.3 dB) at an average P_{out} of 14.7 dBm (15.4 dBm). The average SE measured with a 20-MHz single-carrier 1024-QAM signal with 6.8-dB PAPR at 21-dBm P_{out} is 18.4%.**

***Keywords*— Class-G power amplifier (PA), digital transmitter, quadrature transmitter, digital PA (DPA), RFDAC, switched-capacitor PA (SCPA), Doherty, voltage-mode Doherty (VMD).**

I. Introduction

Modern wireless communication systems require RF transceivers with very low power consumption, high linearity, and wide bandwidth to support the demand for a very high data throughput for mobile subscribers. For example, communication standards such as 802.11ax require high linearity of <–40-dB error vector magnitude (EVM) and a bandwidth of up to 160 MHz. High linearity and wide bandwidth enable a very fast communication speed, while increased energy efficiency gives an extended life for battery-powered devices. For improved power efficiency and output power (P_{out}), many power amplifier (PA) architectures such as Doherty [1], Class-G [2][3], power combining [3][4], polar [5], and digital PA (DPA) [1]–[7] have been investigated. Doherty architecture demonstrates an improved efficiency with an additional efficiency peak through load modulation, while Class-G provides multiple efficiency peaks at power back-off (PBO) with multiple supply voltages. For DPAs, an enhanced Class-G technique demonstrated an improved efficiency and linearity associated with the distributed transition of supply voltages over multiple unit cells [2].

A combination of these techniques could lead to better efficiency. For example, a polar Class-G DPA with Doherty configuration demonstrates a high average efficiency with multiple efficiency peaks at the PBO region. A recent work based on voltage-mode Doherty (VMD) [3] demonstrated an efficient transformer (XFMR) power combining by utilizing two XFMR primary windings concurrently even at the deep PBO region.

A polar transmitter has a good output power and energy efficiency, but it shows a limited bandwidth and requires a complex system implementation such as a coordinate rotation digital computer (CORDIC) and a wideband phase modulator [6]. On the other hand, a quadrature transmitter has a great advantage in its wide bandwidth and simple system architecture. Fig. 1 shows simplified examples of various power combining configurations. The solid and dashed arrows indicate the output vectors of sub-PAs, and the dotted arrow shows the vector sum at the combined PA output. A polar PA in Doherty configuration (Fig. 1 (a)) uses output vectors in the same phase in both main and peak PAs for the output impedance modulation and an extra efficiency peak at the PBO region. However, in this configuration, the phase needs to be modulated externally with a phase modulator. A quadrature PA configuration (Fig. 1 (b)) combines two orthogonal in-phase (I) and quadrature (Q) vectors using XFMR, but its P_{out} and efficiency are degraded because each sub-PA is dedicated to the orthogonal I and Q vectors.

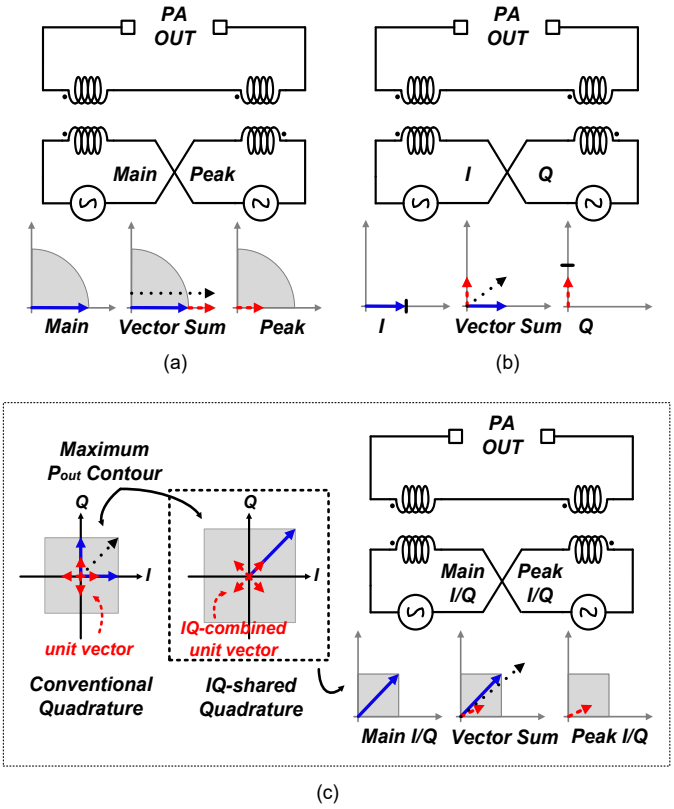

Fig. 1. PA architectures with XFMR power combining: (a) a polar PA in Doherty configuration, (b) a quadrature PA with dedicated I/Q sub-PAs, and (c) a quadrature PA in CDD configuration.

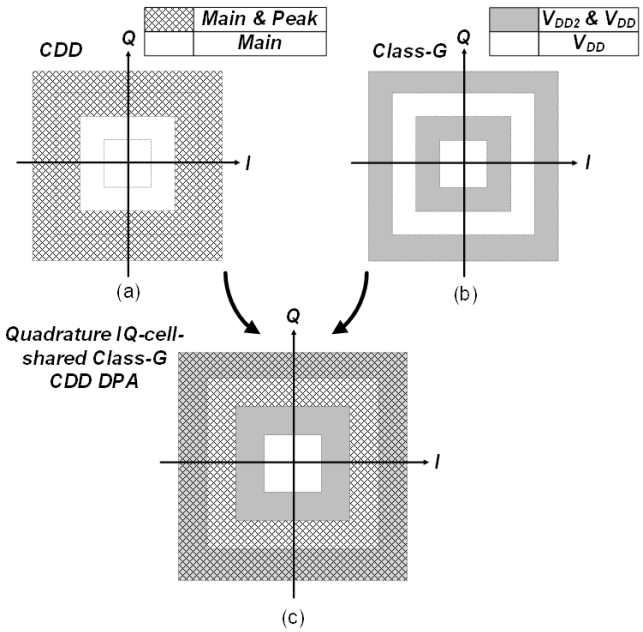

Fig. 2. Operation region vs. I/Q codes for (a) CDD, (b) Class-G, and (c) the quadrature IQ-cell-shared Class-G CDD DPA.

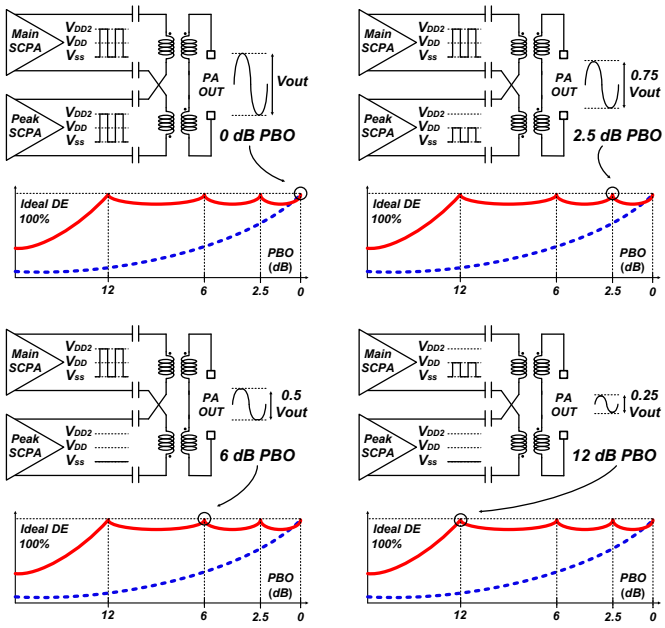

Fig. 3. Ideal DE curve for the Class-G CDD DPA for the output vector with 45°, 135°, 225°, or 315° angle.

II. Design of the Proposed Quadrature IQ-cell- Shared Class-G Complex-Domain Doherty DPA

A. Theory of Operation

A quadrature IQ-cell-shared DPA [7] can generate an output vector in the complex domain as in the conventional quadrature configuration without a phase modulator. The maximum P_{out} and efficiency are significantly improved in comparison to the conventional quadrature configuration (Fig. 1 (b)) because the output vector is not represented by the orthogonal I and Q vectors generated by the dedicated sub-PAs as shown in Fig. 1(c). Proposed complex-domain Doherty (CDD) improves the efficiency with additional efficiency peaks at the PBO region because the peak PA operates only when the main PA generates a maximum P_{out}. The CDD provides a load modulation as in the conventional Doherty configuration for vector components with the same angle, while it expresses the complete complex domain as in the quadrature configuration for orthogonal vector components. The proposed quadrature DPA based on IQ-cell-shared Class-G switched-capacitor (SC) PA (SCPA) operates in the CDD configuration as described in Fig. 1(c). Each main and peak quadrature Class-G IQ-cell-shared SCPA delivers the maximum P_{out} at 45°/135°/225°/315° with IQ-combined unit vectors [7] as shown in Fig. 1(c). The output vectors with different angles in the main and peak Class-G PAs are coupled with XFMR in VMD configuration to achieve multiple efficiency peaks in the complex domain.

Fig. 2 illustrates the operation region in the complex domain of the proposed DPA with CDD and dual-supply Class-G architecture. In Fig. 2 (a), the area marked with a diagonal grid depicts the operation region where both main and peak PAs are turned on, and the white area shows the low-power region where only the main PA operates. The Class-G operation is also implemented for both main and peak PAs, which adds two efficiency peaks in addition to the efficiency peak for Doherty operation. In Fig. 2 (b), the grey area indicates the region of the Class-G operation with both V_{DD} and VDD2 (=2VDD) supply voltages, and the white area represents the area with only V_{DD} supply voltage. The combined operation with CDD and dual-supply Class-G in the complex domain is illustrated in Fig. 2 (c). The detailed operation of the proposed DPA in different PBO regions is illustrated in Fig. 3. An ideal drain efficiency (DE) curve for the output vector with the 45°, 135°, 225°, or 315° angle demonstrates multiple efficiency peaks at 0-dB, 2.5-dB, 6-dB, and 12-dB PBO as shown in Fig. 3. The ideal DE shows an efficiency peak associated with the Doherty at 6-dB PBO and two additional efficiency peaks associated with the Class-G at 2.5-dB and 12-dB PBO. The efficiency curve also shows a smooth transition between different supply voltage domains and between main/peak PAs due to the continuous changes in supply voltages and impedance.

B. Overall Architecture

The proposed 12b quadrature DPA, as shown in Fig. 4, consists of 11b main and peak DPAs that are integrated with a VMD power-combining XFMR for impedance modulation in the complex domain. It operates as a standalone transmitter and generates an RF signal from digital I/Q data without a CORDIC or a phase modulator. As described in Fig. 4, a four-phase signal generator is used to generate the four IQ-combined unit vectors in the quadrature transmitter. Each main and peak PA is a quadrature IQ-cell-shared Class-G SCPA. The most significant bits of the I/Q data are assigned to select the main and peak PAs, and the next 5 and 6 bits are

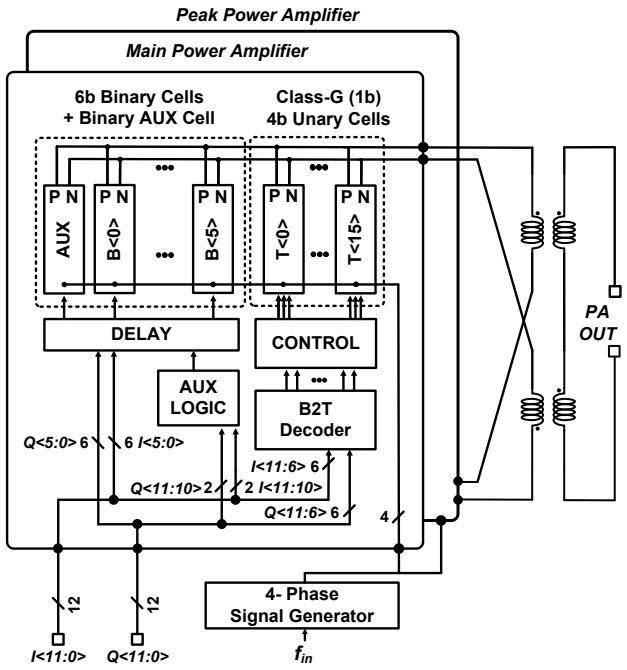

Fig. 4. Block diagram of the quadrature IQ-cell-shared Class-G CDD DPA.

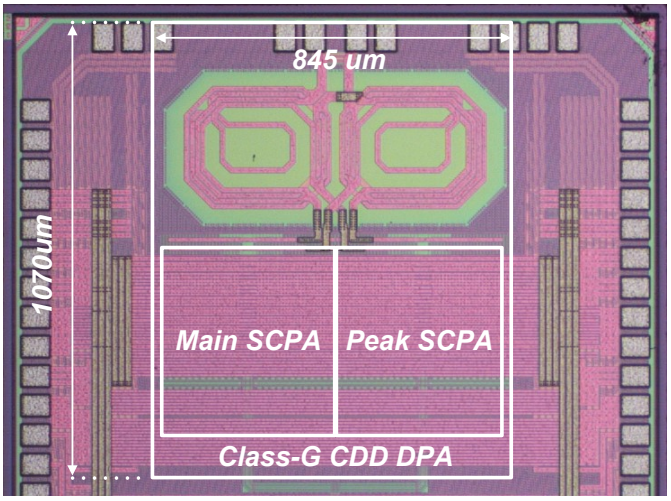

Fig. 5. Die photograph.

allocated to the unary and binary cells of each PA, respectively.

For the linearity in the digital transmitters or DPAs, it is important to match the unary and binary cells. For a better matching, two sets of binary cells are allocated to main and peak PAs even though only one set is required to represent the complete I/Q domain. In addition, multiple delay cells are utilized to compensate for the unwanted delay mismatch between the main and peak PAs and between the unary and binary cells.

III. Measurement Results

The prototype of the quadrature IQ-cell-shared Class-G CDD DPA, fabricated in a 65-nm RF CMOS process, occupies a chip area of 1.07×0.845 mm^2 including main and peak SCPAs, a four-phase signal generator, a LVDS receiver,

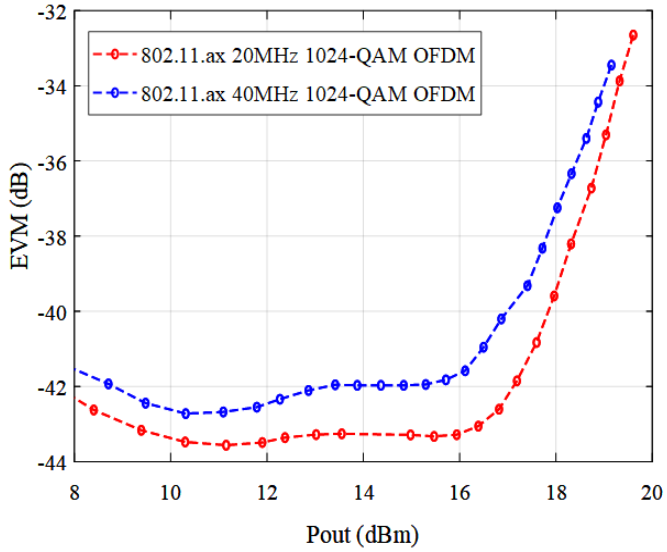

Fig. 6. EVM vs. average P_{out} for an 802.11ax 40-MHz (20-MHz) 1024-QAM OFDM signal with 13.1-dB (12.4-dB) PAPR.

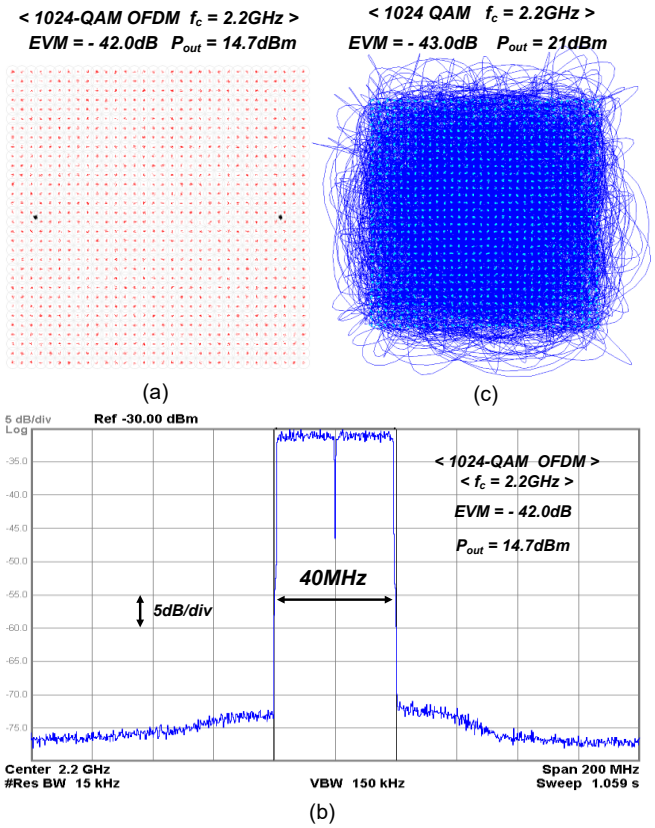

Fig. 7. (a) Constellation and (b) spectrum at average P_{out} of 14.7 dBm (after DPD) for an 802.11ax 40-MHz 1024-QAM OFDM signal with 13.1-dB PAPR. (c) Constellation with a 20-MHz single-carrier 1024-QAM signal at 6.8-dB PBO (after DPD).

a power combining transformer, and pads as shown in the chip micrograph (Fig. 5). The prototype chip is mounted, and wire bonded on PCB.

Fig. 6 shows the measured EVM of the proposed quadrature DPA with an 802.11ax 40-MHz (20-MHz) 1024-

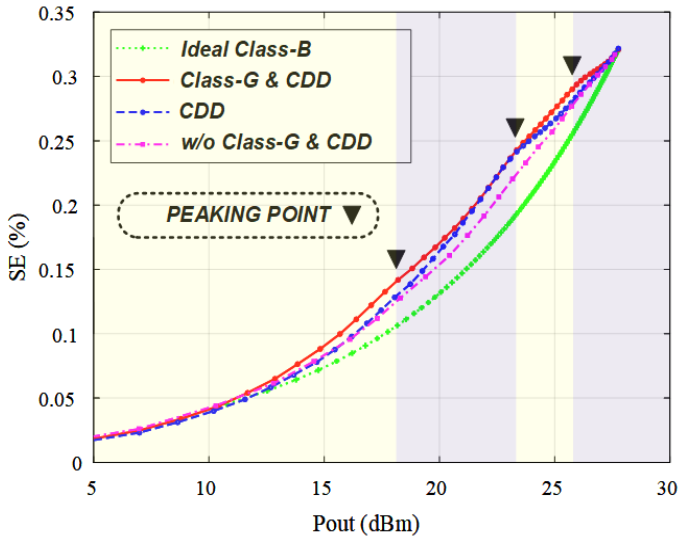

Fig. 8. SE vs. P_{out} for continuous-wave (CW) signal.

QAM OFDM signal with a 13.1-dB (12.4-dB) PAPR at 2.2GHz. The measured EVM is -42.0 dB (-43.3 dB) after digital predistortion (DPD) at 14.7-dBm (15.4-dBm) average P_{out}. The EVM floor is -42.7 dB (-43.5 dB) at an average P_{out} of 10.3 dBm (11.1 dBm), and the PA achieves EVM of <–40 dB for a more than 10-dB (12-dB) dynamic range after DPD. Fig. 7(a) and (b) depict the measured constellation and spectrum for a 40-MHz 802.11ax signal at 14.7-dBm average P_{out}. The system efficiency (SE) measured with a 20-MHz single-carrier 1024-QAM signal with 6.8-dB PAPR at 21-dBm P_{out} is 18.4%. The measured constellation is depicted in Fig. 7(c) and demonstrates –43.0-dB EVM.

Fig. 8 shows the measured SE vs. P_{out} at 2.2GHz with a continuous-wave (CW) signal. The SE of the proposed IQ-cell-shared Class-G CDD DPA clearly demonstrates multiple efficiency peaks associated with Doherty and Class-G in comparison to the ideal efficiency of Class-B PA and other operation modes with/without Doherty and/or Class-G operation. The maximum SE is 32.1% at 27.8-dBm P_{out}. Three additional peaks at 2.5-dB, 6-dB, and 12-dB PBO improve the overall efficiency. The SE depicted in this figure reflects the total power consumption in the complete quadrature transmitter chain. It is noted that the prototype quadrature DPA demonstrates a large digital power dissipation in logic circuits in a 65-nm CMOS process, which degrades the efficiency at the PBO region. However, the power dissipation in digital circuits scales down significantly in the advanced nanometer CMOS technology, and the efficiency improvement at PBO will be more noticeable in the advanced CMOS nodes. A comparison to the state-of-the-art PAs is shown in Table 1.

IV. Conclusion

A linear highly efficient transmitter based on a quadrature CDD SCPA is implemented in a 65-nm CMOS. The combination of quadrature IQ-cell-shared Class-G and CDD techniques improves the SE at the PBO region by providing multiple efficiency peaks, and the linearization techniques for unary and binary cells enhance the linearity of the quadrature DPA.

Table 1. Performance comparison with the state-of-the-art

	ISSCC 2017 [3]	JSSC 2016 [4]	RFIC 2018 [7]	**This work**
Architecture	Polar Class-G VMD	Quadrature Class-G	Quadrature Class-G	Quadrature Class-G CDD
Process	45 nm	65 nm	65 nm	65 nm
Supply	2.4/1.2V	2.4/1.2V	2.5/1.2V	2.55/1.25V
Resolution	9b (5+4)	7b (6+1)	11b (6+5)	12b (1+5+6)
frequency	3.5GHz	2GHz	2.2GHz	2.2GHz
Peak power	25.3 dBm	20.5 dBm	30.1 dBm	27.8 dBm
Peak PAE	30.4%	20%	37.0%	32.1%
Modulation	10-MHz 32-Carrier 1024 QAM	LTE 10-MHz 64 QAM	20-MHz Single-Carrier 256 QAM	20-MHz Single-Carrier 1024 QAM
Avg. power	14.8 dBm	14.5 dBm	22.5 dBm	21 dBm
PAPR	10.5 dB	6 dB**	7.6 dB	6.8 dB
System efficiency	18.0%*	12.2%	18.3%	18.4%
EVM (DPD)	-40.3 dB	-28.8 dB	-40.3 dB	-43.0 dB

* Power consumption of PA only excluding CORDIC and phase modulator
** Estimated from the peak/average power.

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