## 20.5 1.4THz, -13dBm-EIRP Frequency Multiplier Chain Using Symmetric- and Asymmetric-CV Varactors in 65nm CMOS

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THz region of electromagnetic spectrum has unique features making it attractive in spectroscopic studies, material inspection, tera-bit/sec communication, and biological- and non-biological-imaging applications. Owing to challenges in producing sufficiently strong signals, this region of spectrum has been exclusively served by III-V electronics or bulky cryogenic-temperature technologies such as QCLs [1]. Recently, advanced half-THz SiGe technologies and multi-element spatial power-combining techniques to increase the output power were successfully used to generate 0dBm of power at 0.53THz and -17dBm peak EIRP at 0.82THz [2-4]. Both solutions, however, suffer from low realized bandwidths (3%), limiting their utility in a slew of imaging and communication applications. Alternatively, high-quality accumulation-mode symmetric MOS varactors (SVARs) [5] in standard CMOS have been demonstrated as efficient odd-harmonic generators in broadband tripler and quintupler operating around 0.4THz [6] and 0.7THz [7], respectively. In this work, a 1.4THz multiplier chain of 10$^{th}$ order using MOS VARs in a 65nm standard CMOS process is demonstrated. The multiplier incorporates a new asymmetric VAR (ASVAR) for multiplication by 2 in addition to an SVAR for frequency quintupling. The circuit produces -13dBm peak EIRP at 1.33THz and operates over a setup-limited bandwidth of more than 11%. The fully integrated multiplier chain does not require any silicon lens or substrate thinning making it a compact and affordable solution for emerging THz applications.

An SVAR with adaptive CV control through n-well bias in standard CMOS process is shown in Fig. 20.5.1 [5]. It is also possible to engineer a pseudo-asymmetric CV VAR, as shown in Fig. 20.5.1, by shunt connection of two N-type MOS VARs. This asymmetry, unlike that of a single N-VAR, inhibits unwanted odd-harmonics without any degradation of desired even-order terms. In addition, by retaining the tuning range (defined as a ratio of max. to min. capacitance) of comprising VARs, an ASVAR, unlike its SVAR counterparts, does not suffer from reduction in peak realized-dynamic-cutoff frequencies ($f_{cd}$) – a figure-of-merit for reactive multipliers defined as $f_{cd}=[C_{min}^{-1}-C_{max}^{-1}]/2\pi R_s$ [5]. Therefore, ASVARs can operate at higher output frequencies.

To gauge the high frequency limit of VARs in a 65nm process, the simulated $f_{cd}$ is plotted for N-VARs with varying channel lengths ($L_g$) and widths ($W_g$). As plotted in Fig. 20.5.1, the optimum $f_{cd}$ points occur at a sub-design-rule $L_g$ of 0.1μm or below. A peak $f_{cd}$ of 3.22THz is reached with $W_g/L_g$ of 0.2μm/0.08μm. Due to higher impact of intrinsic device and interconnect parasitics at extremely scaled VARs, a relatively longer $L_g$ of 0.1μm with simulated $f_{cd}$ of 3.2THz was selected for the last stage ASVAR-based doubler (×2) stage (Fig. 20.5.2). While $W_g/L_g$ of 0.3μm/0.1μm is chosen for the SVAR ×5 stage to minimize the footprint of larger total capacitance needed to produce sufficient power at 0.7THz for driving the final doubler. P-type varactors are not supported by the foundry. The necessary P-VAR model for building SVAR is created from the process parameters. Further improvements for SVAR and ASVAR models are made with EM simulations using ANSYS HFSS.

A block diagram and schematic of the multiplier-chain are depicted in Fig. 20.5.2. At 140GHz, with 18dBm of available power to the input pad ($P_{in}$), the harmonic-load-pull simulations reveal an optimum when N- and P-VARs with 33 fingers each are used for the SVAR ×5. A simulated -3dBm power is delivered to the 1.4THz ASVAR ×2 stage when $V_{G1}/V_{NW1}$ is biased at 2.75/5.5V and $V_{G2}/V_{NW2}$ at -0.3/0V. At this power level, an ASVAR with 2 fingers each for N-VAR1/N-VAR2 delivers to the antenna an unsaturated $P_{out}$ of -21dBm in simulations with a 20dB of conversion loss (CL). Improved performance is expected with smaller-channel length and width VARs. The matching and harmonic terminations are carried out using 5μm-wide GCPW transmission-lines (TLs) realized between the ~3μm thick M10 and shunted thin metals 1 and 2. The $Z_o$ is 48Ω and the loss is 1.5dB/mm at 0.4THz. TL1 through TL9 and a 1:0.87 turn-ratio transformer formed between AL and M10 levels serve as harmonic terminations and 50Ω input match. TL10-TL12 and C3 along with the on-chip antenna array serve as harmonic terminations and output match in the ASVAR ×2 stage. The 20fF custom finger-capacitor C3 helps isolate the top plate DC-bias of SVAR from that of ASVAR and acts as a high-pass filter to minimize feed-though of the input signal at $f_0$ and its harmonics below 0.7THz. All bypass capacitors with values of 1.5-3pF are custom MOM type with an HFSS-simulated self-resonant frequency of 0.7THz. The bias resistors of 10kΩ are formed using the high-resistivity polysilicon layer. A 19kΩ shunt-resistor placed across the SVAR and ASVAR for protection against plasma-damage, increases simulated loss by 2dB at 1.4THz.

The design includes two on-chip patch antennas to radiate the THz signals (Fig. 20.5.2). The 3dB directivity boost offered by the additional element helps radiate a stronger signal and facilitates testing in the presence of high free-space propagation loss at THz frequencies. Each patch element formed with the AL layer on a ground plane made of strapped M1 to M6 metal levels is 45μm×72μm in size. The 0.5λ element-spacing (214μm) is chosen using HFSS simulations to improve spatial combining and grating lobe suppression. The array achieves a simulated peak gain of 9.7dBi and 200GHz impedance bandwidth ($|S_{11}|$<-5dB). The 3μm-wide-M10 element-feed line and notch dimensions in the patch antenna are co-optimized with the 1.4THz ×2 stage for optimum signal extraction.

Figure 20.5.3 shows the measured EIRP and radiated conversion loss, $CL_{EIRP}$ (=EIRP-$P_{in}$). The free-space test setup used for characterization of THz multiplier chain is also shown. A VDI AMC fed by an Agilent signal source is used for WR6 signal generation. This signal is then provided to the input of the CMOS multiplier chain using a GSG probe. A calibrated VDI WR0.65-band detector coupled with a horn antenna is used for collection of the radiated power from the circuit. The test setup includes a lock-in amplifier (SR810) to ensure the desired-signal reception. To mitigate spurious coupling and detector-response-time effects, a relatively low modulation frequency of 30Hz is used. A TX-to-RX separation of 1.8cm is employed to ensure far-field operation. The input power reaching the GSG pad is calibrated using a VDI PM4 meter and manufacturer-provided probe-insertion-loss data. The multiplier reaches a peak EIRP of -13dBm at 1.33THz and a minimum $CL_{EIRP}$ of 30dB (CL≈40dB excluding the simulated antenna gain). The results show a ~5% down shift in the center frequency and a ~3dB lower power than in simulations. The faster power roll-off below 1.3THz is due to bandwidth limitations of the WR6 input source. The frequency down-shift is also seen from the input $|S_{11}|$ plot (not shown). The measured-antenna-beam patterns plotted in Fig. 20.5.4 follow those of the HFSS simulations. Figure 20.5.5 shows the measured $1/R^2$ dependence, EIRP and $CL_{EIRP}$ versus input power. Figure 20.5.6 depicts a preliminary output spectrum of the circuit obtained using a Fourier-transform spectrometer (FTS) and comparison with the prior state of the art. Finally, the die micrograph is given in Fig. 20.5.7. Relative to implementations shown in Fig. 20.5.6, this work has the highest EIRP among CMOS and SiGe-HBT-based sources operating above 600GHz, highest output power above 740GHz, including those with silicon lens, and has comparable performance with the GaAs solution (Fig. 20.5.6).

*Acknowledgements:*
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*References:*

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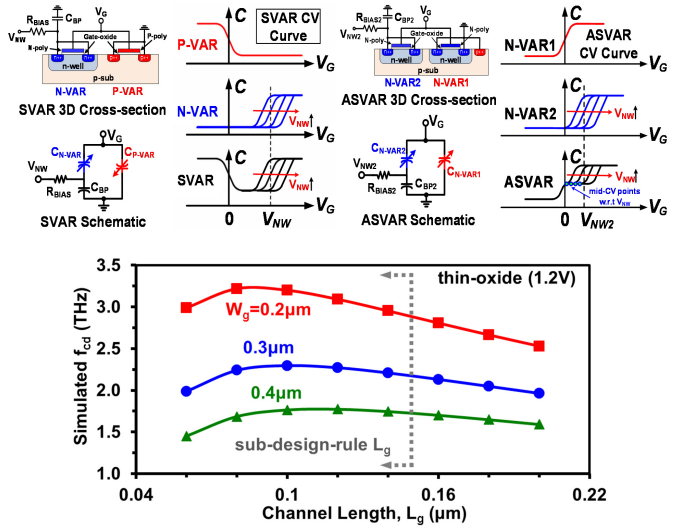



Figure 20.5.1: Symmetric- and asymmetric-MOS-varactor concept, and simulated dynamic-cut-off frequency of N-type varactors in CMOS.

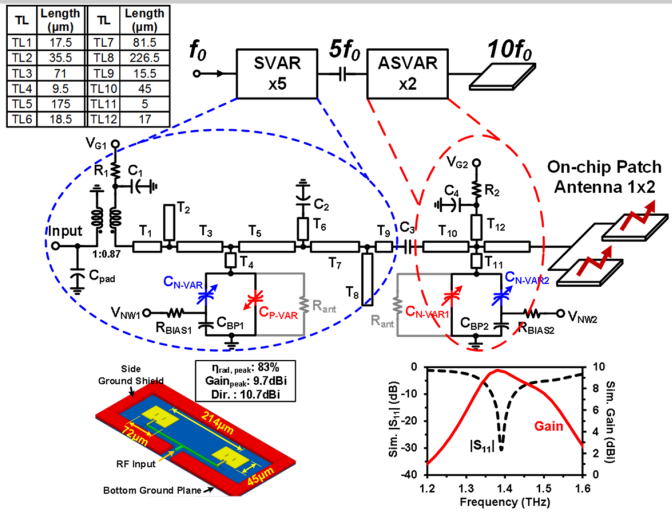



Figure 20.5.2: Block diagram and schematic of the 1.4THz multiplier chain, transmission-line lengths, on-chip antenna dimensions, and simulated $|S_{11}|$ and gain of the antenna.

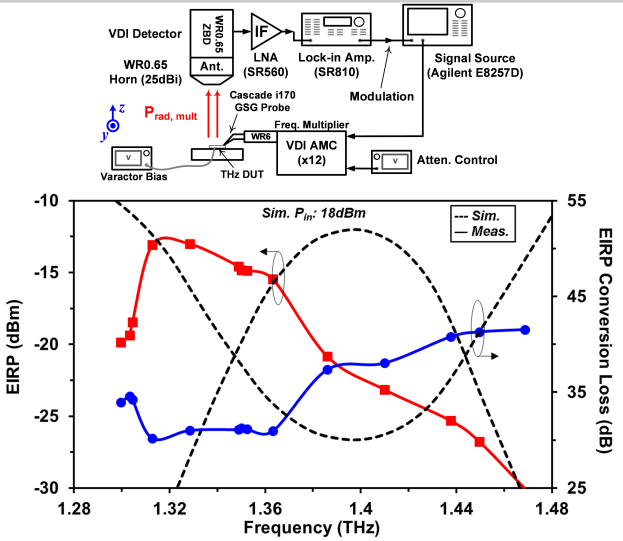



Figure 20.5.3: THz power-measurement setup and EIRP, CL performance of the multiplier chain.

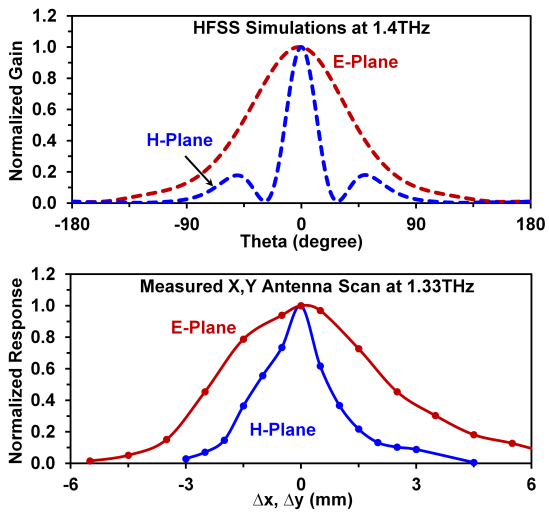



Figure 20.5.4: Simulated radiation-pattern and measured antenna scan in X, Y.

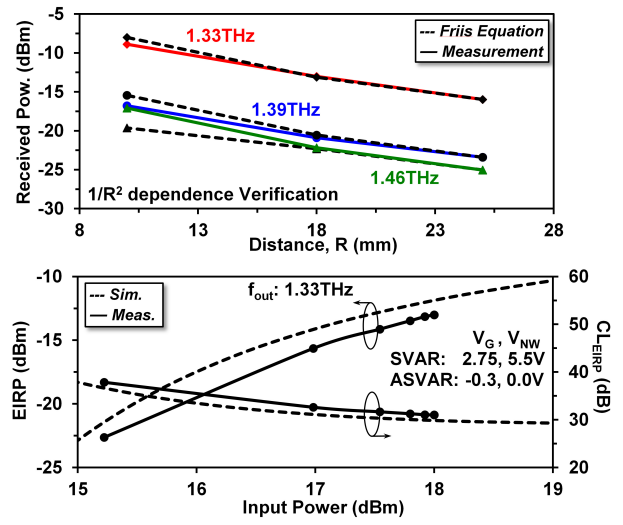
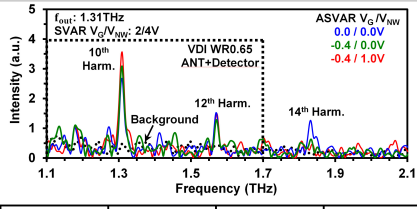



Figure 20.5.5: Measured 1/R² dependence and EIRP, $CL_{EIRP}$ over swept input power.




| Reference | This Work | VLSI2015 [7] | MTT2015 [4] | ISSCC2011 [3] | MTT2004††† |
|---|---|---|---|---|---|
| Type | MOS-VAR x10 | SVAR x5 | Active HBT x6 | Active HBT x5 | SBD x16 |
| $f_{out}$ (THz) | 1.33 | 0.72 | 0.99 | 0.823 | 1.5 |
| $EIRP_{max}$ (dBm) | -13 | -22.2 | -37 (Silicon Lens, 2 x 2 Array) | -17 (2 x 2 Array) | N/A |
| Peak $P_{out}$ (dBm) | -22.7† | -21.3† | N/A | N/A | -18.2 |
| $CL_{min}$ (dB) | 39.9† (17.1dBm) | 33.8 | N/A | N/A | 38.2 |
| **BW (GHz) | 150†† (11.3%) | 80†† (11.6%) | N/A | 25 (3%) | 170 (11.3%) |
| DC Pow. (mW) | 0 | 0 | 4000* | 3700* | N/A |
| Area (mm²) | 0.39 | 0.26 | 3.28* | 3.225* | N/A |
| Technology ($f_{max}$) | 65nm CMOS (250GHz) | 65nm CMOS (250GHz) | 0.25μm SiGe (435GHz) | 0.25μm SiGe (435GHz) | GaAs (N/A) |

†Assuming peak simulated $G_{ant}$ ††Setup limited †††G. Chattopadhyay, et al., MTT,v. 52,n. 5, pp. 1538–1547, May 04.
*Includes other circuitry **Not a 3dB bandwidth

Figure 20.5.6: Preliminary output spectrum from a Fourier transform spectrometer and comparison with prior state-of-the-art.

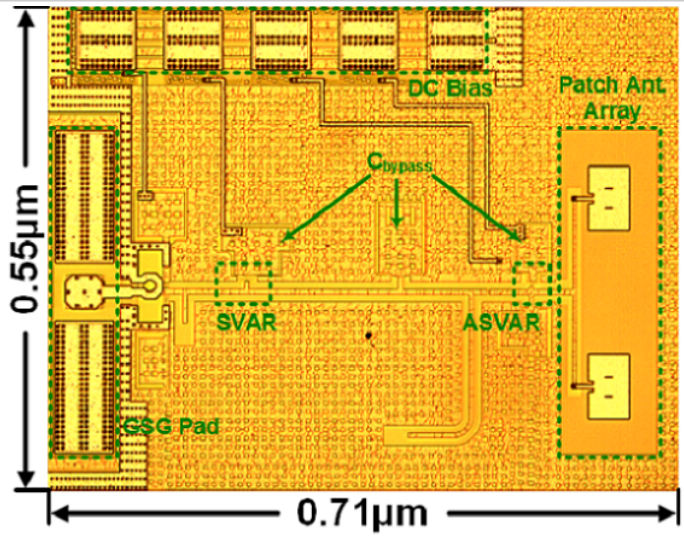



Figure 20.5.7: Die micrograph.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