# Strained Si Channel MOSFETs with Embedded Silicon Carbon Formed by Solid Phase Epitaxy

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**Abstract**

Current drive enhancement is demonstrated in sub-40 nm NFETs with strained silicon carbon (Si:C) source and drain using a novel solid-phase epitaxy (SPE) technique for the first time. The very simple process uses no recess etch or epi deposition steps, adds minimal process cost, and can be easily integrated into a standard CMOS process. With a record high 1.65 at% substitutional C concentration in source and drain, 615 MPa uniaxial tensile stress was introduced in the channel, leading to a 35% improvement in electron mobility and 6% and 15% current drive increase in sub-40 and 200 nm channel length devices respectively. (Keywords: silicon carbon, MOSFET, strained Si, mobility and solid phase epitaxy)

## Introduction

Strained Si channel has become an essential component of modern high-performance CMOS technology. Materials with same crystal structure but different lattice constants are good candidates for strain engineering. SiGe has been successfully incorporated in the source and drain of PFETs to strain the channel compressively and increase the hole mobility [1, 2]. With the lattice constant that is smaller than Si, silicon carbon alloy (Si:C) embedded in the source and drain can induce tensile strain to the channel and improve the electron mobility for NFETs. A relatively small substitutional C concentration ($[C]_{sub}$=1~2 at%) in Si is sufficient to generate a high strain level.

A straightforward approach to form embedded Si:C (e-Si:C) is to recess source and drain with an etch and then deposit Si:C using a selective epi process [3]. However, due to the extremely low solid solubility of C in Si, it is difficult to grow Si:C with $[C]_{sub}$ >1 at% selectively, and in many cases such approach can result in more than half of the total carbon content ($[C]_{tot}$) at interstitial sites [4]. Furthermore, thermal processes after the Si:C epi can easily precipitate C atoms out from the substitutional sites, causing the loss of stress and affecting the junction and transport properties.

We report a novel technique that combines carbon implant and solid-phase epitaxy (SPE) to form high quality e-Si:C in the source and drain of NFETs. Compared to the conventional recess etch-selective epi approach, the SPE method has significant advantages: 1) high substitutional C concentration can be achieved, 2) dopants in source and drain are activated during the SPE and there is no need for high-temperature process after the Si:C growth, and 3) the simple process for NFETs can readily be integrated with embedded SiGe for PFETs without adding additional masking and epi deposition steps.

## Process and Device Fabrication

As shown in Fig. 1, the process for e-Si:C device fabrication with SPE is very simple compared to the recess etch-selective epi process. Epitaxial Si:C film was formed by implanting C into an amorphized Si layer and regrowing it with SPE. HRXRD measurement (Fig. 2) and calculation with Berti and Kelires's methodology [5, 6] showed $[C]_{sub}$=1.65 at%, the highest substitutional C concentration for Si:C that is incorporated in the source and drain of NFETs to date. The well defined thickness fringes in XRD rocking curve indicate high crystal quality and smooth surface. SIMS analysis confirms that $[C]_{tot}=[C]_{sub}$ within the measurement accuracy, i.e. C is completely substitutional in the SPE Si:C film.

The device fabrication steps followed most part of an industry-standard 65 nm bulk CMOS process. C was implanted together with the source/drain doping. A protective layer was used to block carbon implant into the poly gate. Si:C SPE and doping activation were completed at one anneal. The wafers then went through standard NiSi formation and BEOL. No high temperature process was needed after Si:C SPE, so there were no C precipitation issues. The baseline control wafers went through exactly the same process as described above except the C implantation. Splits with combinations of e-Si:C and neutral liner (NL) or tensile stress liner (TL) were designed to clearly highlight the impact of e-Si:C stressor as well as to investigate the interaction between e-Si:C and stress-inducing liner.

## Results and Discussion

Fig. 3 (a) shows the cross-sectional STEM image of an NFET with e-Si:C. Convergent beam electron diffraction (CBED) technique was used to measure the stress in the channel of this device. Fig. 3 (b) shows the measured uniaxial tensile stress as a function of depth at the center of the channel. The stress increases as the location gets closer to the top surface of the channel, with the maximum stress of 615 MPa, roughly equivalent to the channel stress induced by 100 nm-thick nitride film with 2 GPa tensile stress.

The $V_t$ roll-off (Fig. 4) and $I_{off}$-$V_{tsat}$ (Fig. 5) plots indicate that the $V_t$ and short channel effects of the e-Si:C devices and the control devices are matched very well. Fig. 6 shows the $R_{on}$ vs. $L_{GATE}$ plots of the e-Si:C NFET and the control devices. The electron mobility was extracted using $\mu_n=1/[W\cdot Q_{inv}\cdot(dR_{on}/dL_{GATE})]$ [7] and the results showed a 35% $\mu_n$ enhancement for the e-Si:C NFETs compared to the control devices. However, series resistance of the e-Si:C NFET is clearly higher than the control device, and offsets the performance gain obtained from the strain effect. The series resistance increase is due to the lower doping activation in Si:C compared to that in Si, as shown by the $R_s$-$[C]_{tot}$ relationship in Fig. 7.

In spite of the higher series resistance, $I_{on}$-$I_{off}$ comparison in Fig. 8 indicates a 6% $I_{on}$ improvement due to the enhanced mobility for e-Si:C NFETs at $I_{off}$=100 nA/μm. When the e-Si:C stressor is integrated with tensile stress liner, the performance enhancements from both stress elements are retained and additive to each other. Longer channel devices are less influenced by series resistance. Fig. 9 shows the typical I-V characteristics of an e-Si:C NFET and a control device at $L_{GATE}$=200 nm with matched $V_t$. There is a 15% drive current improvement with e-Si:C NFETs.

Fig. 10 shows the reverse diode leakage current of the e-Si:C NMOS devices compared to the typical leakage obtained without incorporating e-Si:C. There is some increase in the junction leakage but the increase is within an acceptable range that can be optimized with junction design.

With the implantation-SPE process for e-Si:C, a lithography step can be easily added to block C implant in PFETs. For certain PFETs, we intentionally integrated e-Si:C in the source and drain to monitor the effect of tensile strain as the hole mobility is expected to decrease with the uniaxial tensile strain. The $R_{on}$-$L_{GATE}$ plots (Fig. 11) shows a 60% hole mobility degradation, confirming the successful introduction of tensile strain by e-Si:C.

## Conclusion

Embedded Si:C in source and drain was formed for the first time by very simple implantation and SPE regrowth process to enhance NFET performance. Tensile stress of 615 MPa was generated in the channel with a record high 1.65 at.% substitutional C concentration in the source and drain regions, resulting in 35% electron mobility improvement and 6% and 15% drive current improvement for sub-40 and 200 nm channel length NFETs, respectively.

## References

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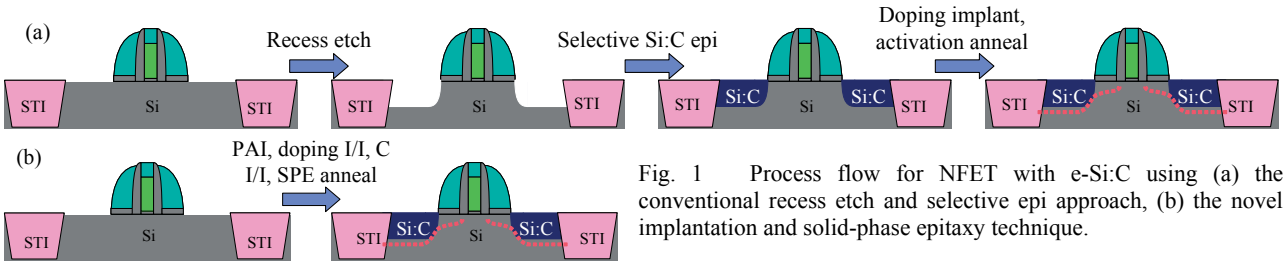


Fig. 1 Process flow for NFET with e-Si:C using (a) the conventional recess etch and selective epi approach, (b) the novel implantation and solid-phase epitaxy technique.

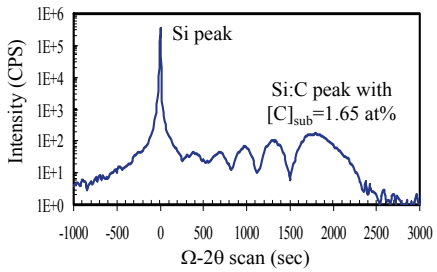


Fig. 2 HRXRD rocking curve of the SPE Si:C film ($[C]_{sub}$=1.65 at.%) grown on (100) Si substrate. The well defined Si:C peak and fringes indicate that the Si:C film is high-quality single crystal.

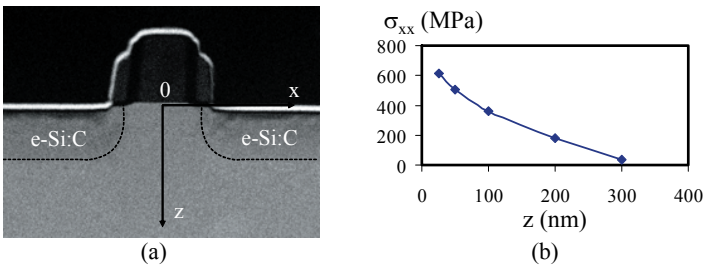


Fig. 3 (a) Cross-sectional STEM image of an NFET with e-Si:C before silicidation. (b) The uniaxial tensile stress ($\sigma_{xx}$) measured by CBED as a function of depth ($z$) at the center of the channel (x=0). The stress at z=25 nm is 615MPa.

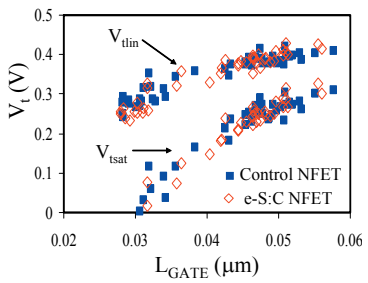


Fig. 4 NFET $V_t$ as a function of gate length. The e-Si:C devices match with the control devices very well.

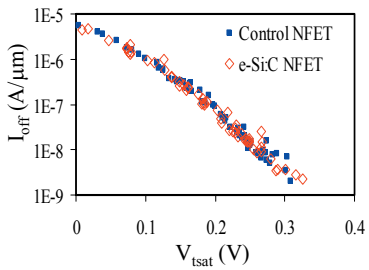


Fig. 5 NFET $I_{off}$ as a function of saturation threshold voltage.

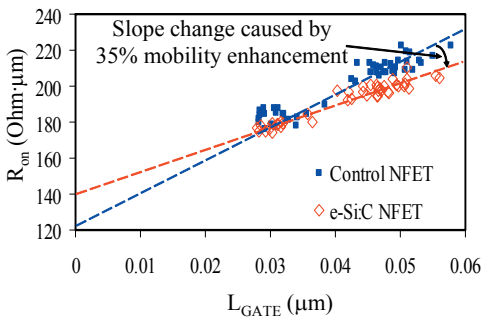


Fig. 6 NFET resistance as a function of gate length showing a 35% electron mobility improvement but higher series resistance with e-Si:C.

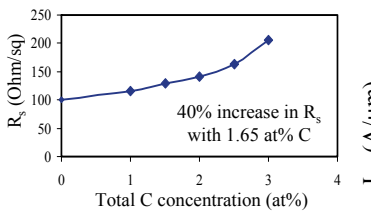


Fig. 7 Sheet resistance of As doped SPE Si:C as a function of total C content. The As activation is degraded as more C is implanted.

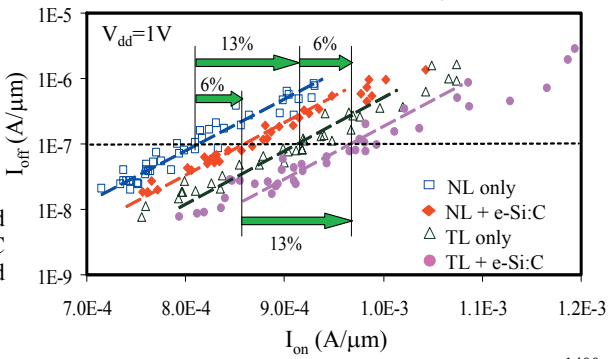


Fig. 8 $I_{on}$-$I_{off}$ performance comparison for NFETs with different stress elements (NL: neutral liner, TL: tensile liner). Drive current is improved by 6% due to the e-Si:C tensile stressor. When e-Si:C is integrated with TL, both the improvement by e-Si:C (6%) and the improvement by TL (13%) are retained and they are additive to each other.

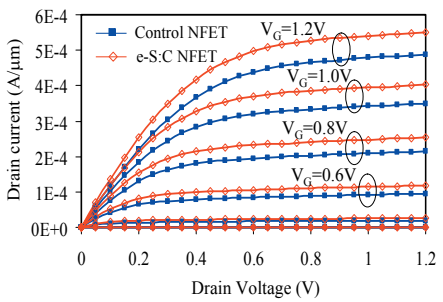


Fig. 9 Typical I-V characteristics for NFETs with $L_{GATE}$=0.2 μm. The drive current (at $V_D$=$V_G$=1V) of e-Si:C NFET is 15% higher than the control device with matched $V_t$.

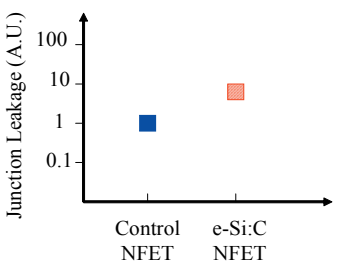


Fig. 10 NFET junction leakage comparison between e-Si:C and control devices. There is a slight leakage increase due to e-Si:C but it is within the acceptable range.

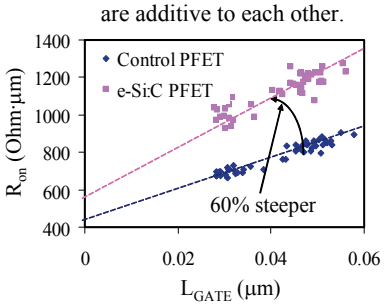


Fig. 11 $R_{on}$ vs $L_{GATE}$ plots for PFETs. Si:C was incorporated in the source and drain of certain PFET devices. The 60% slope increase due to $\mu_p$ reduction as expected confirms the tensile strain induced by e-Si:C.