Built-in Self Testing of a DRP-Based GSM Transmitter

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***Abstract*— We present a novel approach for built-in self-testing (BIST) of an RF wireless transmitter. This approach, based on fully-digital hardware and on software algorithms, allows the testing of the transmitter's analog/RF circuitry while providing low-cost replacements for the costly traditional RF tests. The testing approach is structural in nature and substitutes for the commonly employed RF performance testing of high-cost test equipment and extended test times. The test coverage achieved for the analog circuitry is maximized to approach 100% and the test-time and associated test costs are minimized. The presented techniques have been successfully verified in a commercial 90 nm CMOS single-chip GSM radio based on the Digital RF Processor (DRP^{TM}) technology.**

I. Introduction

As the market continuously drives price reduction of mobile phones and their components, it becomes increasingly important to reduce *all* costs associated with the fabrication of a cellular handset's transceiver SoC. This includes the costs of final testing at production, which is expected to constitute only a limited percentage of the total production cost. Additionally, high production yields are expected, in order to maintain profitability, thus inhibiting the use of simplified overly-strict tests that would intolerably impact the yield. Furthermore, increasingly small percentages of shipped defective devices are being required by customers (given in unites of DPPM, for defective parts per million), such that the test coverage and reliability expected from semiconductor manufacturers are demanding as well. Consequently, new testing environments and techniques are sought for that would allow all these conflicting goals to be met simultaneously. This paper presents a novel approach in *design-for-testing* (DfT) applied in a Digital RF Processor (DRP^{TM})-based GSM SoC for that purpose. This approach is demonstrated here through two examples of testing mechanisms that were successfully implemented in the transceiver and are in use in the mass-production of the Texas Instruments GSM single-chip radio [1] [2] fabricated in 90 nm CMOS.

This paper is organized as follows: Section II provides background and cites previous work targeting RF/analog BIST, Section III presents the proposed approach of this work, with two subsections providing details for two different examples demonstrating this approach. Analysis and measured results are provided for both examples. The Conclusion section summarizes the presented work and discusses future extensions of it.

II. Background and Previous Work

For many years, the semiconductor industry has been benefiting from automated means for inserting testing circuitry into *digital* designs and calculating its coverage. The scan chains used for this purpose provide structural testing, which typically targets the detection of silicon defects through symptoms such as "stuck at 0/1", rather than functionally testing the circuitry. Contrarily, in analog/RF designs, the structural approach is not as prevalent and is not built into the most commonly used analog CAD tools. Radio transceivers have traditionally been designed in "analog friendly" fabrication processes, such as SiGe, with their production testing typically being based on high-cost testers having RF capabilities both for stimuli and for measurements. The recent SoC trend, forcing transceiver implementations to adapt to digital design and fabrication environments, has also created the need and the opportunity for lower cost testing techniques for the transceiver, which approach those of the structural nature used for the greater digital portion of the SoC.

The research presented here focuses on a GSM frequency synthesizer, which provides for RF carrier generation and modulation in the transmitter [1] and for RF down conversion in the receiver [2]. It is an extension of the work presented in [3] [4] [5] and in [6], where the first BIST implementation based on all-digital hardware for an ADPLL was presented in the context of a DRP-based Bluetooth transceiver. Since the implementation of the ADPLL is, by definition, digital, the hooks for its BIST are digital as well and were designed in the same VHDL design environment. Contrarily, prior reports demonstrate dedicated designs of BIST circuitry targeting PLL circuits, involving additional analog circuitry and various compromises in terms of implementation and coverage [7]. An on-chip jitter analyzer for a PLL is described in [8], which consumes large additional area.

The prior publications [3] [4] on this subject have been focused solely on ADPLL BIST as means for parametric characterization of key RF performance. This may be useful in screening devices failing specifications not necessarily due to manufacturing defects but also due to design marginalities. The quantitative analysis and proof of concept presented there focused on the absolute correlation between performance measured externally and the internal (BIST) estimations. Reference [3] is similar in focus to [4] but adds more qualitative analysis of the phase error signal PHE (or ϕ_E) and analytically explains

how the PHE signal can be used for measurement of absolute RF performance.

III. The Proposed Testing Approach

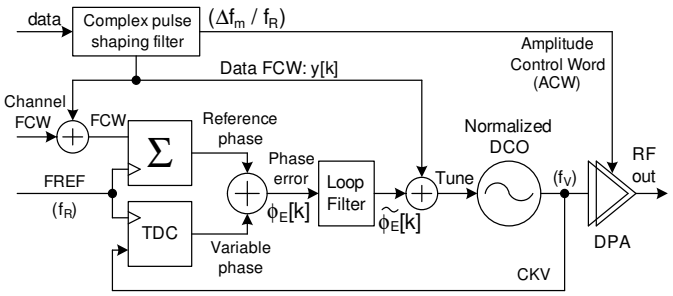

Fig. 1. ADPLL-based polar transmitter for wireless applications.

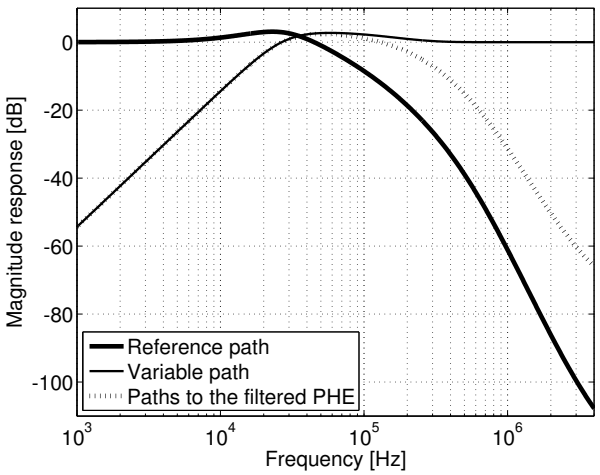

Fig. 2. ADPLL closed-loop transfer function for the reference (normalized by N) and variable paths with the default loop setting. The settings establish the closed-loop bandwidth of about 40 kHz and provide 33 dB of attenuation of the FREF phase noise and TDC quantization noise at 400 kHz offset. The type-II setting provides 40 dB/dec filtering of the DCO 1/f noise.

The approach presented in this paper, tailored for final testing at production, is structural in nature and does not attempt to directly assess the parametric performance committed in the transceiver's specifications, but rather verifies that its elements do not suffer fabrication defects that would result in incompliance and increased DPPM.

The ADPLL BIST mechanisms, presented here as examples for this approach, target two different entities of analog nature. The first example is a BIST for the oscillator noise, which is useful not only for the detection of fabrication defects that result in degraded noise performance in the digitally controlled oscillator (DCO), but can also serve for various other purposes including oscillator bias calibration. The second example is a BIST for the frequency tuning varactors in the DCO, which is also useful for *design-for-characterization* (DfC), as it is a convenient means for investigating mismatches between these nominally identical MOS elements [9].

A. DCO Phase Noise BIST

The noise performance of the oscillator is critical for the GSM transmitter to meet its phase-trajectory error (PTE) specifications for the GMSK modulation and its error vector magnitude (EVM) specifications for the EDGE modulation. Although controlled digitally by the ADPLL, the DCO is an RF circuit and occupies a large area on the die, which may be prone to defects. These facts combined make it critical to detect defects resulting in intolerably degraded DCO phase noise performance. Software-based variance estimation of the digital PHE signal within the ADPLL serves for this purpose.

As shown in Fig. 1, the PHE signal $\phi_E[k]$ is the digital output of the phase detector and is numerically the difference between the reference and variable phase [3]. This digital signal is internal to the ADPLL and hence providing it for BIST purposes does not require overhead in terms of circuit design. The digital nature of the PHE signal allows the on-chip processor to directly sample and process it seamlessly.

Fig. 2 shows the magnitude response of the filtered PHE with respect to the reference (i.e., 26 MHz crystal resonator) and variable (i.e., DCO) paths. The transfer function of interest relates to that of the variable phase, which is band-pass in nature [3]. The plots illustrate the impact of the phase noise signals from the crystal reference and from the DCO on PHE. The type-II loop setting suppresses the close-in 1/f noise of the DCO while the IIR filters shape the spectrum at offsets higher than the loop bandwidth. As evident from Fig. 2, PHE will be insensitive to noise dominant at frequency offsets less than 1 kHz due to the type-II loop configuration. PHE will also be insensitive to noise at frequency offsets greater than 100 kHz due to the noise shaping of the IIR filters. But as shown in Fig. 3, the DCO phase noise degradation suffered due to a defect covers a wide range of frequency offsets from the carrier. This includes the offsets of 10 kHz to 100 kHz to which the PHE is most sensitive. Hence, it is possible to detect DCO defects resulting in noise performance degradation using PHE. The reference phase noise does not dominate over the DCO phase noise at PHE, such that the DCO phase noise estimation remains feasible in this BIST.

Fig. 3 shows measured RF carrier spectra of a defective and a nominal DCO. The degradation in phase noise in the defective device is shown to be wide. When GMSK modulation was applied, the defective device was over 2^o higher in phase trajectory error (PTE) than the nominal device. Additionally, the degradation in the GMSK modulated spectrum at a 400 kHz offset was about 15 dB.

Fig. 4 compares the DCO performance of four different devices and establishes the DCO phase noise relationship with RMS phase error, which is measured at the RF output and estimated with PHE. These results are compared with simulations based on the model described in [3], which predicts the impact of phase noise on PTE very accurately. The internal BIST estimation is also shown to correlate well with the external PTE measurement based on standard RF equipment. Notice that the results in Fig. 4 are relative rather than absolute,

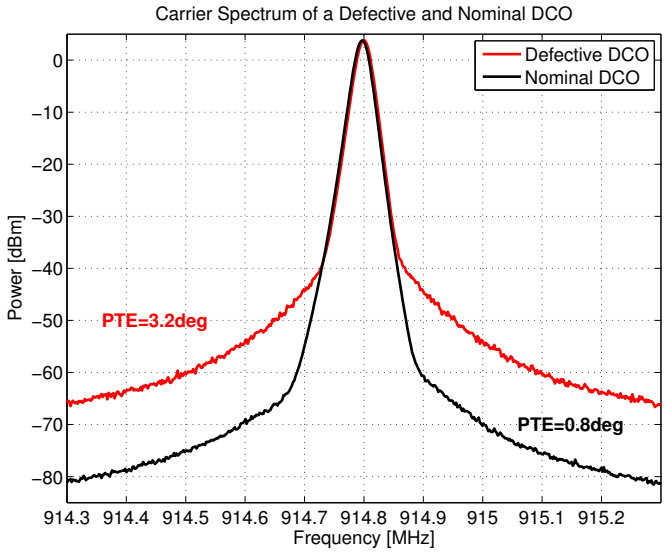

Fig. 3. Carrier spectrum of a nominal and a defective DCO with phase trajectory error measurement quoted when GMSK modulation was applied.

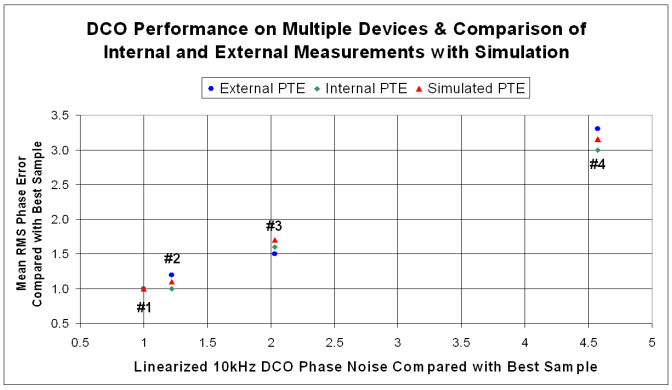

Fig. 4. RMS phase error vs. 10 kHz DCO phase noise on various devices. Noise level results are normalized to the best sample which is sample #1 in the plot.

i.e., all measurements are normalized to the best measured sample. It makes sense in defect-oriented testing (DOT) to use a standard reference in order to establish meaningful limits for device screening that are often not directly derived from its parametric performance specifications. In this case, limits should be established to screen out sample #4, which is considered defective.

B. DCO Capacitor Bank BIST

The DCO tracking bank [1] consists of digitally biased varactors that are responsible for the fine frequency tracking and modulation performed in the ADPLL. The MOS varactors comprising it are nominally of identical capacitances [9] and can create frequency steps of about 15 kHz in a high-band RF signal in the 1.8 GHz frequency band. The finer frequency steps required by the DCO tracking and modulation are obtained through high-rate $\Sigma\Delta$ dithering [1]. The purpose of the BIST presented in this subsection is to verify that each of the 128 settings of this bank is operational and provides the expected frequency step (i.e., is not shorted, disconnected, or out of range, as a result of a fault). The BIST is based on scanning through the entire bank of varactors and testing each one of them at a time. The test for each one is based on the ability to address it directly using the 7-bit control word of this bank, and the ability to detect the effect of this by monitoring the phase error signal PHE, or ϕ_E, within the ADPLL (see Fig. 1). Since the frequency step for each of the tested capacitances is relatively low and the PHE signal is contaminated with noise, as shown in [4], the signal corresponding to the activation or deactivation of a single varactor is too noisy for the detection of it to be sufficiently accurate. Extending the duration of the frequency step cannot serve for the purpose of increasing the corresponding energy in the PHE signal and improving the signal-to-noise ratio, since the closed loop operation will cancel the effect of this frequency step within a duration corresponding to the loop bandwidth. This is also evident from the transfer function for the filtered PHE signal versus the variable-phase of the DCO, which is shown to be of band-pass characteristics in Fig. 2.

The BIST is therefore designed such that it periodically toggles the tested capacitance at a rate that allows the accumulation of detected energy at the output of the phase detector, thereby allowing the measurement to be sufficiently reliable for the purpose of testing. For the sake of test time minimization, the number of such periods to be used for the testing of each capacitance could not be made arbitrarily high and the toggling frequency and number of periods was chosen such that the accumulation would produce a sufficiently high signal-to-noise ratio within a reasonable period of time. The minimal signal-to-noise ratio had to ensure that the natural probability for an erroneous decision in the test result, as a result of the additive noise, would not adversely impact the DPPM.

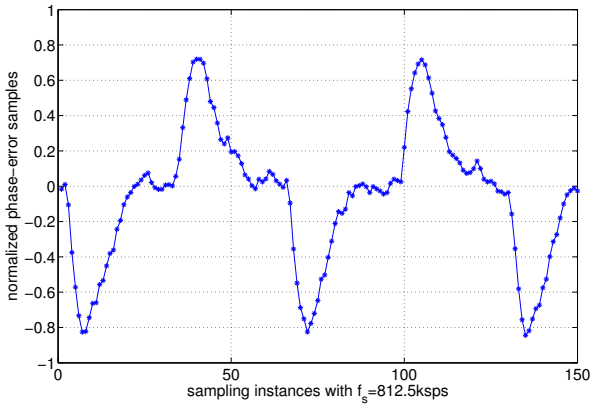

Fig. 5. Digitally captured periodic waveform of the PHE signal during the testing of one of the tracking bank varactors.

Fig. 5 shows samples representing about 2.5 periods of the signal created at PHE as a result of the frequency perturbations caused by the toggling of a tested capacitance at a rate of about

TABLE I

NORMALIZED CAPACITANCE ESTIMATED BY RF BIST.

cap.#	1	2	3	4	5	6	7	8
norm cap.	1.00	0.98	0.95	0.93	0.98	0.92	0.97	0.97
range [%]	9.1	5.6	8.7	7.4	12.4	5.1	5.3	6.1
ext. meas.	1.00	1.01	0.97	0.96	1.01	0.94	0.96	0.99

12.7 kHz. This rate and a few of its harmonics have reasonable gain according to the transfer function denoted "Paths to the filtered PHE" in Fig. 2. The energy in this signal is accumulated by using an approximate matched filter in software, such that a quantitative result is obtained which corresponds to the tested capacitance. Table I lists the normalized results measured for the first 8 capacitors in a specific device over 10 consecutive runs. The PHE signal energy accumulated for each of the 8 varactors over 16 periods of its on/off toggling was compared to that of the first one (which is why the first value in the first row of the table is 1). The normalized values reflect very low mismatch between capacitances, but the normalized range of results for the 10 consecutive runs of the BIST routine is shown to be as high as 12.4% in one case, which represents over 6% of measurement error around the average value. Depending on the test requirements, this range may be tightened by increasing the number of toggling periods used while paying the penalty of increased test time. The test time represented in this example is at least 1.3 ms per tested varactor (to complete 16 periods at 12.7 kHz and additional computation time). For an array of 128 settings, this will add up to about 0.17 seconds. The third row in the table represents a normalized external measurement obtained at the transmitter's RF output and is shown to be in agreement with the BIST results to within several percents.

The test limits for this BIST, to be used for the screening of faulty devices at final testing, are chosen based on the following assumptions: (1) A disconnect in the control for a specific varactor or a defect in the varactor itself would result in considerably lower capacitance. (2) A short between two control lines of two separate varactors would considerably increase the amount of detected capacitance. (3) Small deviations in the capacitance from its nominal value (e.g., 10%) have insignificant impact on the ADPLL performance due to its employment of dynamic element matching (DEM) [1], and therefore do not need to be detected by the BIST.

The PHE signal energy detected for the first capacitor in the array is tested against relatively lenient test limits, which are derived from the natural distribution of the capacitance over process (over 30% of variance, which is anyway internally calibrated for in the ADPLL). The rest of the capacitances are normalized against the first value and are expected to be within the mismatch error from it, which is a narrower range. A device under test is failed if any of its tested capacitances is found to exceed the predefined limits allowed for it, and this indication is conveyed from the internal processor to the tester via a digital interface. Since the capacitances and their control are verified at the nodes in which they are used during normal operation (semi-functional test), the coverage offered by this scanning BIST is 100%. This is contrary to indirect structural approaches, where the tested elements are tested with dedicated stimuli that is injected through some analog mux, and/or when tested using a measurement that does not depend on their true impact in the circuit of interest, as discussed in [7]. This is because a fault that is beyond the node where multiplexing takes place may not be detected by such test.

IV. CONCLUSION

We have presented a structural testing approach and demonstrated two derived practical examples of defect-oriented built-in self-test (BIST) mechanisms for RF circuitry in the GSM local oscillator and transmitter. The internal estimations achieved with the BIST mechanisms are shown to be in agreement with external measurements and simulated models and effectively serve to substitute for traditional performance tests based on external RF measurements. The test times associated with these BIST routines are low and they are shown to effectively cover the elements they are targeting. The presented approach for analog/RF circuitry is extendable into other blocks of the DRP as well, thus further reducing the need for external tests and reducing test costs for the cellular transceiver SoC.

V. ACKNOWLEDGMENT

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