8.7 A 20mW 61dB SNDR (60MHz BW) 1b 3rd-Order Continuous-Time Delta-Sigma Modulator Clocked at 6GHz in 45nm CMOS

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Continuous-Time ΔΣ Modulators are a popular architecture choice for ADCs in deep-submicron processes [1-4]. The maximum sampling rate is set by Excess Loop Delay (ELD) considerations. ELD comprises the comparator latency, feedback DAC delay (DEM delay etc.) and any additional delay due to parasitics. For a wideband 1b modulator clocking at high speeds (multi-GHz), the key challenge is modulator stability due to large ELD set by comparator speed limitations and integrator parasitic poles. This paper describes circuit techniques to minimize ELD and a compensation scheme that ensures modulator stability given a 1-clock-period ELD. These techniques have enabled the design of a 3rd-order 1b modulator clocked at 6GHz in 45nm CMOS.

Traditional techniques for ELD compensation use a DAC in a fast feedback loop around the comparator such that the comparator's decision is fed back in time for the next sample. The delay due to parasitic poles makes this scheme infeasible in scenarios where 1-clock ELD is required. A recent approach [5] allows for ELD between 1-to-2 clock cycles but results in a noise penalty on account of a zero in the Noise Transfer Function (NTF). Our technique compensates for 1-clock ELD in the presence of parasitic poles without incurring such a noise penalty.

Figure 8.7.1 shows the system block diagram of the ADC with the ELD compensation scheme. The approach replaces the innermost feedback DAC (I_4) with a transconductor whose inputs track the output of the 2nd latch as shown in Fig. 8.7.1. The current feedback begins at half a clock delay from the sampling instant and continues as the 2nd latch amplifies the decision of the 1st latch to full digital levels. The circuit in Fig. 8.7.2 shows the feedback path through the cascode of the 1st comparator's pre-amplifier. The input differential pair (M_a/M_b) is designed to fully switch the feedback current I_4 with a differential signal >100mV. If the output at the end of the 1st latch's regeneration is >100mV, I_4 is fully switched and full ELD compensation results. If not, during the track period, the 2nd latch gains up the output and there is a high probability that I_4 is fully switched before the next sampling event ensuring stability. However, if the output of the 2nd latch doesn't reach digital levels at the end of 1 clock period, the DFF in Fig. 8.7.1 enters a metastable state with the result that DACs $I_1 - I_3$ can switch differently from I_4. However, the inner feedback does not always have to match the outer feedback. The difference between the digital output to the I_1-I_3 feedbacks and the I_4 feedback due to metastability is noise-shaped and system simulations indicate a minimal impact on SNR.

The ADC loop filter is implemented as a combination of active and passive integrators [6] as shown in Fig. 8.7.1. The first integrator is passive (R_1C_1) and is followed by two active Gm-C integrators. Feed-forward paths are used to minimize the signal swings within the loop to improve ADC linearity [6]. The feedback DACs ($I_1 - I_3$) are current-steering 1b Return-to-Zero (RZ) DACs. The innermost loop for ELD compensation (I_4) is implemented in an RZ fashion as well, with the reset happening during the hold phase of the T/H. FIR filters are employed in the feedback path to minimize the impact of timing jitter [7] with a 4-tap FIR filter chosen for this design.

The circuit schematic of the comparator is shown in Fig. 8.7.2. The comparator consists of a pre-amplification stage (M_1-M_4 and R_1-R_2) and a positive feedback cross-coupled pair M_5/M_6. The load resistor is split between R_1 and R_4 based on an optimization between pre-amplifier gain, bandwidth, latch regeneration gain and time constant. Resistors R_3/R_4 isolate the cross-coupled pair from the parasitic capacitances of the pre-amplifier and the subsequent comparator stage. When CLK goes low, the input is amplified while simultaneously the latch is reset to reduce hysteresis. The resistors R_1-R_4 along with the reset switches are sized to maximize the pre-amplifier gain and bandwidth while minimizing residual memory on the cross-coupled pair. When CLK goes high, the comparator enters regeneration. The 2nd comparator stage (slave stage) is identical to the 1st comparator and works on the opposite clock polarity.

Figure 8.7.3 shows the circuit schematic of the Gm cells along with the feed-forward paths. The feed-forward approach is described in [6]. The Gm cells need high gain, low noise, good linearity and low excess delay. Without circuit modifications, a conventional Gm stage cannot meet these performance requirements especially given the constraint that the excess delay caused by parasitic poles needs to be significantly smaller than the clock period. The main parasitic pole is at g_{mc}/C_P where g_{mc} is the transconductance of the cascode devices M_3/M_4 and C_P is the capacitance at its source. Our approach adds a feed-forward capacitance C_{FF} that introduces a LHP zero at g_{mc}/C_{FF}. Furthermore, it also modifies the inherent parasitic pole location from g_{mc}/C_P to $g_{mc}/(C_P+C_{FF})$. Choosing C_{FF} such that $C_{FF}>>C_P$ results in a pole-zero cancellation. The RHP zero due to the gate-drain overlap capacitance of the input pair is neutralized by the neutralization capacitor C_N. The combination of feed-forward and neutralization techniques results in the Gm cell having an excess delay significantly less than a clock period (equivalently a 40GHz pole). This aids in overall system stability and allows for an aggressive NTF without additional power consumption. The Gm cell's power consumption is now set solely from thermal noise and linearity considerations.

The feedback DACs (I_1-I_3), shown in Fig. 8.7.1, are implemented as 1b PMOS current-steering DACs. The main DAC element works off a 1.8V supply and is a cascoded current source with its headroom maximized to minimize noise. Choice of devices and biasing ensures that the devices are in their safe operating zones at all times negating any reliability concerns. The DAC inputs are driven by D-Flip Flops (DFF) that latch the output of the comparator. A chain of 4 DFFs each driving 4 equal units of the feedback current ($0.25*I_1$) implement a 4-tap FIR filter ($[1+z^{-1}+z^{-2}+z^{-3}]/4$). The output of the first DFF is also fed back to DACs $I_2 - I_3$.

Figure 8.7.4 plots the ADC's measured output FFT for a sinusoidal input -3dB below Full Scale (FS) at 10MHz (0dBFS is $2V_{pp}$ input differential). The measured SNDR in a 60MHz BW is 60.6dB and the SFDR is 75dBc. A plot of the SNR/SNDR vs. input signal amplitude is shown in Fig. 8.7.5. Based on a 2-tone test (-9dBFS at 5MHz/50MHz such that the inter-modulation components are at band edge), the IIP3 and IIP2 are measured to be +36dBm and +61dBm respectively. Figure 8.7.7 shows a die micrograph of the ADC. The ADC occupies an area of $0.49mm^2$. The ADC operates off of 1.8V for the feedback DACs, 1.4V for the analog supply and 1.4V for the digital supply. The ADC power consumption (excluding decimation filters) is 20mW for an FoM of 190fJ/conv-step. Table 1 compares the ADC with the state-of-the art designs [1-4]. Compared with [2-3], the ADC has 3× the BW with comparable FoM, while in comparison to [1] the FoM is 3.7× lower.

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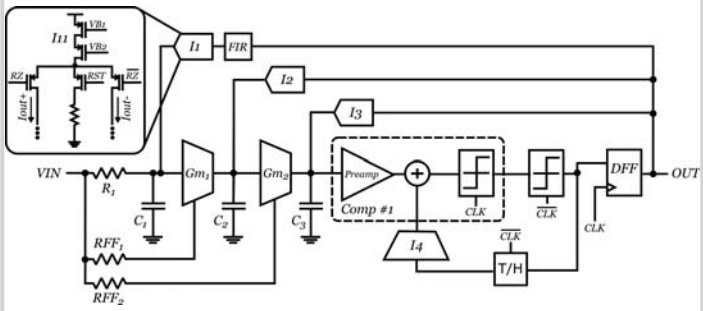

Figure 8.7.1: Block diagram representation of the ADC architecture.

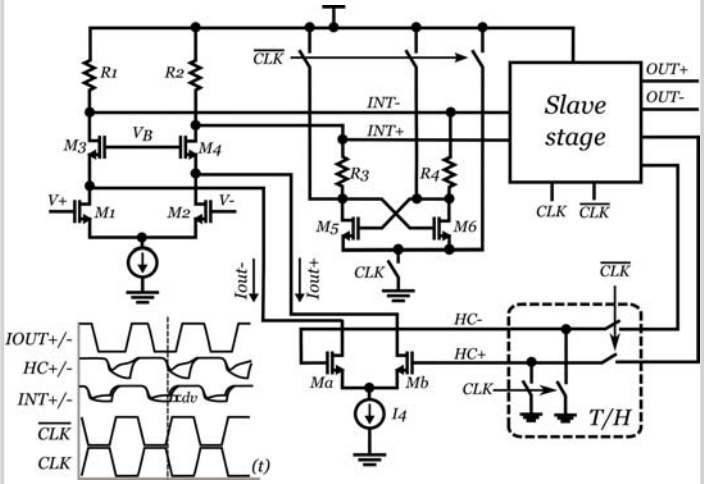

Figure 8.7.2: Circuit schematic of the comparator module along with the ELD compensation scheme and timing diagram with representative waveforms at key nodes.

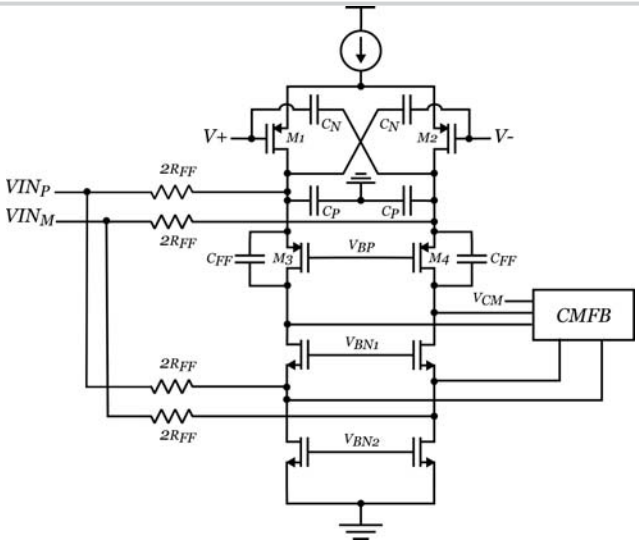

Figure 8.7.3: Circuit schematic of the Gm cell showing the feed-forward and neutralization capacitors and the feed-forward paths.

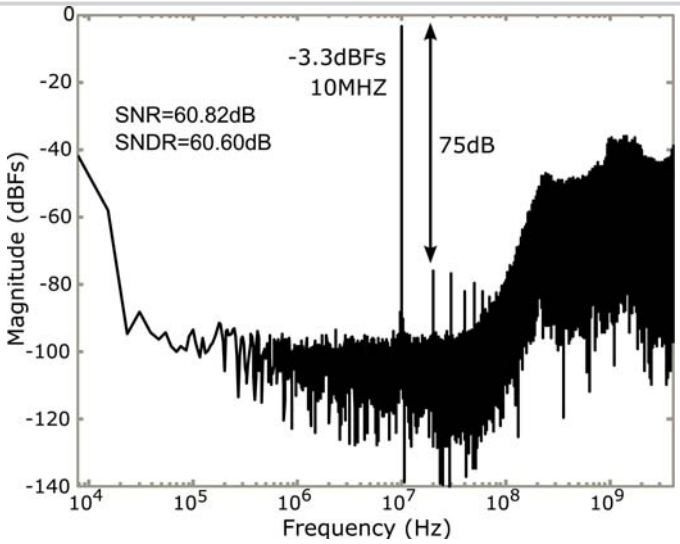

Figure 8.7.4: Measured FFT of the ADC's 1b output showing a SNDR of 60.6dB in 60MHz BW with an SFDR of 75dBc for a -3dBFS input signal at 10MHz.

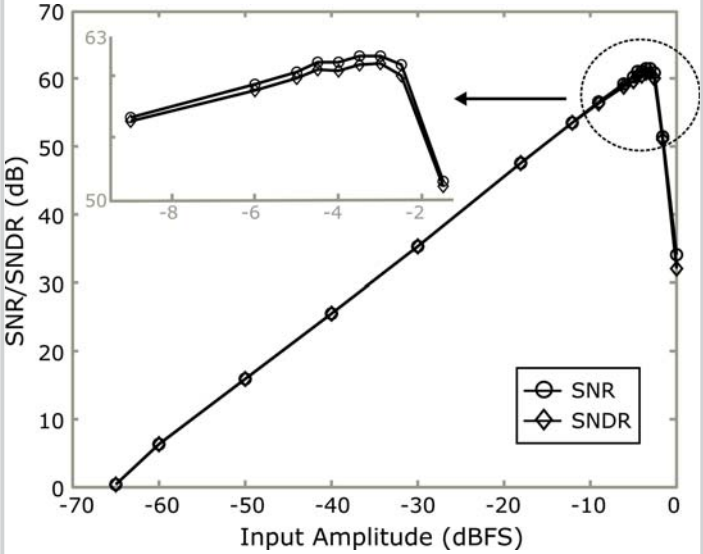

Figure 8.7.5: Plot of SNR/SNDR vs. Input Signal Amplitude.

	This work	[1]	[2]	[3]	[4]
Architecture	ΔΣ	ΔΣ	ΔΣ	ΔΣ	ΔΣ
Fs	6GHz	4GHz	640MHz	900MHz	640MHz
BW	60MHz	125MHz	20MHz	20MHz	20MHz
SNR	61.5dB	65.5dB	76dB	81.2dB	N/A
SNDR	60.6dB	65dB	74dB	78.1dB	56dB
Power	20mW	256mW	20mW	87mW	8.5mW
Area	0.49mm^2	0.9mm^2	8.6mm^2	0.45mm^2	0.4mm^2
FOM	0.19pJ/ Conv-step	0.7pJ/ Conv-step	0.12pJ/ Conv-step	0.33pJ/ Conv-step	0.41pJ/ Conv-step
Technology	45nm CMOS	45nm CMOS	130nm CMOS	130nm CMOS	90nm CMOS

Figure 8.7.6: Performance summary of the ADC and comparison to prior art where FoM = Power/((2$^{(SNDR-1.76)/6.02)}$*2*BW).

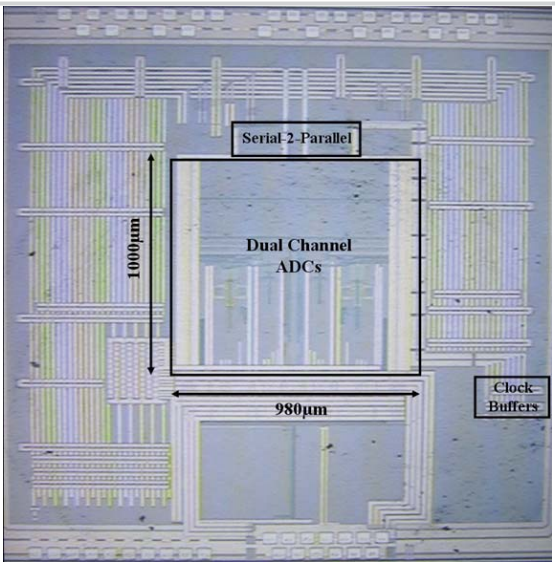

Figure 8.7.7: Die photograph of the prototype ADC.

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