A 16-Element Phased-Array CMOS Transmitter with Variable Gain Controlled Linear Power Amplifier for 5G New Radio

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***Abstract*—This paper presents a 28-GHz 16-element phased-array transmitter for the fifth-generation (5G) new radio (NR) applications, focusing on the power amplifier (PA). The IC was fabricated using a 28-nm bulk CMOS technology with a flip-chip package, and evaluated with 5G NR signal having an 800-MHz total bandwidth. Each channel of the 16 phased-array transmitter has a 16 dBm output at 1-dB compression point and a large gain range from 24 to 63 dB. The full 16-element array achieves an average output power of 18 dBm with a record-level system error vector magnitude (EVM) of less than -33.5 dB (<2.1%) at a total power consumption of 1.63 W (102 mW of per channel) including all biases, digital control, and power-management-unit (PMU) blocks, over the frequency band from 26.5 to 29.5 GHz.**

***Keywords*— 28GHz, 5G, beamforming, mm-wave, phased array, transceiver, transmitter.**

I. Introduction

Increasing demands for high data rate systems are driving the development of the fifth generation (5G) wireless systems with data rates on the order of more than 1-10Gb/s. To accomplish the demands/needs, 5G communications will be deployed at millimeter-wave (mm-wave) bands such as 28 and 39 GHz.

Recent works have demonstrated mm-wave transceiver ICs supporting switching or combining among three 4-channel sub-array groups in 28nm bulk CMOS [1], direct conversion transceiver at 28GHz [2], phased arrays for picocells in SiGe [3], and transceiver ICs with RF interfaces for large-scale arrays in SiGe [4]-[5]. This work presents the 16-element phased-array transmitter that significantly improves the power consumption as well as the linearity in the full-array operation. It also increases transmit (TX) output power per channel element compared to the recently reported solutions.

5G systems are based on orthogonal frequency-division multiplexing (OFDM), which adds more challenges to the power amplifier (PA) design due to its high peak-to-average power ratio (PAPR) of 10-dB and wide bandwidth around 1 GHz. When the PA operates with the wide bandwidth signal, the second order nonlinearity at the envelope frequency can be particularly problematic due to the large fractional bandwidth [6]-[8]. The PA mixes up the envelope with the amplified fundamental component, which is called memory effect. In Section III-(a), a PA structure is proposed to relieve the memory effect by isolating the V_{DD} path between the final- and other-stages. A large dynamic gain range is implemented in TX and the PA is responsible for a large portion of the gain ranges. It has an advantage in noise figure (NF) for operation with a wide bandwidth signal, that will be described in Section III-(b). In Section IV, the measurement results will be shown.

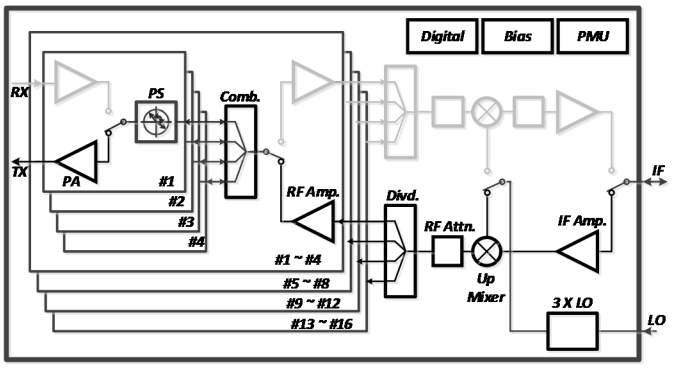

Fig. 1. A simplified block diagram of developed 5G transceiver with 16-element array

II. Transmitter Architecture

Fig. 1 shows the proposed architecture of the 16-element phased-array transceiver. In this work, we focus on the design of the TX path and its performance. The input frequency is from 10.36 to 12.04 GHz, and the transmitter converts it to an output RF frequency from 26.5 to 29.5 GHz. The TX path has a large dynamic gain range from 24 to 63 dB with a 1-dB gain step. A 1-dB step attenuator is proposed at the input matching of the PA. The PA can cover the 18 dB gain range and the rest of the gain ranges are provided by the TX intermediate frequency (IF) amplifier and RF attenuator. The TX IF amplifier has NF of less than 4.5 dB at the maximum gain-mode and covers 9 dB gain range with a 3 dB gain-step using the current control method by turning off a common-gate (CG) transistor. The RF step attenuator between the up-mixer and the combiner provides low insertion loss as well as high linearity. It has a gain range of 12 dB with a 3 dB gain-step. The 4-bit passive phase shifter is used in each channel and it has an insertion loss of less than 7.3 dB for all the phase controls. The PA which is a key block of the TX path, is composed of four amplifier stages. Both good linearity and high efficiency are achieved by the proposed PA structure with the even harmonic control method, which will be explained in Section III-(a).

III. Design of Power Amplifier

A. Structure of 4-Stage Power Amplifier

The PA in each channel is composed of four stages as shown in Fig. 2. In general, the final-stage of a PA has a deep class-AB topology to get a high efficiency but it generates large 2nd order intermodulation (IM2) components at the 2nd harmonic and envelope frequencies. The 2nd harmonic termination circuits can eliminate the mixed 3rd order intermodulation

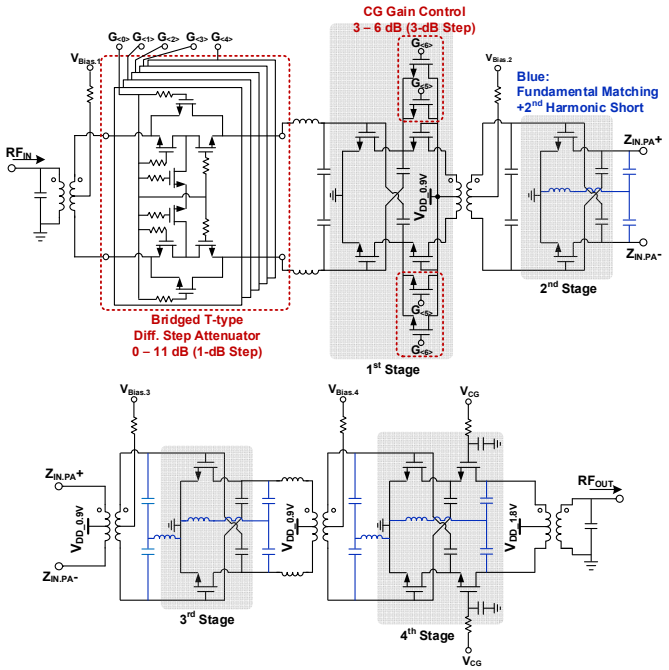

Fig. 2. A schematic of the proposed 4-stage PA in each channel.

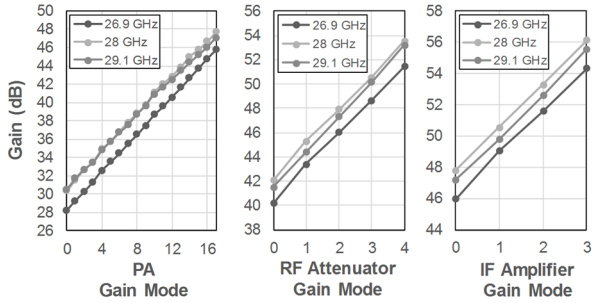

Fig. 3. Measured gain of each TX block according to gain-mode control. When the gain of one block is controlled, other block's gain-mode is fixed.

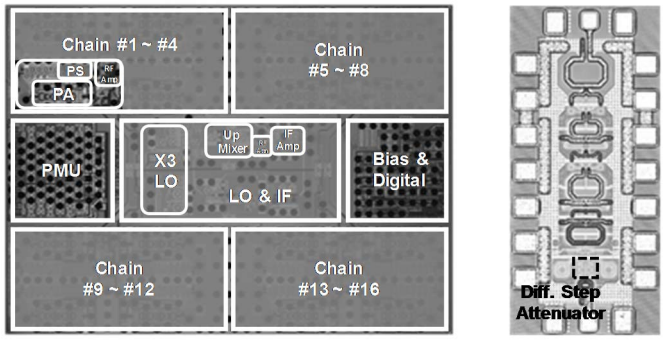

Fig. 4. (a) Die photograph of the 16-element phased array transceiver and (b) IP block of standalone PA for on-wafer probing in a 28-nm bulk CMOS process.

distortions (IMD3s) generated by mixing of the fundamental and 2nd harmonic [6]. However, this circuit does not always ensure the enhanced linearity over a wide bandwidth since the IMD3s are also generated by mixing of the fundamental and envelope nonlinear terms. When the impedance at the envelope frequency is not small enough, the asymmetric IM3 is generated by the memory effect [7]. A severe issue occurs when the envelope nonlinear components from the final-stage feedback to the 1st/2nd/3rd-stages through the V_{DD} path. It not only generates the large mixed IMD3 terms at all the stages but also amplifies the nonlinear components sequentially passing through each stage of the amplifier. Therefore, the linearity is significantly deteriorated. To lessen this problem, the impedance of the V_{DD} network at the envelope frequency should be minimized to near to short. For the 5G system, the low impedance conditions should be retained up to 1 GHz to cover the wide bandwidth of the signal. However, it is difficult to realize this condition by using on-chip passive devices. As one of the solutions for this issue, the on-chip low-drop out (LDO) for the PA is presented in [8], but it is not efficient in terms of the power consumption and size. Especially, the implementation of both the multi-array of the PAs and the LDOs on the chip are a burden. In this work, the stacked amplifier is adopted only for the final-stage and the separated drain-voltage supplies between the final- and other-stages are proposed. The V_{DD} of 0.9V is applied for the 1st/2nd/3rd-stages and the 1.8 V is supplied for the final-stage. This structure can isolate the final-stage from the other-stages at the envelope frequency. The 1st/2nd/3rd-stages have a near class-A biasing compared with the final-stage and their sizes of the transistors are small. Therefore, the IM2 components generated by the 1st/2nd/3rd-stages are relatively small and hardly affect the linearity. The V_{DD} of 1.8V domain that is only for the final-stage can be easily managed at the package side. It is terminated by the off-chip capacitors on the module-package. The dominant IM2s generated by the final-stage are supressed by the 2nd harmonic termination circuit and the separated V_{DD} path isolates the envelope components from the final stage to the 1st/2nd/3rd/-stages. This architecture has advantages in the linearity as well as the efficiency. A stacked structure enhances the gain of the final-stage compared with the common-source (CS), improving the power-added efficiency (PAE) [6]. It is also a suitable structure to obtain a large output power.

B. Large Dynamic Gain Range

The variable-gain control plays a fundamental role in optimizing the system capacity. The transmitter gain should be adjusted so that proper power is received at each terminal. In the 5G system, the signal has a wide bandwidth that expands up to ~1 GHz, so the signal-to-noise ratio (SNR) at a given signal power level is lower than that in the 4G system. For that reason, NF is also an important factor even in TX mode. The first block in a system usually has the most significant impact on the total NF because the effective NFs of the following stages are reduced by the stage gains. Consequently, the NF requirements of the subsequent stages are usually more relaxed. Therefore, when the transmitter operates as a low-gain-mode, the gain should be reduced by the final-block of the TX, preferentially.

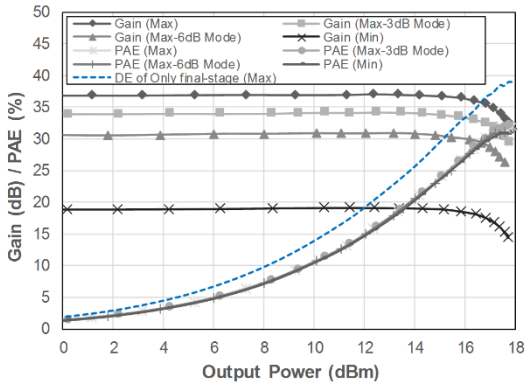

Fig. 5. Measured PAE and gain of the standalone PA for the variable gain mode with a CW signal at 28 GHz.

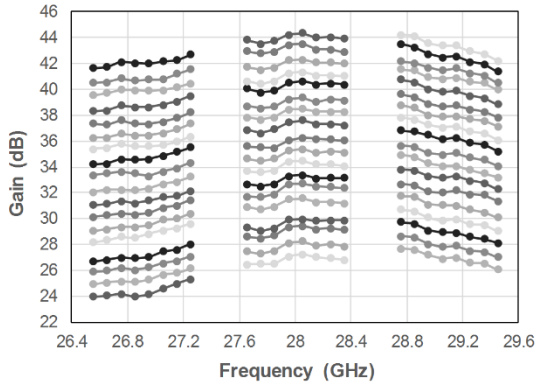

Fig. 6. Measured gain step and flatness response of the transmitter, across the frequency range from 26.5 to 29.5 GHz with the 8CC aggregated signal.

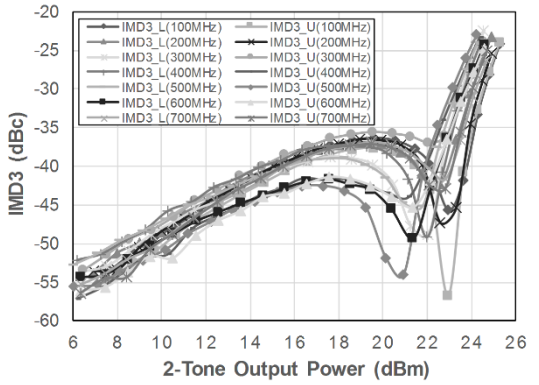

Fig. 7. Measured IMD3 of the fully operated 16-array transmitter for the 2-tone signal with a various tone-spacings at 28 GHz.

In the proposed transmitter, the PA which is a final block of the TX path has a gain range of 18 dB with a 1-dB gain-control step. A 1-dB gain step is provided by proposed differential step attenuator at the input of the first-stage, as shown in Fig. 2. It is a bridged T-type attenuator and each required resistance is realized by a parasitic R_{on} of the corresponding transistor. The R_{on} of a transistor has better tolerance than the poly resistor for the process variation. The step attenuator is merged into the input matching network and has a compact layout area. It has a sufficient linearity to drive the PA for all gain-modes. A 3-dB gain step is implemented by turning off the CG transistor at the first-stage. The combination of the attenuator and CG control

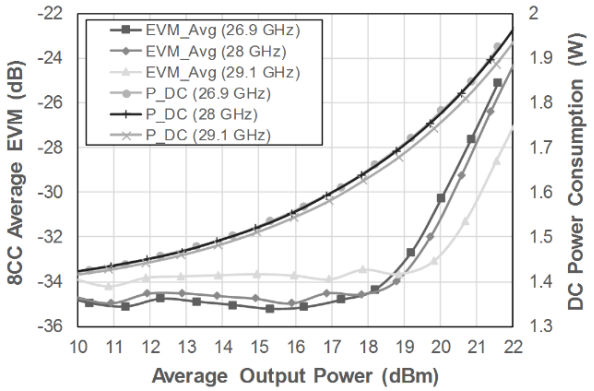

Fig. 8. Measured EVM and consuming DC power of the fully operated 16-array transmitter for the 8CC 5G NR signal at center frequency of 26.9, 28, and 29.1 GHz, respectively.

can cover the 18 dB gain range. A few gain steps in the PA can be used for channel power equalization in the multi-array system. The IF amplifier and the RF attenuator have 9 dB and 12 dB gain ranges, respectively, with a 3 dB gain-steps. Fig. 3 shows the measured TX gain for the 5G signal having an 800 MHz bandwidth, according to the gain control of each block. As a result, a large dynamic gain range from 24 to 63 dB is implemented in the TX.

IV. Implementation and Measurement

The proposed transceiver was fabricated using a 28-nm bulk CMOS technology with a flip-chip package, and the total chip area is 4.7*6.4mm^2 as shown in Fig. 4(a). First, to validate the performance of the standalone PA, the intellectual property (IP) block of the PA shown in Fig. 4(b) is measured using on-wafer probing. Fig. 5 shows a PAE, a drain-efficiency (DE), and a power gain for a continuous waveform (CW) signal at 28 GHz. The 4-stage PA in the maximum gain-mode delivers a gain of 37 dB, a saturated output power of 18 dBm with PAE of 32%, and an output 1-dB compression point (OP_{1dB}) of 16 dBm with PAE of 29%.

The full 16-element operation of the transmitter with a supply voltage of 1.8V is measured by the conduction test using a 16-way combiner on an in-house test board. The one carrier component (CC) of the new radio (NR) signal has 64 quadrature-amplitude-modulation (QAM), 10 dB PAPR, and 100 MHz bandwidth. Eight CCs are aggregated and used for the test. The IF input frequency is two times of the local oscillation (LO) frequency and the RF frequency of the transmitter output is five times of the LO frequency in this system. Fig.6 shows the gain step and the flatness response of the transmitter for the 8CC NR signal. Only a partial gain range is plotted due to both the noise and the maximum driving power limitation of the measurement instruments. The proposed transmitter achieves a good IMD3 performance for the various tone-spacings as shown in Fig. 7. The IMD3s are maintained under -35 dBc up to a 2-tone output power of 22 dBm and a large asymmetry is not observed thanks to the proposed PA structure. Consequently, the proposed transmitter achieves an average error vector magnitude (EVM) of under -33.5 dB (<2.1%) for

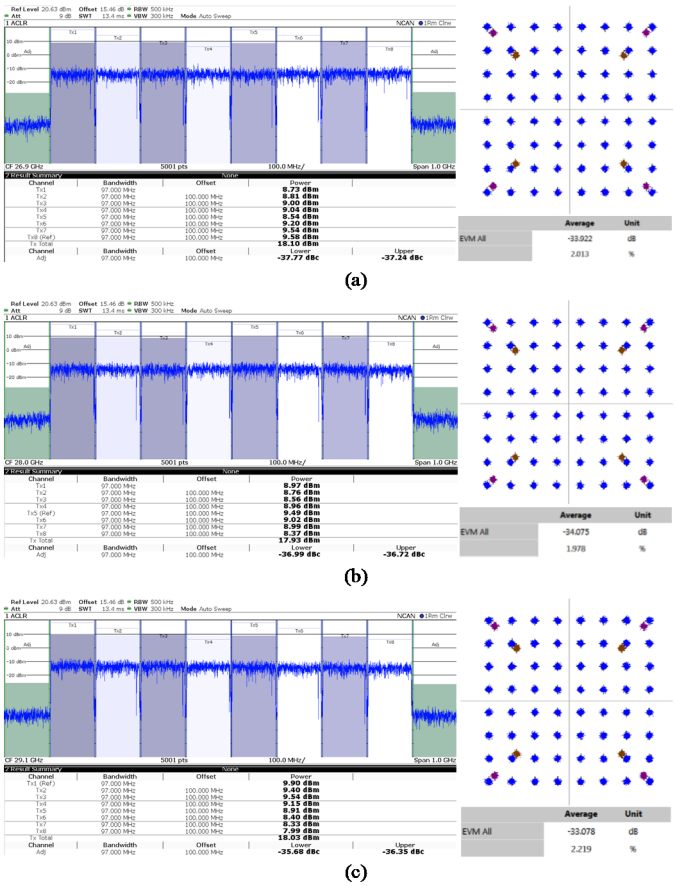

Fig. 9. Measured 5G 8CC NR spectra and EVM in TX mode at an average output power of 18 dBm. (a) A 1st CC EVM of -33.9 dB at 26.9 GHz, (b) a 4th CC EVM of -34 dB at 28 GHz, (c) and an 8th CC EVM of -33 dB at 29.1 GHz.

the 8CC and the total power consumption of 1.63 W (102 mW/channel) including all bias, digital control, and power-management-unit (PMU) blocks, at an average output power of 18 dBm across the 26.9 to 29.1 GHz. These data are shown in Fig. 8. The measured spectra of 5G NR 8CC and EVM constellations are depicted in Fig. 9. Table 1 summarizes the comparison of the measured results with state-of-the-art 28 GHz phased-array transceivers having at least 4 channels. This work delivers higher OP_{1dB} and superior EVM performance in comparison with those of the state-of-the-art transceivers in TX mode. It consumes 102 mW/channel.

V. Conclusions

A 28-GHz 16-element phased-array transceiver for 5G applications is presented, focusing on the transmitter with the PA. In the design of the PA, a stacked amplifier is adopted only for the final-stage and the separated drain-voltage domain between the final- and other-stages is proposed. This architecture provides advantages for both the linearity and the efficiency. A large dynamic gain range from 24 to 63 dB is implemented in TX. The PA is responsible for a large portion of the gain ranges and it provides merits in NF for a wide bandwidth signal operation. The transceiver was fabricated using 28-nm bulk CMOS technology with flip-chip. For the 8CC of NR signal having 64QAM, 10 dB PAPR, and 800 MHz bandwidth, it achieves superior EVM of under -33.5 dB (<2.1%) and total power consumption of 1.63 W (102 mW/channel) at an average output power of 18 dBm.

Table 1. Performance summary compared with state of the art 28 GHz phased-array transceivers in TX mode.

Parameter	**This Work**		ISSCC18 [1]	JSSC18 [2]	JSSC17 [3]	JSSC18 [4]
Technology	28nm RF CMOS		28nm LP RF CMOS	28nm RF CMOS	0.13um SiGe BiCMOS	0.18um SiGe BiCMOS
Front end channels per IC	16		24	8	32	4
TX Input / RX Output Interface	11.2 GHz IF		6.5 GHz IF	Analog IQ BB	3 GHz IF	RF
Measured RF Frequency	26.5 - 29.5 GHz		27.5 - 28.5 GHz	25.8 - 28 GHz	27.5 - 28.5 GHz	28 - 29 GHz
Signal & Bandwidth (BW)	5G NR OFDM 64QAM **10 dB PAPR 800 MHz BW**	5G NR OFDM 64QAM **10 dB PAPR 100 MHz BW**	OFDM 64QAM - 400 MHz BW	LTE 64QAM 7.5 dB PAPR 20 MHz BW	-	-
Phase Shifter Resolution	4 bit		3 bit	3 bit	5 bit	6 bit
TX Gain (dB)	**24-63**		34-44	48	17-47	-2 to 12
PA Psat (dBm)	**>17.5**		>14	10.5	16	12.5
PA OP1dB (dBm)	**>16**		>12	9.5	13.5	10.5
PA 64QAM PAE	**7.2% (@6 dBm) 9.2% (@9.2 dBm)**		7.5% (@6 dBm)	3.0%	-	-
TX Total Power (W)	1.63 (16xCH) @Pout 18 dBm		0.36 (4xCH)	0.416 (4xCH)	4.6 (32xCH)	0.8
TX OFDM 64QAM Pout/Channel (dBm)	6	6	6	3	-	2.5
TX OFDM 64QAM EVM (dB)	**<-33.5**	**<-34.5**	<-27*	-	-	-
**TX efficiency per Channel (@EVM -27 dB)	**7.2% (@9.2 dBm)**	**8.2% (@9.9 dBm)**	4.4% (@6 dBm)	-	-	-

*Graphically estimated
**TX efficiency is shown at EVM -27 dB to compare the efficiency with [1]

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