

# A 28 GHz Sub-harmonic Mixer Using LO Doubler in 0.18- $\mu\text{m}$ CMOS Technology

Tsung-Yu Yang, and Hwann-Kaeo Chiou  
Dept. of Electrical Engineering  
National Central University, Jhongli, Taiwan, R.O.C.

**Abstract** — A 28 GHz sub-harmonically pumped passive down conversion mixer fabricated in a 0.18- $\mu\text{m}$  CMOS process is demonstrated. A low power fully differential LO frequency doubler is designed to generate at near half RF frequency. The proposed sub-harmonically pumped passive mixer has advantages in low power consumption, high fundamental frequency suppression, and suitable apply to millimeter-wave frequencies. At 28 GHz RF frequency and 13.2 GHz LO frequency, the measured conversion loss of the mixer is less than 11 dB, single side band noise figure of 11.6 dB, the isolations among LO, IF and RF are over 33 dB, and a third-order intercept point at the input of 8 dBm, while dissipating total current of 0.6 mA from 1 V supply. To the authors' knowledge, the design achieves the highest figure of merit among published down-conversion mixers operating at similar millimeter-wave frequencies in comparable silicon based technology.

**Index Terms**— CMOS, sub-harmonic mixer, millimeter-wave frequencies, monolithic microwave integrated circuit (MMIC).

## I. INTRODUCTION

Recently, down-conversion mixers have been presented in 0.18- $\mu\text{m}$  CMOS technology showing the superior RF performance up to millimeter-wave frequencies. These circuits are, for instance, a 24 GHz front-end [1], a 3-22 GHz distributed single-balanced mixer [2], a 0.3-25 GHz ultra-wideband Gilbert-cell Mixer [3]. However, the CMOS technology has lower  $f_t$  and larger parasitic capacitance makes mixer hard to deliver high conversion gain and linearity under low power consumption in the high frequencies. Much higher linearity can be achieved with passive mixer using the nonlinear variation characteristics for millimeter-wave frequencies. Due to the passive character, mixer has the relative conversion loss. However, the saved dc power can be used for a drive amplifier in front of the mixer.

Furthermore the large local oscillator power was also difficult to achieve out of a CMOS device, thus a sub-harmonically pumped passive mixer (SHM) is commonly used. The SHM has been exhibited the high linearity, low dc power dissipation, and high isolation between LO, RF and IF ports. But the use of CMOS for SHM at mm-wave range has not been extensively investigated and a high performance CMOS SHM for applications above 20 GHz

has not been reported to date. This work demonstrates a 28 GHz SHM with a differential LO frequency doubler implemented in a standard 0.18- $\mu\text{m}$  CMOS technology and the circuit is well suited for the local multipoint distribution service application.

## I. MIXER DESIGN

Figure 2 shows the schematic of the sub-harmonic mixer with the LO frequency doubler circuit. Transistor M5 is taken as a single ended drain mixer where the RF signal is inputted at the gate and LO signal with a  $2f_{LO}$  frequency is injected at the drain. A high Q microstrip transmission line serves as impedance matching for the RF passband. Since the higher loss properties caused by poor substrate isolation of CMOS technology, this transmission line with metal shielding is applied to improve this drawback. The transmission line is realized using the top metal (metal 6) as the signal and the bottom metal (metal 1) as the ground. The NP-MOS LO frequency doubler (M1~M4) is adopted to generate the even order harmonics for the sub-harmonic LO operation. The differential input LO signals are fed into the gate of transistors, which are biased near the class-B region to generate the second harmonic. A diplexer is designed for the separation of the LO and IF signals at the drain port of M5 which suppress the fundamental and odd order harmonics in the node A. And the output IF signal is then taken from the diplexer.

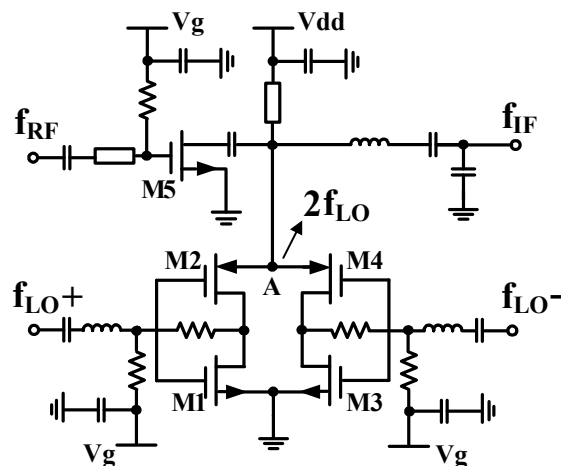


Fig. 1. Schematic of the sub-harmonic mixer circuit

### III. EXPERIMENTAL RESULTS

The photograph of the fabricated 28 GHz sub-harmonic mixer is shown in Fig. 2 and compact chip size is 0.45 mm x 0.67 mm. The fabricated SHM was measured using an on wafer probing system. An RF input signal at 28 GHz was generated by connecting an Anritsu 37397B Vector Network Analyzer and the LO signal at 13.25 GHz generated by Agilent E8254A signal generator. The output signal was detected by an Agilent E4446A spectrum analyzer.

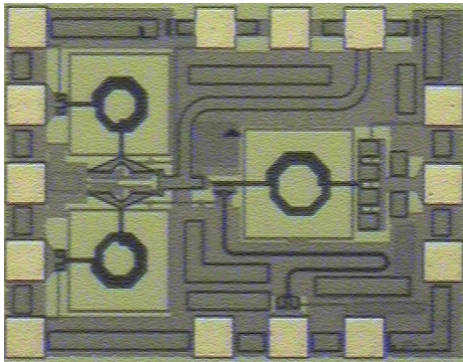


Fig. 2. Photograph of the fabricated 28 GHz sub-harmonic mixer

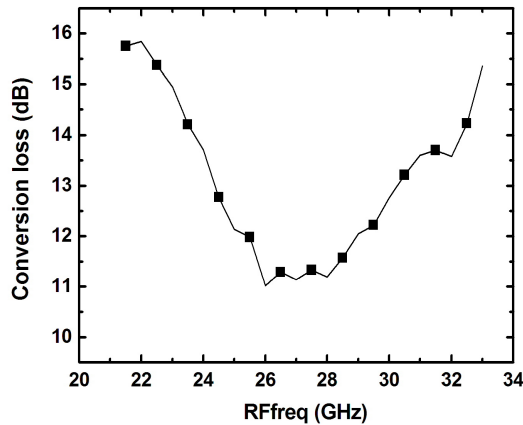


Fig. 3 Measured the Conversion loss vs. RF frequency

In Fig. 3, the conversion loss is measured at a fixed 1.5 GHz IF frequency under the 13 dBm LO drives. The obtained conversion loss is less than 13 dB within an RF bandwidth from 24 to 30 GHz.

The measured noise figure is less than 12 dB from RF 25 to 29 GHz as shown in Fig. 4. Fig. 5 illustrates the measured isolations and the 2LO-to-IF and LO-to-IF isolations exceed 60 dB and 40 dB as the LO frequency varies from 10 to 16 GHz. The measured LO-to-RF isolation also well agrees with the simulation and is better than 32 dB for the LO signal. Fig. 6 shows the measured output power of input power for the mixer at 28 GHz. The observed input 1-dB compression point is -2.7 dBm under the 13 dBm LO drive. Table I presents a summary of the mixer characteristics. The simulated and measured results are matched very well.

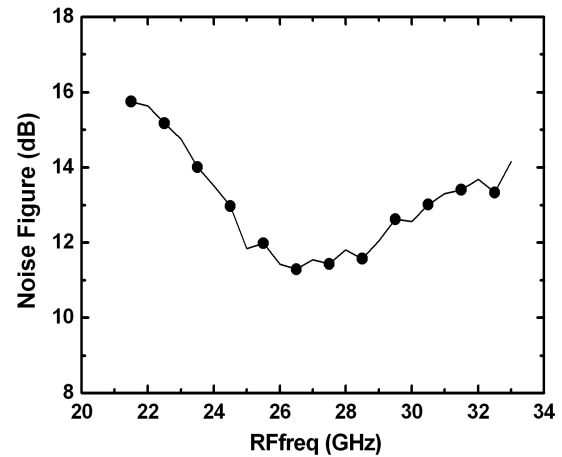


Fig. 4. Measured the Noise Figure vs. RF frequency

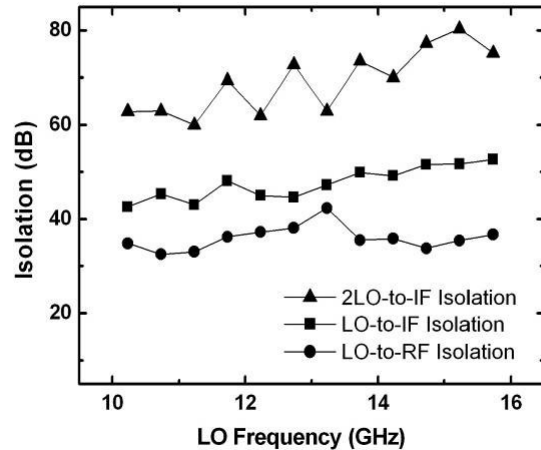


Fig. 5. Isolations vs. LO Frequency

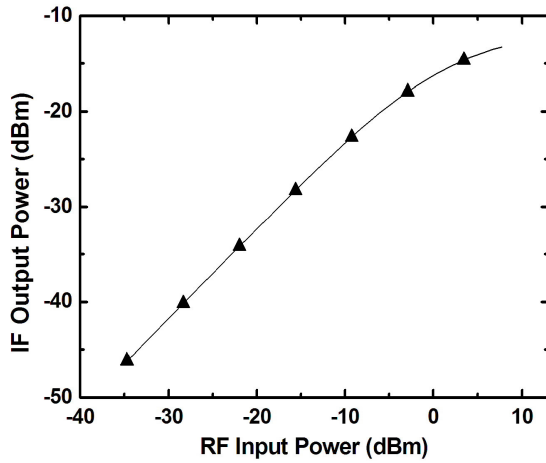


Fig. 6. Output Power vs. RF Input Power

TABLE I  
PERFORMANCE SUMMARY

Parameter	Simulated	Measured
RF Frequency (GHz)	28	28
RF Return Loss (dB)	10.7	8.1
Conversion Loss (dB)	11.02	11.15
SSB Noise Figure (dB)	11.05	11.6
IP <sub>1dB</sub> (dBm)	-4.5	-2.7
P <sub>DC</sub> (mW)	0.4	0.64

A figure of merit (FOM) is the value of a fair presentation that represents the performance of a circuit. The FOM of mixer has been defined here is [11]

$$\text{FOM} = 20 \cdot \log(f_{\text{RF}}) + \text{CG} - \text{NF} + \text{IIP}_3 - 10 \cdot \log(P_{\text{DC}})$$

where  $f_{\text{RF}}$  is the RF frequency normalized to 1 Hz, CG is the conversion gain in dB, NF is the single-sideband noise figure in dB, IIP<sub>3</sub> is the third-order input-referred intercept point in dBm, and P<sub>DC</sub> is the power consumption in mW normalized to 1mW. Here we particularly include another important parameter of  $f_i$  to normalize the used process. The new FOM<sub>1</sub> is defined as below

$$\text{FOM}_1 = 20 \cdot \log(f_{\text{RF}}/f_i) + \text{CG} - \text{NF} + \text{IIP}_3 - 10 \cdot \log(P_{\text{DC}})$$

All higher parameter values show better performances are accounted to the FOM<sub>1</sub>. Therefore, a larger FOM<sub>1</sub> would show an overall better performance of a mixer design. Table II compares the experimental results of Si-based mixer designs operated at millimeter-wave frequencies. The high performance sub-harmonic mixer discussed here is able to achieve a FOM up to 158, which is higher compared to the other previous works.

## V. CONCLUSIONS

The proposed sub-harmonic mixer has features of low conversion loss, small size, and a simple architecture for integrated millimeter-wave circuits. The LO signal is generated by a NP-MOS frequency doubler to provide an efficiently pumping to a single end mixer. The obtained FOM of 158 is the best result among the previous CMOS subharmonic mixer design at Ka band.

## ACKNOWLEDGEMENT

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## REFERENCES

- [1] Xiang Guan, and Hajimiri, A., "A 24-GHz CMOS front-end," *Solid-State Circuits, IEEE Journal of* Volume 39, Issue 2, Feb. 2004 Page(s):368 – 373
- [2] Xiaohua Fan, and Sanchez-Sinencio, E., "3-22GHz CMOS distributed single-balanced mixer," *SOC Conference, 2004. Proceedings IEEE International* 12-15 Sept. 2004 Page(s):93 – 96
- [3] Ming-Da Tsai, and Huei Wang, "A 0.3-25-GHz ultra-wideband mixer using commercial 0.18- $\mu\text{m}$  CMOS technology," *Microwave and Wireless Components Letters, IEEE* Volume 14, Issue 11, Nov. 2004 Page(s):522 – 524
- [4] Lynch, M.W., Holdenried, C.D., and Haslett, J.W., "A 17-GHz direct down-conversion mixer in a 47-GHz SiGe process," *Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE* 8-10 June 2003 Page(s):461 – 464
- [5] Ellinger, F., "26-34 GHz CMOS mixer," *Electronics*

- Letters Volume 40, Issue 22, 28 Oct. 2004 Page(s):1417 – 1419
- [6] Ellinger, F., Rodoni, L.C., Sialm, G., Kromer, C., von Buren, G., Schmatz, M.L., Menolfi, C., Toifl, T., Morf, T., Kossel, M., and Jackel, H., “30-40-GHz drain-pumped passive-mixer MMIC fabricated on VLSI SOI CMOS technology,” *Microwave Theory and Techniques*, IEEE Transactions on Volume 52, Issue 5, May 2004 Page(s):1382 – 1391
- [7] Ellinger, F., “26.5–30-GHz Resistive Mixer in 90-nm VLSI SOI CMOS Technology with High Linearity for WLAN,” *Microwave Theory and Techniques*, IEEE Transactions on Volume 53, Issue 8, Aug. 2005 Page(s):2559 – 2565
- [8] Verma, A., Li Gao, O, K.K., and Lin, J. , “A K-band down-conversion mixer with 1.4-GHz bandwidth in 0.13  $\mu\text{m}$  CMOS technology,” *Microwave and Wireless Components Letters*, IEEE Volume 15, Issue 8, Aug. 2005 Page(s):493 – 495
- [9] Viallon, C., Graffeuil, J., and Parra, T., “High performance K-band active mixer using BiCMOS SiGe process,” *Electronics Letters* Volume 41, Issue 3, 3 Feb 2005 Page(s):134 - 135”
- [10] Wang, Y., Duster, J.S., Kornegay, K.T., Hyun-min Park, and Laskar, J.,” An 18 GHz low noise high linearity active mixer in SiGe,” *Circuits and Systems*, 2005. ISCAS2005. IEEE International Symposium on 23-26 May 2005 Page(s):3243 - 3246 Vol. 4
- [11] Lam, J.: ‘1.2V CMOS down conversion mixer and VCO design for RF front-end transceiver applications’. MAsc thesis, McMaster University, Canada, 2003

TABLE II  
COMPARISONS WITH FORMER WORKS

Time	2003	2004	2004	2005	2005	2005	2005	This Work
References	[4] RFIC	[5] EL	[6] MTT	[7] MTT	[8] MWCL	[9] EL	[10] ISCAS	
Technology	0.35- $\mu\text{m}$ SiGe	90-nm CMOS	90-nm CMOS	90-nm CMOS	0.13- $\mu\text{m}$ CMOS	0.25- $\mu\text{m}$ SiGe	0.35- $\mu\text{m}$ SiGe	0.18- $\mu\text{m}$ CMOS
Type	Active	Active	Passive	Passive	Active	Active	Active	Passive
Architecture	Gilbert Cell	Gilbert Cell	Drain pumped	Gate pumped	Gilbert Cell	Gilbert Cell	Gilbert Cell	Sub- harmonic
RF frequency (GHz)	17.35	30	35	27	19	20	18	28
LO frequency (GHz)	17.35	27.5	32.5	24.5	16.3	19	17.9	13.2
IF frequency (GHz)	0	2.5	2.5	2.5	2.7	1	0.1	1.6
Conversion Gain (dB)	12	-2.6	-4.6	-10.3	1	18.2	4.5	-11.15
IIP <sub>3</sub> (dBm)	-10	0.5	2	12.7	-2	-19	-1	8
SSB Noise Figure (dB)	11.5	13.5	7.9	11.4	9	15	10.1	11.6
Isolation (dB)								
LO-IF	NA	NA	45	22	50	65	NA	63
2LO-IF	20		11	24	41	35	31	48
P <sub>DC</sub> (mW)	39.6	20	0	0	6.9	550	16.5	0.64
Chip Area (mm <sup>2</sup> )	0.9646	0.2	0.235	0.1216	0.5313	2.1	NA	0.3
FOM <sub>1</sub>	149	137	156	156	149	141	153	158