Demonstration of scaled Ge p-channel FinFETs integrated on Si

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Abstract

We report the first demonstration of scaled Ge p-channel FinFET devices fabricated on a Si bulk FinFET baseline using the Aspect-Ratio-Trapping (ART) technique [1]. Excellent subthreshold characteristics (long-channel subthreshold swing SS=76mV/dec at 0.5V), good SCE control and high transconductance (1.2 mS/μm at 1V, 1.05 mS/μm at 0.5V) are achieved. The Ge FinFET presented in this work exhibits highest g_m/SS at V_{dd}=1V reported for non-planar unstrained Ge pFETs to date.

Introduction

Recently, FinFETs (or tri-gate transistors) have been identified as the transistor architecture of choice to enable Moore's law to continue for the years to come [2-4]. To further improve device performance, high mobility semiconductor materials, in particular InGaAs for n-type and Ge for p-type transistors [5-15], are being investigated to replace Si as the channel. In this work we present the first demonstration of scaled Ge p-channel FinFETs integrated on a bulk Si FinFET platform using ART hetero epitaxy.

Process Integration

Non-coalesced aspect-ratio-trapping hetero epitaxy [1] (Fig. 1) involves the heterogeneous epitaxial growth inside trenches trapping the threading dislocations that originate at the heterostructure interface and propagate into the epitaxy region along the <111> directions. When applying a height-width aspect ratio of the active area larger than ~1.4 threading dislocations terminate at the STI interface leaving the top part defect-free for device definition. After careful optimization of the Ge heterogeneous epitaxy growth conditions, high-quality

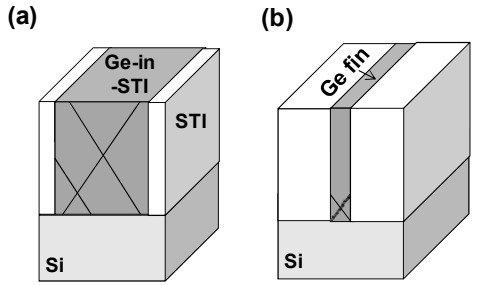

Figure 1. Schematic of Ge-in-STI epitaxy in wide (a) and narrow (b) active areas. If height-to-width aspect ratio of the heterogeneous epitaxy region is larger than 1.4, threading dislocations in narrow trenches originating from the interface will terminate at the STI sidewalls leaving the top part defect-free for device definition, i.e. Aspect-Ratio-Trapping (ART).

- (100) Si wafers
- STI Formation
- Ge fin formation
- Nwell implant + anneal
- Si cap passivation
- Gate formation
- B extensions
- Spacers
- B HDD + anneal
- S/D epitaxy
- NiGe formation
- M1 Back-end

Figure 2. Process flow of the Ge ART bulk FinFET used in the present work.

Ge was obtained in the top part of the fin. Ge p-channel FinFETs were fabricated using the process flow as shown in Fig. 2. (100) Si wafers are used as starting material and the fins are defined in the [100] channel direction. Thin Si interfacial layer was used for interface passivation [6-9] and subsequently HfO_2/TiN was deposited as gate stack. Standard implanted B extensions, B HDD, S/D epitaxy and Ni metallization scheme was used for S/D contacts [7]. Fig. 3 shows cross-sectional TEM images through the fin after full device processing. (110) facets were formed at the corners of the fin top, related to the relatively high thermal budget used during the selective Si cap deposition. Conformality of the metal gate, dielectric and Si cap layers was within 15% (Fig. 3b,c). All device parameters are normalized to the effective device width $2 \cdot H_{fin} + W_{fin}$.

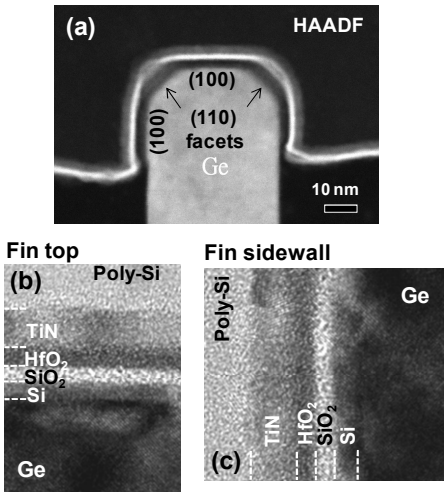

Figure 3. TEM micrographs of cross-sections of a Ge FinFET (W_{fin}=40nm) after full processing: (a) High Angle Annular Dark Field (HAADF) image of the Ge FinFET device showing the (110) facets at the corners of the fin and high resolution TEM images showing the gate stack on fin top (b) and fin sidewall (c). Conformality is within 15%.

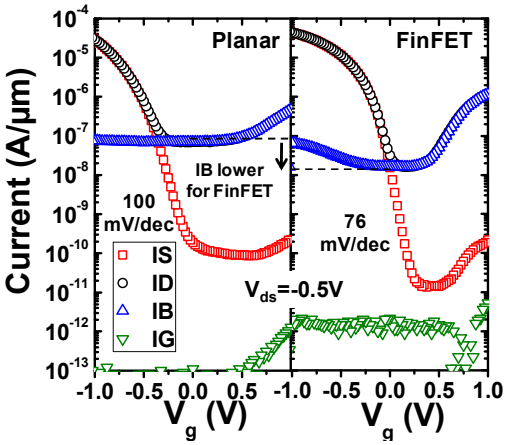

Figure 4. Long channel IV (1 μm) at V_{ds}=-0.5V comparing a Ge planar device and Ge FinFET. Note that I_{bulk} is lower for FinFET. SS for FinFET was 76 mV/dec, while for Ge-in-STI planar device SS equals 100 mV/dec.

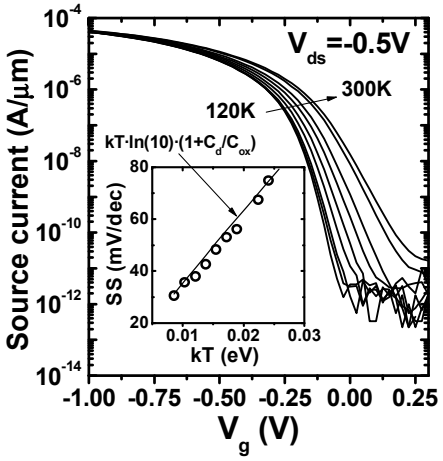

Figure 5. Long channel (1 μm) I_s/V_g at V_{ds}=-0.5V of Ge FinFET measured at different temperature. Inset: SS vs. kT. The fit assumes C_{it}=0. Charge pumping measurements confirmed good quality dielectric/ channel interface (N_{it}=2·10^{10}cm^{-2}). C_{ox} was determined from CV. The channel doping corresponding to the fitted depletion capacitance (C_d) was used in our 3D TCAD calibration (see Fig. 12).

Device Results

Long channel (1 μm) transfer characteristics at V_{ds}=-0.5V for a Ge-in-STI planar and a Ge FinFET are shown in Fig. 4. Firstly, we observe a reduction in the bulk current, that limits $I_{d,off}$, for the FinFET and secondly the SS for the Ge FinFET was 76 mV/dec indicating a low D_{it} gate dielectric/channel interface. This was confirmed by charge pumping measurements on long channel Ge FinFETs (N_{it}=2·10^{10}cm^{-2}). Low temperature I_s/V_g measurements were conducted and SS was plotted as a function of T (Fig. 5). SS follows ideal kT·ln(10)·(1+C_d/C_{ox}) and the corresponding depletion capacitance, C_d, is used as input parameter in our TCAD calibration (see Fig. 12). It was demonstrated by [6-8] that off-state drain current for Ge MOSFET suffers from junction/well band-to-band tunneling (BTBT) and trap-assisted tunneling (TAT) mechanism due to the relatively small band gap of Ge (~0.66eV) [16,17].

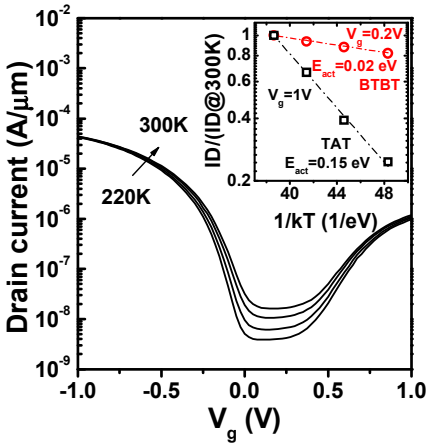

Figure 6. Long channel I_d/V_g (1 μm) at V_{ds}=-0.5V of Ge FinFET measured in the temperature range of 220-300K. Inset: Arrhenius plot of normalized I_d. At V_g=0.2V leakage current is dominated by TAT leakage with E_{act}=0.15eV and at V_g=1V BTBT leakage (E_{act}=0.02eV) is dominating.

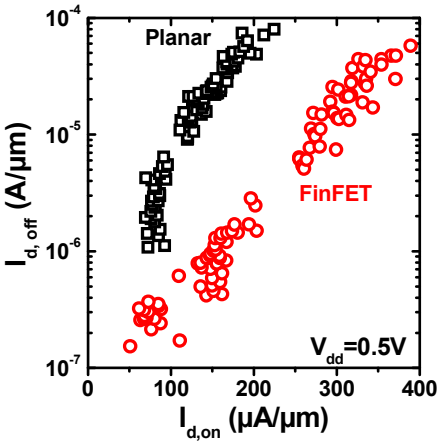

Figure 7. $I_{d,on}$ vs I_{off} at V_{dd}=0.5V measured at V_t offset (I_{off} at V_t+125mV; I_{on} at V_t-375mV) comparing Ge-in-STI planar and Ge FinFET devices.

In our devices, we investigated the leakage mechanisms by low temperature I_d/V_g measurements on long channel devices (Fig. 6) and plotting normalized I_d at different V_g in the substhreshold region vs 1/kT (see inset). At V_g=0.2V, we find an activation energy of ~0.15eV which is consistent with the TAT mechanism [17]. In strong accumulation (V_g=1V) gate-induced drain leakage (GIDL) becomes dominant by a BTBT mechanism being virtually temperature independent. Fig. 7 shows the I_{on}/I_{off} measured at V_{ds}=-0.5V and fixed gate overdrive comparing the Ge planar devices and FinFETs. The performance benefit of the FinFET is attributed to the better electrostatic gate control over the channel. The latter becomes apparent from Fig. 8, where DIBL and V_t are plotted as a function of L_g comparing the planar and FinFET devices. R_{ext} was determined as 82 Ω·μm (Fig. 9) which is comparable to the value reported for an optimized contact scheme [6]. Fig. 10 shows average peak transconductance vs gate length. Highest peak g_m for a gate length of 70nm was 1.2 mS/μm at 1V and 1.05 mS/μm at 0.5V. Figs. 11-13 show the subthreshold and output characteristics of a short channel FinFET.

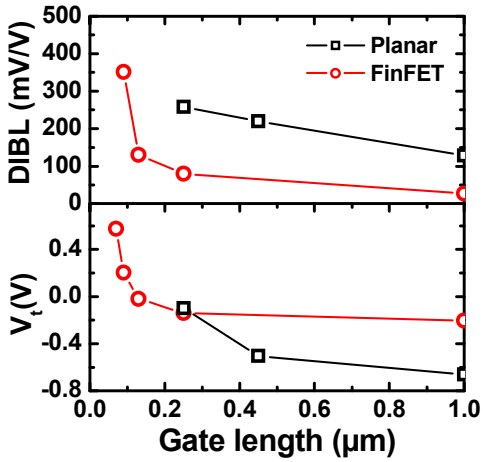

Figure 8. DIBL vs L_g and V_t roll-off curve at V_{ds}=-50mV for Ge planar device and Ge FinFET. SCE immunity is improved for the FinFET architecture.

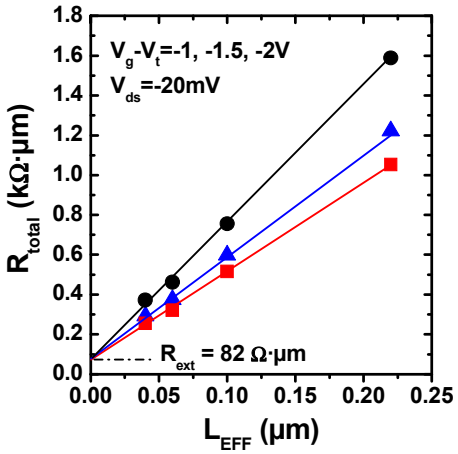

Figure 9. R_{total} (=V_{ds}/I_{ds} with I_{ds} at V_{gs}-V_t=-1,-1.5,-2V and V_{ds}=-0.02V) vs effective gate length L_{eff} of Ge FinFET. R_{ext} was determined as 82 Ω·μm, similar as was found in [6].

3D TCAD simulations were performed using an in-house model based on experimentally calibrated parameters. Our initial results match well with the experimental data (Fig.12). Fig. 14 shows g_m/SS_{sat} plots at V_{dd} of 1V benchmarking our Ge FinFET data with recent unstrained Ge MuGFETs [11-15]. The Ge FinFET presented in this work exhibits highest g_m/SS at V_{dd}=1V reported for non-planar unstrained Ge pFETs to date.

Conclusions

We report a Ge FinFET integrated onto a bulk Si FinFET platform. Excellent subthreshold characteristics (long channel SS=76mV/dec), good SCE control and high performance (1.2mS/μm at V_{dd}=1V) are achieved. The Ge FinFET presented in this work shows best g_m/SS_{sat} of relaxed Ge MuGFET devices reported to date and paves the way for introduction of Ge as a PMOS option for future FinFET technologies.

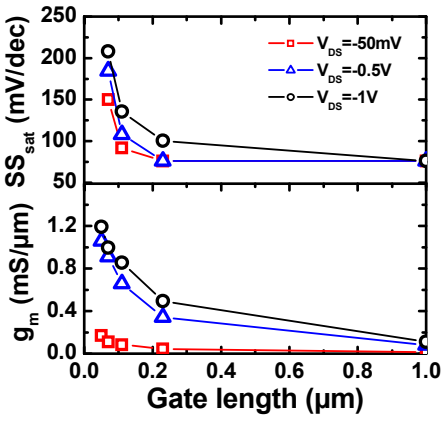

Figure 10. Subthreshold swing and peak g_m at V_{ds} = -0.05V, -0.5V and -1V as a function of gate length for Ge FinFET.

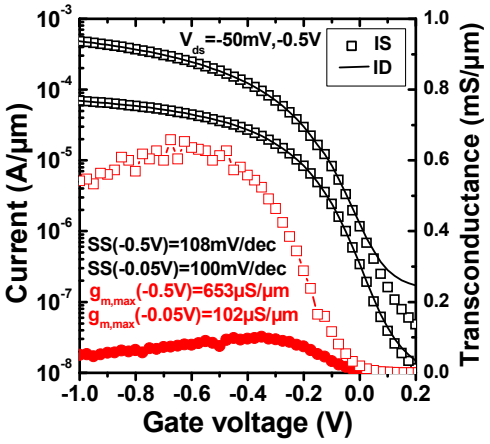

Figure 11. Linear (V_{ds}=-50mV) and saturation (V_{ds}=-0.5V) subthreshold characteristics (symbols: source current, solid line: drain current) and extrinsic transconductance of Ge FinFET (L_g=110nm).

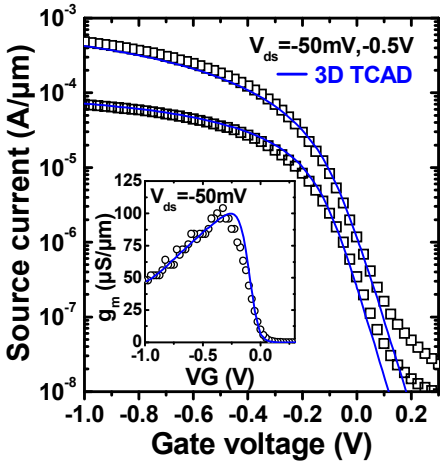

Figure 12. Subthreshold characteristics and linear transconductance (inset) of Ge FinFET (L_g=110nm) comparing measured data and 3D TCAD calibration using in-house model based on experimentally calibrated parameters.

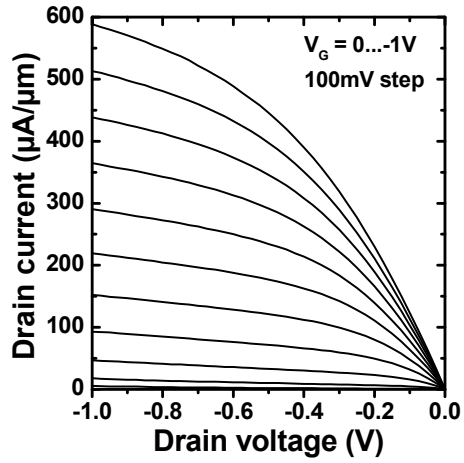

Figure 13. Output characteristics of Ge FinFET (L_g=110nm).

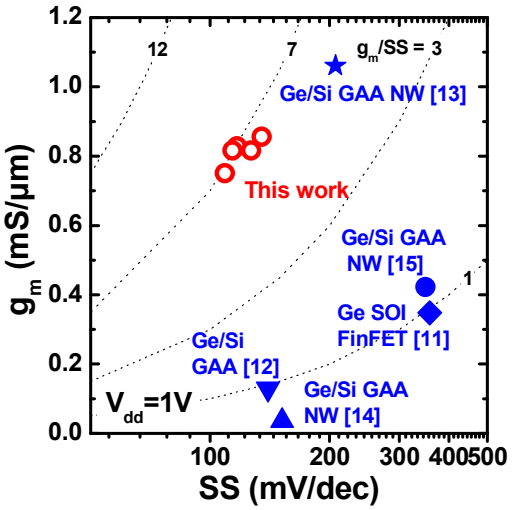

Figure 14. g_m vs SS benchmark at V_{dd}= 1V for Ge FinFETs. Included are Ge-on-Insulator FinFETs [11], Ge gate-all-around (GAA) [12], Ge/Si core/shell nanowire (NW) GAA [13-15]. For NW data, device width is normalized with wire perimeter π·d. At 1V, our data represent best g_m/SS_{sat} compared to recent unstrained Ge MuGFET devices.

Acknowledgement - IMEC is acknowledged for processing capabilities and technical support. The authors would like to thank Dr. Y. C. Sun for management support.

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