MMW Lab In-Situ to Extract Noise Parameters of 65nm CMOS Aiming 70~90GHz Applications

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***Abstract* — In this paper, the design and use of an In-Situ Tuner (IST) aiming On-Wafer multi-impedance method are presented. The conventional method using Off-Wafer Tuner is limited by the frequency range and has losses between this external Tuner and the Device Under Test (DUT). Here, IST is placed near the DUT to achieve higher |Γ| and to cancel losses between the impedance generator and the device. The architecture of the Tuner is based on variable lumped R and C elements fulfilled with Cold-FET and varactors controlled through biasing and associated to coplanar transmission line (cpw-TL) for phase shifting. Detailed and dedicated noise de-embedding technique is described to extract the 4 noise (NF_{min}, R_n, Γ_{opt}) parameters of a 65nm MOSFETs silicon transistor through the use of this in-situ multi-impedance method. The 75-110GHz noise test bench using cold-noise source method and the noise measurement are described showing Transistor capabilities at MMW.**

***Index Terms* — Active devices, transistors, MOSFET, in-situ lab., Impedance tuner, noise microwave measurement, multi-impedance, varactor, transmission lines, cold FET.**

I. Introduction

Actual and coming High Frequency (HF) dynamic performances of Si devices (CMOS: MOSFETs) are very attractive for mass market applications (60GHz WLAN & WPAN, Wireless HDMI, Wireless USB, 77GHz automotive radars …) and to forecast design in MMW-band. They present cut-off frequencies higher than 200GHz and NF_{min} in the range of 2dB@60GHz. In order to increase their intrinsic HF performance, the optimization of the process step and the modeling in MMW-range to build accurate electrical models are key issues. HF characterization of Noise behavior is so mandatory in this frequency range.

The theory of linear noisy network teaches us that the whole knowledge of the noise in linear two-port at fixed frequency requires the knowledge of the four noise parameters NF_{min}, R_n, Real(Γ_{opt}), Imag(Γ_{opt}) [1] where Γopt is the optimum reflection coefficient provided by the source admittance $Y_{opt}=G_{opt}+jB_{opt}$. Therefore, the challenge is to characterize these 4 noise parameters of the device up to 110GHz on Transistor having Γopt very different to 50Ω and NF_{min} around 2dB in that frequency range. This paper presents the extraction of the 4 noise parameters based on in-situ tuner design for optimum on wafer MOSFET measurement. This In-Situ Tuner is integrated near the Transistor on the On-Wafer tested structure and used to apply multi-impedance method.

Firstly, the tuner specifications are defined and its design is presented. Secondly, we describe the proposed noise measurement setup based on multi-impedance method and Cold noise source. Thirdly, the dedicated de-embedding is developed and finally we present the nMOS noise extraction results.

II. In-Situ Tuner (IST) Design

The architecture of the tuner uses lumped element, cold-nMOS (as variable resistance) in series with a varactor (as variable capacitance) and a cpw-TL:

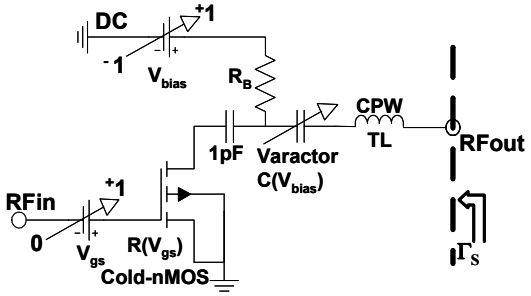


Figure. 1. Electrical representation of the IST

First of all, to know impedance to be synthesized, a large set of MOS transistors in the tested technology has been studied through electrical model in term of stability circles, optimal source reflection coefficient for NF_{min}, and available gain in the concerned frequency range.

The first prototype has been achieved on STMicroelectronics 65nm HR SOI technology on High Resistivity (HR) substrate providing 6 metallization [2]

levels for analog applications and more for digitals. The used TL is a coplanar one with Z_c near 50Ω. [2-3-4].

In addition, a varactor based on N^+poly/Nwell structure is used. The device is made of 5 poly fingers in parallel. Each finger has 0.35µm length and 3µm width. A cold-nMOS based on 80 poly fingers (Lg= 0.12µm, Wu=0.5µm) in parallel with two gates accesses is used as variable resistor.

The sensitivity and the repeatability of the impedances have to be taken into account in the method robustness to guarantee the same impedances during alone TUNER characterization and DUT (=TUNER + DEVICE) one [5].

On Fig.2, overviews of the IST layout and an example of the synthesized impedance are illustrated at 80 GHz using three different TL lengths.

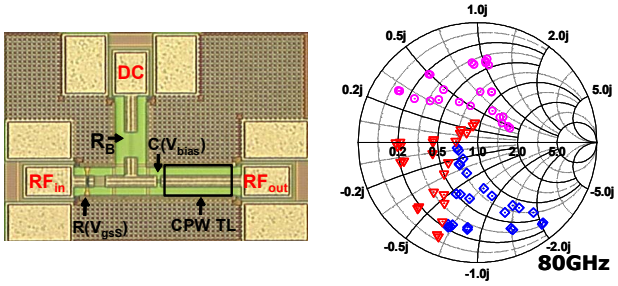


Fig.2 (Left) In-Situ Tuner layout;
(Right) example of synthesized impedance @ 80GHz

III. MULTI-IMPEDANCE NOISE EXTRACTION METHOD BASED ON 50Ω NOISE BENCH AND IST

A. Noise Test Bench in W Band.

Fig.3 represents the IEMN in-house [6] waveguide noise figure measurement setup, which has been designed for broad band measurements in 75-110 GHz frequency range. The measurements are based on cold-noise source. The measurements in whole W band are enabled by the use of a frequency down-converter (FDC). The FDC is composed by a Millitech® mixer with a quite low value for conversion loss (11 dB) and which converts the noise in W band to a fixed IF equaled to 100 MHz. The IF signals are measured by a HP NFM 8970B (the LNA with the FDC and the NFM formed the W noise receiver). The local oscillator signal of the mixer is generated by a HP8362 sweeper; gain is amplified through a Miteq® medium power amplifier and tripled with a passive Tripler fabricated by Millitech®. The use of a LNA with very low noise characteristics (NF=~4.5dB, manufactured by Spacek®) led to the decrease of the FDC noise figure and an increase of the sensitivity of noise receiver.

The noise source is connected to the output switch in order to calibrate the W noise receiver.

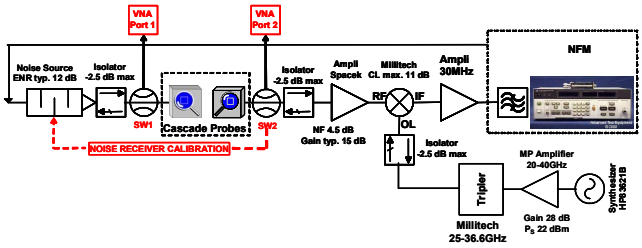


Fig.3 50Ω•Noise-figure measurement setup used in MMW band

B. Multi-Impedance Method

Introduced by R.Q Lane at the end of the 60th year [7], the multi-impedance technique consists in the extraction of the 4 noise parameters by the measurement of 4 noise factors for 4 different source admittances $Y_S=G_S+jB_S$.

The principle of this method is to extract the four noise parameters, from noise figure or noise powers measured for several Γ_S, using numerical procedure.

In the conventional setup the tuner is located Off-Wafer and is usually a mechanical one. One of the main limitation of Off-Wafer TUNER is the area of the $|\Gamma_S|$ achievable in the DEVICE reference plane due to losses between external TUNER and DEVICE input (cables, connectors, RF probes) mainly in MMW frequency range. The second limitation is the test time. The proposed solution is based on multi-impedance concept but uses integrated tuner in the test structure On-Wafer. The method is based on Fig.4 setup using (P'1S, P'2S) reference plane and Eq.1.

$$NF = NF_{\min} + \frac{R_n}{G_S}\left|Y_S - Y_{opt}\right|^2 = \left[A + B\left(G_S + \frac{B_S^2}{G_S}\right) + C\frac{1}{G_S} + D\frac{B_S}{G_S}\right] \quad (1)$$

Eq.1 is linear regarding 4 parameters (A, B, C and D) that can be obtained by the measurement of a minimum set of 4 noise factors for 4 different admittances (Y_S).

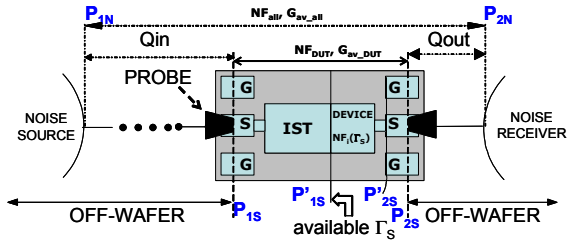


Fig.4 Multi-impedance method test bench (Tuner On-Wafer)

Thanks to (A, B, C, D) determination [5], we can obtain NF_{min}, R_n, and Γopt. Nevertheless, for extraction accuracy reason, we approximately use "N=80" instead of 4

different source admittances (Y_s), and deduce A, B, C and D by minimizing the error ε defined by Eq.2:

$$\varepsilon = \frac{1}{2}\sum_{i=1}^{N}\frac{1}{NF_i^2}\left[A+B\left(G_{Si}+\frac{B_{Si}^2}{G_{Si}}\right)+\frac{C}{G_{Si}}+\frac{DB_{Si}}{G_{Si}}-NF_i\right]^2 \quad (2)$$

C. Cold Noise Source in W Band

As shown above in the test bench synoptic the reference plane for the receiver calibration is at the input of the second switch (see sw2 on Fig.3).

Measurement methods vary for different applications; some applications have high gain and low noise figure, some have low gain and high noise figure (mixer…), and some have very high gain and wide range of noise figure (receiver systems). Measurement methods have to be chosen carefully. In our case Cold-noise source is chosen because of Tuner's high losses [5] and low DUT gain at these frequencies.

IV. Experimental Results

In this section, we present the experimental data obtained with this study.

A. De-embedding Procedure and Noise Experimental results.

The principle of the Cold-noise source technique is to measure just the cold-noise power "P_{cold}" of the DUT when a 50• termination is applied to its input. The available gain "G_{av_all}" (Fig.4) is also required to be measured in this method. Having these two values, gain and noise power of whole system, the whole noise figure "NF_{ALL}" is calculated between P1N and P2N using Eq.3.

$$NF_{ALL} = \frac{P_{cold}}{kTBG_{avALL}} \quad (3)$$

Where B is the bandwidth over which the cold-noise power measurement (P_{cold}) is made. The temperature T is set to 290K and k=1.38 x 10^{-23}J/K.

The method is based on Fig.4 setup using (P1N, P2N) as noise reference plane. We first measure the cold noise power (P_{cold}) in P2N and after we go through 3 de-embedding steps to obtain intrinsic DEVICE noise results in (P'1S, P'2S) planes in Fig.5.

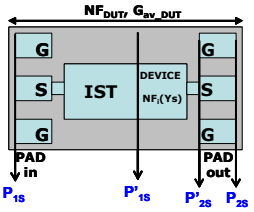
(Step.1): transform the cold noise power "P_{cold}" (Fig.4) to the noise figure (Eq.3) of the whole system between (P1N, P2N): initial references.

(Step.2): thanks to the use of FRIIS formula (Eq.4) we obtain the noise figure (Fig.6-Left) of the DUT (=TUNER + DEVICE) between (P1S, P2S)

$$NF_{DUT} = G_{avQin} * NF_{ALL} + \frac{G_{avQout}-1}{G_{avDUT}*G_{avQout}} \quad (4)$$

(Step.3): At the 3rd step before applying the FRIIS formula between (P1S, P2S) (see Fig.4,5) to obtain noise parameter of intrinsic DEVICE (nMOS) between P'1S and P'2S, we must determine the S parameter of input and output GSG PAD.

The determination of the equivalent input and output PAD S matrix is achieved by the measurement of associated OPEN structure. The measure of the associated OPEN structure allows us to define two equivalents 2 ports device (Fig.5).



$$PAD_{IN}: \quad Z_{OPEN\_IN} = \frac{1}{\psi}\begin{bmatrix}1 & 1\\ 1 & 1\end{bmatrix};\ \psi = \frac{1}{Y_{OPEN}(1,1)+Y_{OPEN}(2,1)}$$

$$PAD_{OUT}: \quad Z_{OPEN\_OUT} = \frac{1}{\zeta}\begin{bmatrix}1 & 1\\ 1 & 1\end{bmatrix};\ \zeta = \frac{1}{Y_{OPEN}(2,2)+Y_{OPEN}(2,1)}$$

Fig5. PAD 2*2ports devices representation

After having the impedance matrix of the equivalent PAD IN and PAD OUT capacitance, we can compute (PAD IN + IST) and PAD OUT available gains and apply FRIIS (Eq.5) between P1S and P2S to extract intrinsic DEVICE (nMOS) noise figure between P'1S and P'2S (Fig.6-Right)

$$NF_{DEVICE} = G_{avPAD_{IN}+IST} * NF_{DUT} + \frac{G_{avPAD_{OUT}}-1}{G_{avDEVICE}*G_{avPAD_{OUT}}} \quad (5)$$

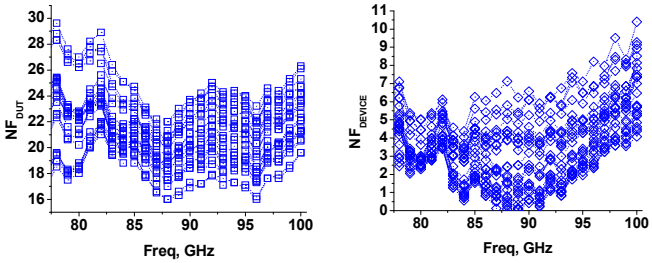


Fig.6 (Left) NF at the DUT plane between (P1S, P2S)
(Right) NF at the DEVICE plane between (P'1S, P'2S)
nMOS Device bias are Vgs=0.72V and Vds=1.2V

Now we can apply the multi-impedance method to extract the four noise parameters of the DEVICE (nMOS).

B. Extraction of the Four Noise Parameters

The extraction of the four noise parameters is achieved by the use of the in-house multi-impedance method

developed on ADS ® "Advanced Design System" software.

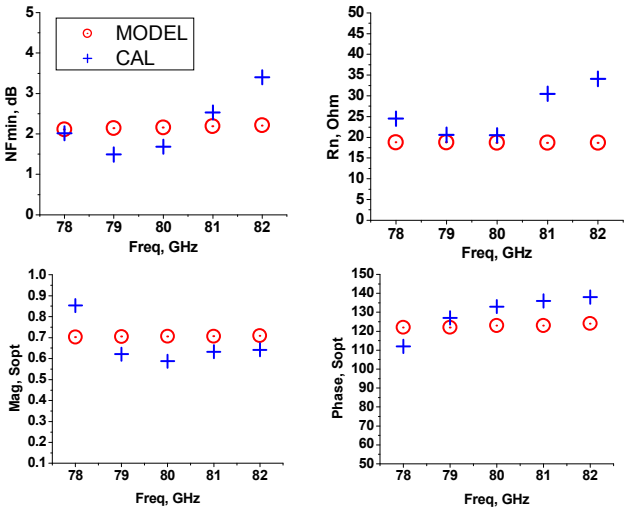


Fig.7. The four Noise Parameters of the (40*0.06)µm² nMOS (Vg/Vds = 0.72/ 1.2V) with 2 Gates Accesses

Fig.7 shows the 4 noise parameters of the DEVICE (nMOS) from 78GHz up to 82GHz frequency range. Above 82GHz nMOS has no gain any more that is why NF has no signification and is no shown.

C. Perspectives for Tuner improvement

As shown in Fig.8, we can see a good agreement between Tuner measurements and electrical simulations.

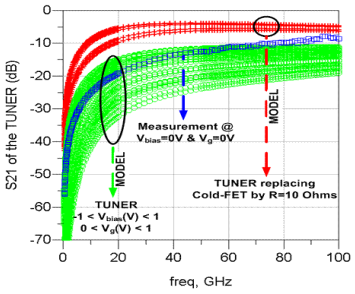


Fig.8. Tuner S_{21} simulation versus measurement

Nevertheless, we observe insertion losses around 20dB in the 60-100GHz range. Reducing the Cold-FET resistance would improve losses as shown in the same figure. This losses reduction will allow higher $\Gamma(Y_S)$ at the Transistor input. In addition reducing C_{gs} of the cold-FET will also improve losses.

VII. CONCLUSION

The extraction of the four noise parameters (NF_{min}, R_n and $Y_{opt}=G_{opt}+jB_{opt}$) of Si 65nm CMOS in MMW range is presented on this paper. The used technique is the multi-impedance test set, based on In-Situ Tuner directly integrated near the Transistor. The trade-offs between the gain and the noise of the Transistor allows the choice of the noise characterization method. In our case the Cold-noise method is used to achieve measurement. The developed dedicated de-embedding steps and the electrical results in the DEVICE reference plane are shown, giving a high correlation between simulations and measurement.

We obtain NF_{min} around 2dB, Rn near 20Ω and Γopt~0.6/130°.

Next step will be to extract the noise sources of the nMOS transistor and to test methodology higher in frequency with transistors providing higher gain above 80GHz (sub 65nm CMOS and SiGeC HBT).

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