BEOL Scaling Limits and Next Generation Technology Prospects

Azad Naeemi
Georgia Institute of Technology
791 Atlantic Drive
Atlanta, GA 30332
azad@gatech.edu

Ahmet Ceyhan
Georgia Institute of Technology
791 Atlantic Drive
Atlanta, GA 30332
aceyhan3@gatech.edu

Vachan Kumar
Georgia Institute of Technology
791 Atlantic Drive
Atlanta, GA 30332
vkumar38@gatech.edu

Chenyun Pan
Georgia Institute of Technology
791 Atlantic Drive
Atlanta, GA 30332
chenyun.pan@gatech.edu

Rouhollah M. Iraei
Georgia Institute of Technology
791 Atlantic Drive
Atlanta, GA 30332
rmi3@gatech.edu

Shaloo Rakheja
Massachusetts Institute of Technology
60 Vassar Street
Cambridge, MA 02139
shaloo@mit.edu

ABSTRACT

This paper presents the major limitations to the interconnect technology scaling at future technology generations and demonstrates both evolutionary and radical potential solutions to the BEOL scaling problem. To address the local interconnect challenges, a novel hybrid Al-Cu interconnect technology is introduced. Performances of carbon-based interconnects are evaluated as a more radical solution. The impact of interconnects and the optimal interconnect options are investigated for emerging next generation devices. Interconnects for new state variables, namely spintronic interconnects, are studied and their potential performances in an all-spin logic system are evaluated.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles – *advanced technologies, VLSI (very large scale integration)*. C.4 [Computer Systems Organization]: Performance of Systems – *performance attributes*.

General Terms

Performance, Design.

Keywords

All-spin logic, carbon-based interconnects, emerging FETs, hybrid Al-Cu interconnects, new state variables, spintronic interconnects.

1. INTRODUCTION

While interconnects have imposed major limitations on integrated circuits in the past decades, the nature and severity of the interconnect problem have changed in the latest technology generations. In terms of energy, interconnects have always accounted for more than half of the capacitance on a chip; hence, have dissipated more than 50% of the dynamic power on a chip [1]. However, the gradual scaling of the dielectric constant used to mitigate the impact of the increase in the aggregate on-chip interconnect length. The scaling of the effective dielectric constant has almost stopped at around 2.5 to 2.7 due to mechanical and reliability issues [2] and it may not be possible to achieve dielectric constants below 2. In terms of delay, both local and global interconnects have imposed speed penalties. In the past, the intrinsic delays of local interconnects used to scale with technology. This is no longer true, mainly because of the resistivity increase due to size effects [3] such as extra electron scatterings at wire surfaces and grain boundaries. As a result, the intrinsic RC delay of an average length interconnect will increase in the future (Fig. 1) [4].

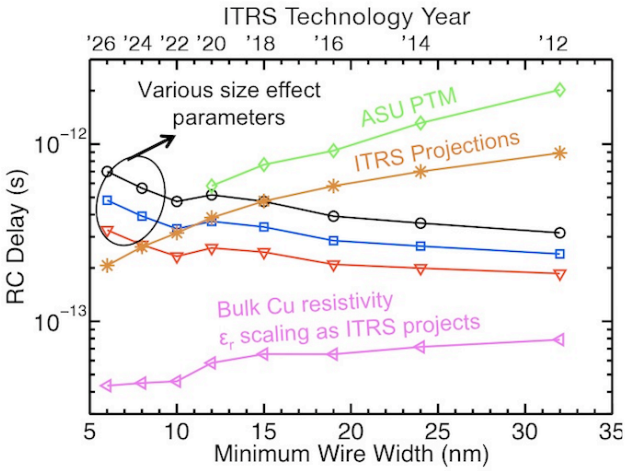

Figure 1. RC delays of 10-gate-pitch-long Cu/low-*k* wires and FinFETs are compared. Both ITRS projections [5] and predictive technology models [6] for FinFETs at sub-20-nm technology generations are illustrated.

The research in the area of interconnect technology has targeted mitigating size effects by changing or modifying the liner material to decrease electron scattering at wire surfaces, increasing grain sizes in copper to reduce grain boundary scattering, and finding and developing novel materials that may offer lower resistivities. More radical approaches involve replacing Cu wires with bundles of densely packed carbon nanotubes (CNTs) and multi-layer graphene nanoribbons (GNRs). Achieving the desired density in

DAC '14, June 01 - 05 2014, San Francisco, CA, USA

http://dx.doi.org/10.1145/2593069.2596672

CNT bundles and making reliable ohmic connections to all nanotubes are major challenges yet to be addressed [4]. For graphene, while there has been major progress in growth and fabrication, the edge scattering in narrow ribbons is a major limitation.

The semiconductor industry is exploring a diverse set of switching devices to carry technology advancement to beyond the 10-year visibility limit. Some of the potential candidates such as III-V field effect transistors (FETs) and tunnel FETs still use electronic charge as their computational state variable and some such as spintronic switches use novel state variables. These novel devices differ in structure and operating principles and they offer different connectivity challenges and opportunities.

The rest of this paper is organized as follows. In Section 2, a novel hybrid Al-Cu interconnect technology is introduced as a potential evolutionary solution to the local interconnect problem. The potential performances of carbon-based interconnects are modeled and benchmarked in Section 3. The optimal interconnect technologies for various FETs are discussed in Section 4. The potential performance of spintronic interconnects is evaluated in Section 5, and the paper is concluded in Section 6.

2. HYBRID Al-Cu INTERCONNECTS

More than a decade ago, the semiconductor industry switched from Al to Cu for its superior conductivity and its significantly better resistance to electromigration. However, it has long been known that Cu loses its conductivity advantage at nanoscale dimensions because the bulk electron mean free path (MFP) in Cu (40 nm) is larger than that in Al (16 nm), leading to more pronounced size effects in Cu wires. Furthermore, Al wires do not need diffusion barriers, which take a large fraction of the volume of a wire at nanoscale dimensions. Despite these facts, it is widely believed that it is improbable to switch back to Al because of the reliability problems caused by almost 5 times lower current conduction capacity of Al as compared to Cu. However, the mean-time-to-failure for Al wires conducting an AC current is more than 4 orders of magnitude higher compared to Al wires conducting a DC current equal to the root mean square value of the AC current [7]. This fact opens the possibility of a hybrid interconnect technology, where metals with high current conduction capacities (e.g. Cu or tungsten (W)) are used for local power distribution networks, and a low resistivity metal is used for signal wires. For short local signal wires that are minimum-sized, Al can be a promising candidate. For longer interconnect lengths with wider cross-sectional dimensions, Cu can again be used as it offers a better resistivity at larger dimensions.

A simplified sequence of the fabrication steps for the proposed hybrid interconnect technology is shown in Fig. 2 [8]. A thick layer of Al is deposited and annealed so that the grain size can be enlarged. This will result in an average grain size that is equal to the film thickness [9]. The Al film is then polished down to the desired thickness, which is followed by pattering minimum-sized Al wires with a subtractive process. Then, the dielectric material is deposited, and the trenches are made for the Cu power wires. Finally, liner/diffusion/seed layers are formed inside the trenches, and Cu is electroplated into trenches. Although this process requires two lithography/etch steps, the cost of the second step will be lower because of the relaxed pitch used for Cu wires. In principle, this process allows the signal and power wires to have different thicknesses. For power wires, important metrics are resistance and current density; thereby, larger thicknesses are desired. For signal wires, a larger thickness increases the

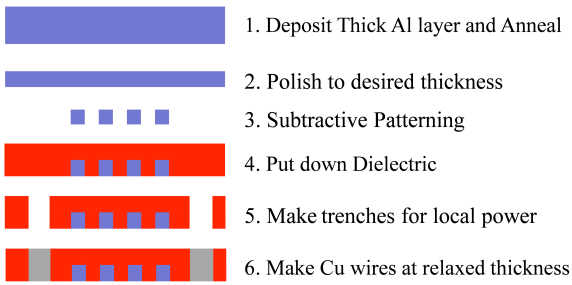

Figure 2. The flowchart of the subtractive Al-Cu hybrid interconnect manufacturing process [8].

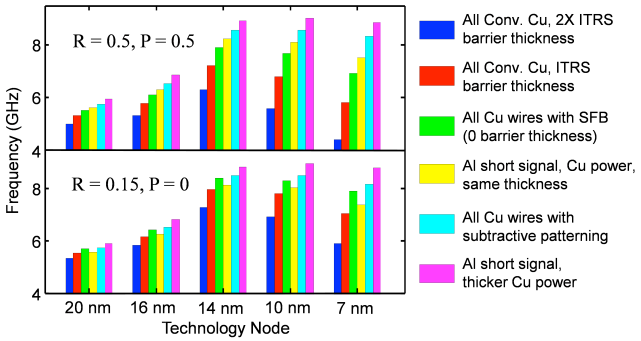

Figure 3. Optimal clock frequency is illustrated for six different interconnect configurations at multiple technology generations. Two sets of reflectivity, *R*, and specularity, *p*, parameters are used based on experimental data [8].

interconnect capacitance, which adversely affects power dissipation and even signal delay for short wires because the resistance is dominated by driver resistance.

The system-level design methodology in [10] provides the optimal clock frequency based on the multi-level interconnection network optimization, the number of logic gates, die size and power density budgets, and the device-level model. This methodology has been applied to several commercially available Intel multi-core processors crossing three technology generations from 65nm to 32nm technology node from three architectures. The simulation data for the chip throughput and clock frequency match the published raw data. In this work, device models for bulk FinFET from 20 nm to 7 nm nodes are obtained from [6].

Figure 3 illustrates the optimal clock frequency at the optimal aspect ratio for six types of interconnect architectures for various technology nodes. The optimal clock frequency begins to decrease below the 14-nm technology node; particularly for the processors using Cu interconnects with thick diffusion barriers, in which the size effects are prominent. The proposed Al-Cu interconnect technology can significantly suppress this frequency drop.

3. CARBON-BASED INTERCONNECTS

A more radical potential solution to address the local interconnect problem is to change the interconnect material all together. Carbon-based interconnects have long been considered as promising alternatives for future nanoscale interconnects due to their long mean free path (MFP), high current carrying capability and high thermal conductivity.

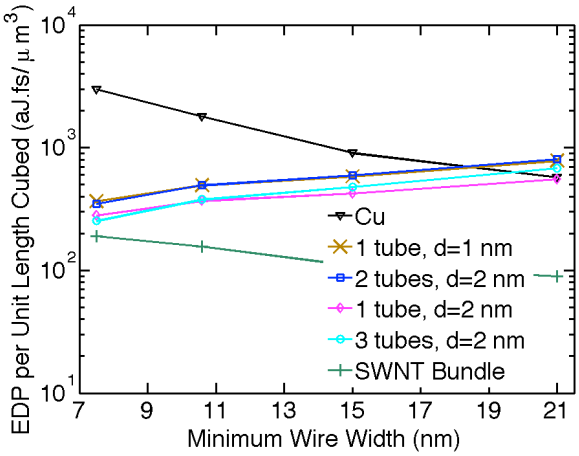

Figure 4. Comparison of the EDP per unit length cubed associated with Cu, bundles of SWNT and individual or a few parallel SWNT interconnects.

Table 1. Status update on key metrics for SWNT interconnects.

	Needed	Demonstrated
Tube diameter	>2 nm	2.5±0.4 nm [20] 1.2±0.3 nm [21]
Tube density	250 CNTs/μm	20-40 CNTs/μm [20] 10-30 CNTs/μm [21]
Conversion to metallic	~100%	25% [35]
Contact + quantum resistance	10 KΩ	10-30 KΩ [2]
Alignment	~ 100%	99.5% [21]

3.1 CNT Interconnects

Early studies on CNT interconnect showed that individual carbon nanotubes are too resistive for high-performance chips due to the limited number of conduction channels [11] and can potentially be used in ultra-low-power circuits [12]. Therefore, researchers have extensively studied CNT bundles for nanoelectronic interconnect applications. Considering the difficulties in manufacturing horizontal CNT bundles with good contacts to all the tubes in the bundle, the recent advances in manufacturing highly dense, perfectly aligned horizontal individual CNTs, and the significant increase of the resistivity of Cu wires at ultra-scaled dimensions, delay and energy per bit of individual or a few parallel SWNT interconnects are compared against that of Cu/low-*k* at future technology nodes [4]. It is assumed that a bed of horizontally aligned tubes is first laid on the substrate and then the unwanted tubes are etched away using standard lithography techniques. Using analytical models that are developed in [11] for calculating the per unit length (p.u.l.) resistances of individual SWNTs with various diameters and using RAPHAEL to estimate the p.u.l. capacitances, it is shown [4] that the RC delay of SWNT interconnect designs can outperform Cu at sub-11nm wire dimensions. Figure 4 illustrates that the EDP p.u.l. cubed associated with SWNT interconnect designs is significantly better than that of Cu due to their lower p.u.l. capacitance values. Some of the key parameter values that need to be achieved to outperform Cu interconnects are tabulated and compared against what has already been demonstrated in Table 1.

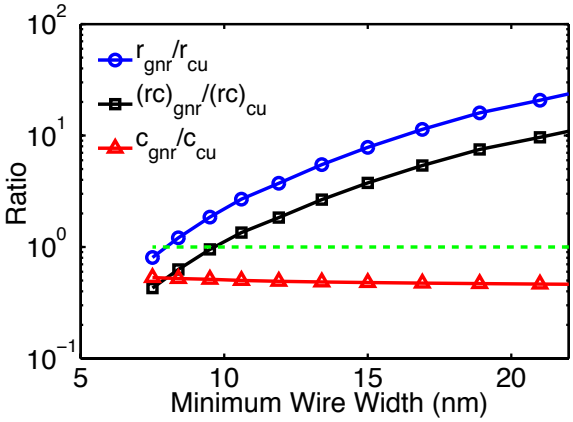

Figure 5. Ratios of p.u.l. interconnect resistance, capacitance and RC product of 5-layer GNRs to that of Cu. GNRs are assumed to have smooth edges and a MFP of 300nm.

With only a few tubes maintaining connection between the driver and the receiver, the probability of having a reliable connection and the performance of this connection are strong functions of how reliable the tubes can be manufactured.

3.2 GNR Interconnects

Graphene exfoliated from Highly Oriented Pyrolitic graphite (HOPG) has been widely used in experiments to demonstrate some of the fundamental properties of graphene [30]. However, processes like epitaxial growth on Silicon Carbide (SiC), or Chemical Vapor Deposition (CVD) growth on copper are essential for graphene to be used in integrated circuits. Although epitaxial growth on silicon carbide can provide graphene with extremely good transport properties [31], CVD growth is more suitable for interconnect applications since CVD grown graphene on copper can be transferred to other substrates. Further, it should be noted that the quality of the substrate and the interface between the substrate and graphene could severely impact the electron mean free path in graphene. Graphene transferred to a preferred substrate can be patterned into graphene nanoribbons (GNR) using conventional lithographic techniques. However, at small wire widths, scattering at the rough GNR edges can severely impact the mean free path.

Compact physical models have been developed for the effective mean free path of GNRs as a function of temperature, carrier density, substrate material, and edge quality [15]. Also, circuit models have been developed that account for the type of interconnect and contact used [14]. These analytical models were further applied to compare the delay and energy of multi-layer GNR interconnects against those of Cu. At the end of ITRS roadmap [5], the p.u.l. resistance of a 5-layer GNR with smooth edges is predicted to be comparable to that of Cu, as shown in Fig. 5. However, since the p.u.l. capacitance of a GNR is roughly half of that of Cu, the RC product of 5-layer GNR is better compared to Cu at sub-10-nm technology nodes. In addition to this performance improvement, the interconnect power is 50% lower.

Although Fig. 5 gives a rough estimate of the intrinsic interconnect performance, the driver size and the interconnect length are also critical parameters that determine the performance of the overall system. Since the delay of short local interconnects

Table 2. **Comparison table summarizing the simulation results. The number of checkmarks indicate the relative magnitude of the impact of interconnect parameters on circuit performance for various device technologies. The best interconnect option for each case is listed in order of suitability.**

Device Type	Device Resistance	Device Capacitance	Interconnect Resistance Impact		Interconnect Capacitance Impact		Best Interconnect Option (targeting EDP)	
			Short	Long	Short	Long	Short	Long
FinFET	Reference	Reference	✓	✓✓✓	✓✓✓	✓✓✓	Bundle	Bundle, GNR*, SWNT*
CNFET	Low	Low	✓✓	✓✓✓	✓✓✓	✓✓✓	Bundle	Bundle, GNR*, SWNT*
TFET	High	Low		✓✓	✓✓✓✓	✓✓✓	SWNT, GNR	SWNT, SWNT*, GNR
Sub-Vt	Very High	Reference		✓✓	✓✓✓✓	✓✓✓✓	SWNT, SWNT*, GNR*	SWNT, SWNT*, GNR*

* indicates smooth edges in the case of GNR interconnects and high-density in the case of mono-layer SWNT interconnect.

is primarily dependent on the driver resistance and interconnect capacitance, GNR is more suitable for short interconnects. However, since the intrinsic delay of interconnects is important at longer lengths, GNRs need to have good quality substrates, smooth edges, good contacts that couple to all the layers, and edge doping to beat Cu. Since hexagonal boron-nitride (h-BN) has lattice that closely matches with graphene, mean free paths as high as 1 μm have been demonstrated for graphene on h-BN substrate [32]. The same paper [32] demonstrates good contacts that couple to both layers of bi-layer graphene. However, this research has been carried out on exfoliated graphene and has not yet been demonstrated on CVD graphene. Although atomically smooth GNRs epitaxially grown on SiC have been demonstrated [31], GNRs obtained from patterning CVD graphene still suffer from significant scattering at the edges. Further, to compensate for the effect of charge screening in multi-layer graphene [33], it is essential to dope the GNR edges of different layers.

4. EMERGING DEVICES

The research pipeline of the semiconductor industry involves increasingly radical potential solutions to carry technology advancement through dimensional scaling to beyond conventional CMOS. Many companies encourage and conduct research on emerging device technologies, which utilize novel materials and concepts of transport, such as carbon-based devices and tunneling FETs (TFETs). However, any device technology that offers advantages in performance, power dissipation or ease in dimensional scaling will have to be complemented with an interconnect technology that offers similar trades. Therefore, it is crucial to investigate the interactions of interconnects with all these emerging devices to obtain the best circuit performance. As the resistance and capacitance values of different device technologies vary significantly, the constraints that they put on interconnects are quite different as well. In this section, we pair various emerging device technologies, such as CNFETs [16], FinFETs [17], TFETs [18] and sub-threshold CMOS, with both conventional Cu/low-*k* and emerging carbon-based interconnects, whose potential has been established in previous sections, to compare the impact of different interconnect technology parameters on device performance at the circuit-level.

The delay and EDP performances of the device-interconnect pairs are calculated using a driver connected to a receiver through an interconnect of varied length. A typical fan-out of 3 is also considered. The driver resistance and receiver capacitance are estimated using predictive SPICE models and running HSPICE simulations for CNFET, FinFET and sub-threshold CMOS circuits. Recently developed analytical models for InAs-based gate-all-around (GAA) TFET circuits are used to estimate driver output resistance and receiver input capacitance in TFET circuits. To perform a fair comparison, we assume a CNFET inverter that is 5× the minimum size as the driver. The number of fins in a FinFET and the number of nanowires in a TFET are calculated such that the total width of the devices is the same as the CNFET. The fin pitch and nanowire pitch are assumed to be equal and as given in [6] for each technology node.

Table 2 summarizes the results of this analysis at the 16-nm technology node and quantifies how much interconnect resistance and capacitance per unit length impact circuit performance for various device types at short and long interconnect lengths taking FinFET devices as reference. For instance, since TFET devices have higher resistance and smaller capacitance compared to FinFET devices, the impact of the interconnect resistance in the overall circuit performance is less than that of FinFET circuits for both short and long interconnects indicated by the smaller number of checkmarks. The impact of the interconnect capacitance, however, is more pronounced for TFET circuits compared to FinFET circuits. The first three best interconnect options that maximize EDP performance at short and long interconnect lengths for each device option are tabulated in Table 2. It is shown that carbon-based interconnects can find use in various device technology options and their use becomes even more beneficial as the technology scaling continues because of the significant performance degradation of Cu/low-*k* interconnect due to size effects [19].

5. SPINTRONIC INTERCONNECTS

As researchers explore novel technologies using alternative tokens for representing information in devices, it is equally important to consider interconnection aspects of these novel technologies. While many novel technologies such as spintronics, plasmonics, photonics, phononics, spin waves, and domain walls are being researched, this section focuses on interconnects for spintronics.

Concepts of spin manipulation in semiconductors and metals through magnetic fields found a mainstream application in magnetic RAMs, while spin manipulation solely through electrical currents forms the principle of spin torque memories [22]. It is easier to envision memories where electron spin orientations in nanomagnets are used to store digital states of "1" and "0". However, a proposal of all spin logic (ASL) with built-in memory by Purdue researchers has set the stage for exploratory research in spin logic [23]. In this paper, we consider an ASL device as the prototype of a switching element in the spin domain for beyond-CMOS applications.

Non Local Spin Valve (NLSV) is the most basic element in ASL interconnects and its structure is shown in Fig. 6. The electrical current passing through the input ferromagnet (FM) and ground,

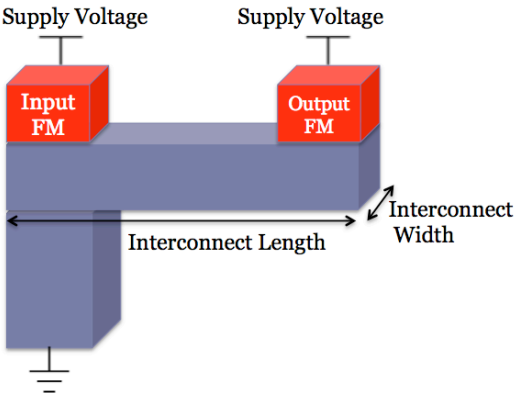

Figure 6. Non-local spin valve structure.

becomes spin polarized in which majority of electrons' magnetic moment would be aligned with the magnetic orientation of the input FM. This spin polarized current, increases the density of the electrons with the spin orientation aligned with the input FM inside the interconnect. The resulting concentration gradient for electrons based on their spin orientations inside the interconnect creates a diffusive spin current towards the output magnet. Spin torque transfer effect causes a torque applied to the output magnet that it can flip the output ferromagnet magnetization to align it with the spin orientation of the majority electrons.

Various materials may be utilized to implement the channel in ASL such as metals (Cu and Al), semiconductors (Si and GaAs), and graphene [24]. However, the channel is typically implemented in metals, since metals allow for an easier spin injection through the transmitting nanomagnet.

5.1 Size Effects

Size effects caused by extra scattering at surface and grain boundaries affect several important parameters for ASL interconnects including resistivity, diffusion coefficient, and spin relaxation length. Among these factors, spin relaxation length is the most important factor since signal attenuates exponentially as interconnect becomes longer than the spin relaxation length. In metals, the dominant spin relaxation mechanism is the Elliott-Yafet (EY) mechanism in which every time an electron is scattered, there is a certain probability that it may lose its spin information [34]. Hence, spin relaxation time is proportional to momentum relaxation time, which gets shorter as interconnect cross-sectional dimensions become smaller, due to size effects. The models for spin relaxation time and spin diffusion length are presented in [24] and Fig. 7 shows how spin relaxation length decreases as interconnect dimensions scale.

5.2 Interconnect Performance

To model an ASL interconnect, one needs to account for the dynamics of the magnet, electronic and spintronic transport through magnet to non-magnet interfaces, electric currents, and spin diffusion. Magnet orientation and electron spin are both vectors and therefore need to be represented in terms of their x, y, and z components. A comprehensive equivalent circuit model that captures all these effects has been developed in [26].

Switching delay has been plotted versus interconnect length in Fig. 8. The widths of the interconnect and the ferromagnets are assumed to be the same as the FM and equal to 37.8 nm. Supply voltage is assumed to be 80 mV. Two cases are compared, the

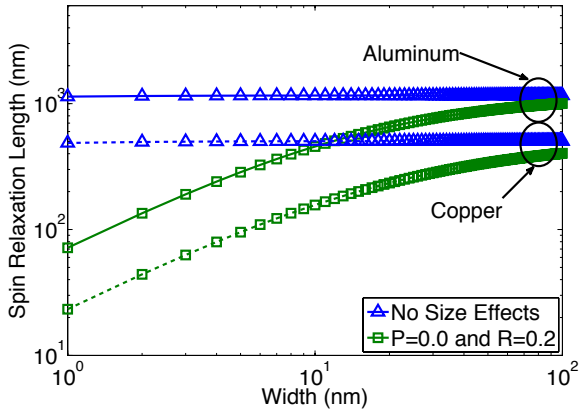

Figure 7. Spin relaxation is plotted versus the interconnect width [24, 29]. Size effects cause the spin relaxation length to decrease with decreasing channel width. If size effects are ignored, spin relaxation length does not depend on the width of the interconnect.

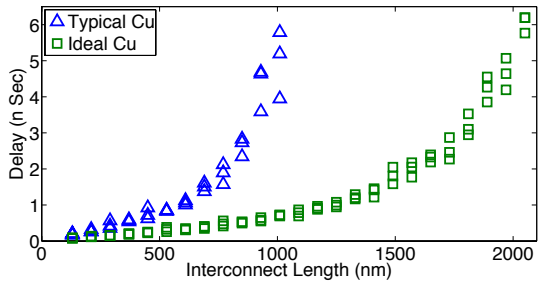

Figure 8. ASL delay versus the interconnect length. Interconnect dimensions are 37.8 nm and 18.9 nm. [29]

ideal case, in which size effects are absent, therefore size effect parameters are R=0, P=1.0, and also a typical case is assumed in which R=0.2, P=0.0. Due to the stochastic nature of thermal noise, simulations for each length are repeated three times considering room temperature.

For a 1μm long interconnect, size effects increase delay by 9 times, and it can be seen that size effects increase the delay of ASL interconnects significantly if interconnects are longer than a few hundred nanometers. This result indicates that size effects are going to impose even more severe limitations on spin diffusion based interconnects and highlights the need for using these interconnects only for short local interconnects.

6. CONCLUSION

Interconnects have been an ever growing challenge facing gigascale integration. Evolutionary solutions such as using subtractive processes to achieve larger grain sizes and using Al wires only for short signal interconnects can potentially offer major advantages as copper resistivity rises with scaling and integration of lower-k dielectrics pose major reliability issues. More radical solutions include the use of carbon-based interconnects such as CNTs and GNRs. However, major breakthroughs in placement and alignment of CNTs and in patterning GNRs with smooth edges and making reliable low-resistance contacts are needed. It is predicted that spin diffusion interconnects will suffer from size effects even more seriously as

compared to their electrical counterparts. This is due to the exponential drop in spin signal as spin relaxation length degrades due to size effects. Thereby, any improvement in Cu interconnect technology such as an increase in average grain size or replacing short signal Cu wires with Al wires will have an even bigger impact on beyond-CMOS spin diffusion interconnects.

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