# Wideband Inductorless Minimal Area RF Front-End

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***Abstract*— This paper presents the design of a fully integrated inductorless wideband RF front-end for wireless applications including WLAN, Bluetooth and UWB. The core of the circuit is comprised of a two stage LNA, followed by a standard Gilbert cell mixer and an output buffer for measurement purposes. The chip was fabricated in 65nm standard CMOS process. The RX offers an input matching of better than -10 dB in a bandwidth from 2.1 GHz to 8.2 GHz. To compensate the gain roll off the LNA incorporates an active inductor load, leading to a peak conversion gain of 20 dB at 3.5 GHz with a 3-dB bandwidth covering the whole matching frequency range. The minimal noise figure is 5.85 dB and kept below 7.5 dB within the whole matching and gain bandwidth. The linearity in terms of $P_{1dB,out}$ and oIP3 offers nearly constant behavior with -2 dBm and 7 dBm respectively. Excluding the buffer the circuit dissipates 47 mW. The die size of 370 $\mu$m by 570 $\mu$m is mainly dominated by the pad-frame, while the active area takes up only 0.05 mm$^2$.**

## I. Introduction

Since the FCC has allocated 7.5 GHz of unlicensed bandwidth for low power high data rate WPANs and high precision positioning systems the race towards the design of ultra-wideband (UWB) receivers had begun. The allowed transmit power level of only -41.2 dBm/MHz as well as state of the art deep-submicron CMOS technology allows for low power, low cost system-on-chip (SOC) solutions. Compared to traditional narrowband systems, design of UWB receivers is quite different and challenging due to the huge operational bandwidth and the low signal power levels. Furthermore the existing tradeoff concerning gain, linearity, noise and power consumption becomes even more critical in nowadays deep-submicron CMOS technologies with very low supply voltages, e.g. 1.2 V in 65nm.

Although WiMedia has mainly specified the circuit requirements for so called mandatory Mode 1 operation (BG1: 3 to 5 GHz), a lot of work has been done on RX front-ends aiming for fullband operation or at least BG1 to BG3 (3 to 8 GHz), serving as universal radio, due to the nonconform regulatory obligations. Beside conventional topologies, e.g. in [1], [2], covering BG 1,2,3, numerous different approaches have been proposed, such as a BiCMOS or a distributed front-end for fullband operation in [3] and [4], respectively, or selective designs with notch filter [5] as well as a two path solution [6]. Furthermore a front-end for BG 1,2,3 reception applying the heterodyne mixing principle has been proposed in [7]. The main disadvantage of the published wideband circuits is the use of passive inductors (except [7]), leading to a large chip area. Due to the fact that UWB will only be an additional application in nowadays wireless multi-standard handhelds, the design of an inductorless RF front-end is of great importance to keep die size and cost as low as possible. Therefore this paper focuses on the design of an inductorless RF front-end with competitive performance compared to already published work.

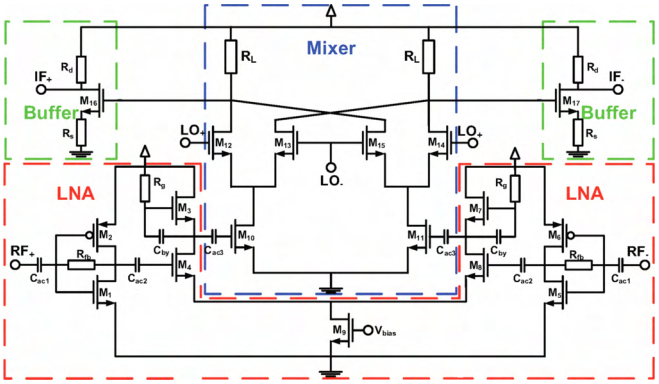


Fig. 1. Circuit schematic of the proposed differential wideband RF front-end

The paper is organized as follows: Section II focuses on the RX circuit implementation. Here, Section II-A introduces the proposed wideband LNA with a detailed explanation of its distinct two stages. Furthermore the functional principle of the source follower based active inductor for gain roll off compensation is highlighted. In Section II-B a brief description of the implemented standard Gilbert cell down-conversion mixer is given. The obtained measurement results of the bonded chip, in terms of input matching, conversion gain, noise figure and linearity, will be presented in Section III. Finally the paper will close with a summary and a performance comparison with already published RF front-ends in Section IV.

## II. RX Circuit Topology

### A. Low Noise Amplifier

The circuit schematic of the proposed AC-coupled differential LNA, depicted in the red box of Fig. 1, is shown in Fig. 2. It is comprised of two stages, whereby the first one is a shunt feedback amplifier ($M_1$,$M_2$,$M_5$,$M_6$), being responsible for the input matching. The equation for the input impedance of such

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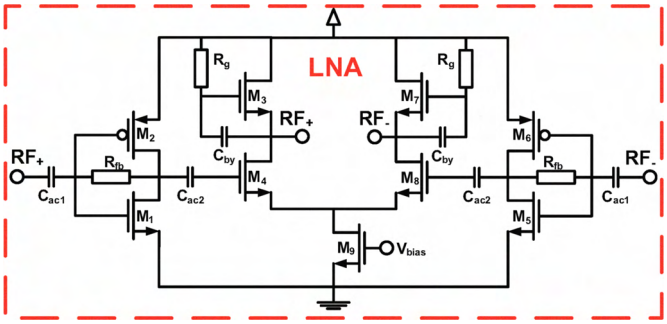



Fig. 2. Circuit schematic of the proposed two stage wideband LNA

a stage is given by

$$Z_{in} = \frac{R_{fb} + (r_{ds}||R_l)}{1 + g_m(r_{ds}||R_l)}. \quad (1)$$

Here $R_{fb}$ is the feedback resistor, $g_m$ and $r_{ds}$ are the MOS device transconductance and channel resistance, respectively, and $R_l$ is the load resistance. Moreover the corresponding voltage gain of a feedback amplifier can be expressed as

$$A_V = \frac{1 - g_m R_{fb}}{1 + \frac{R_{fb}}{(r_{ds}||R_l)}}. \quad (2)$$

These two equations reveal the need for a high ohmic load resistor $R_l$ to maximize the gain, while simultaneously reducing the number of parameters to adjust the input impedance. A feasible way to achieve this, is to apply the so called current reuse technique. A typical approach of such a stage is comprised of stacked NMOS PMOS transistors ($M_1$,$M_2$ and $M_5$,$M_6$). This inverter circuit offers the most efficient way to maximize the transconductance by a fixed DC current, $g_{m,INV} = g_{m,n} + g_{m,p}$, while the load resistor is only determined by the parallel connection of $r_{ds,n}$ and $r_{ds,p}$, leading to nearly intrinsic gain, $A_{V0} = -g_{m,INV}(r_{ds,n}||r_{ds,p})$. Moreover the biasing of the circuit is relaxed by the use of pure resistive shunt feedback, which offers so called self-biasing conditions. Furthermore a tradeoff concerning the proper choice of the feedback resistor has to be payed attention to. Considering gain and noise aspects, $R_{fb}$ should be as high as possible, whereas this will lead to problems considering the input matching (see (1)). Here, the underlying technology node determines the upper and lower limit of $R_{fb}$. To achieve adequate matching of better than -10 dB at 50 Ω source impedance, the corresponding input impedance of the circuit has to be within the range of 25 Ω and 100 Ω. Solving (1), with respect to these values as well as the intrinsic gain of the underlying 65 nm technology, leads to a lower and upper limit of approximately $175\,\Omega < R_{fb} < 700\,\Omega$. The second stage of the LNA, that is AC-coupled to the output node of the first stage via $C_{ac2}$, is a classical differential pair ($M_4$,$M_8$) with current source ($M_9$), offering a common mode suppression to increase the all over stability of the circuit. Although this is a quite current consuming topology, this circuit was preferred to a cascode stage due to the increased stability with respect to common mode oscillation as well as the required DC potential at the output node. This potential is dominated by the load, because instead of simple

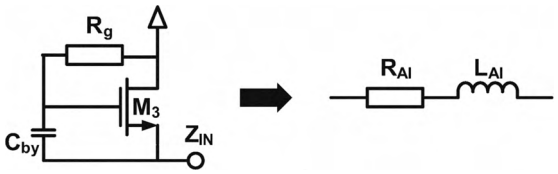



Fig. 3. Source follower based active inductor and its equivalent circuit

resistive loads, transistor $M_3$ and $M_7$ in conjuction with $R_g$ and $C_{by}$ were applied, serving as basic active inductor [8] to compensate the gain roll off at higher frequencies. For a propper setting of the required inductance value and quality factor, 600 mV to 650 mV at the source of $M_3$ and $M_7$ were needed, leading to some problems concerning the design of an adequate cascode stage operating under a supply voltage of 1.2 V only.

The single ended circuit schematic of the active inductor is shown in Fig. 3. This is a slightly modified version of the well known source follower based topology. Here, an additional external bypass capacitance $C_{by}$ has been added to get a better control of the resulting inductance $L_{AI}$ and the corresponding series resistance $R_{AI}$. The simplified input impedance at higher frequencies seen at the source of $M_3$ can be expressed as follows:

$$Z_{in,AI} = R_{AI} + sL_{AI} = \frac{1}{g_m} + \frac{sR_g(C_{gs} + C_{by})}{g_m} \quad (3)$$

(3) reveals that the use of the bypass capacitance $C_{by}$ allows for more design freedom. This is a quite interesting issue, because this modification allows for more tuning possibilities, whereas the inductance is somehow decoupled from the resistive losses, represented by $R_{AI}$ and vice versa.

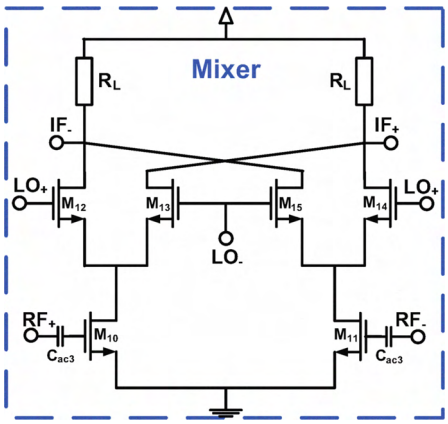


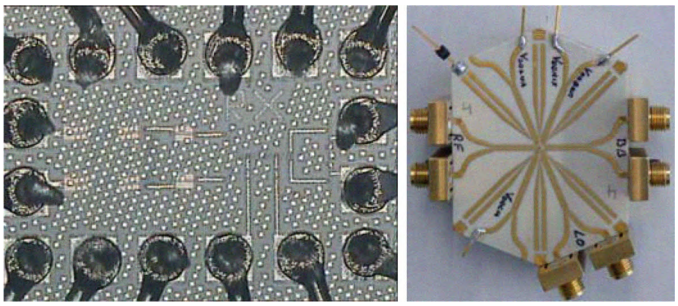

Fig. 4. Gilbert cell down-conversion mixer

### B. Mixer

The mixer circuit applied within the proposed RX is a standard Gilbert cell depicted in Fig. 4, which is AC-coupled to the LNA by $C_{ac3}$. The basic three stage design consists of a RF transconductance stage ($M_{10}$, $M_{11}$), the switching quads ($M_{12}$ to $M_{15}$) as well as an IF load represented by $R_L$. During the front-end design the focus was mainly set on the wideband LNA and on the inductorless issue. Therefore the use of a standard Gilbert mixer without any tuning coils is not the optimal choice to break the existing design trade-off in terms of conversion gain, noise figure and linearity,

mainly influenced by the biasing current [9] (e.g. by current bleeding). Especially the linearity of the circuit is negatively influenced by the chosen topology. Furthermore due to the direct conversion mixing principle, the IF output of the mixer is DC-coupled to a simple output buffer for measurement purposes ($M_{16}$, $M_{17}$, $R_d$ and $R_s$, green box in Fig. 1). This buffer slightly decreases the all over performance of the front-end.

## III. Measurement Results



(a) (b)

Fig. 5. Chipphoto of the fabricated wideband RX: (a) On-wafer and (b) On-board mounted measurement setup

Fig. 5(a) shows the on-wafer chip micrograph of the RF front-end. The circuit has been fabricated in a standard 65nm CMOS process with 1 poly layer, 6 Cu layers and one Al pad top level. The die size of 370 $\mu$m by 570 $\mu$m (0.21 mm$^2$) is determined by the pad frame and not by the active area, which only takes up a fraction of approximately 0.05 mm$^2$. The chip was mounted on a RO4003 board with SMA connectors as illustrated in Fig. 5(b).

Fig. 6 shows the RX performance in terms of input matching and conversion gain of the bonded chip. The input matching, provided by the inverter stage of the LNA reveals a return loss of better than -10 dB from 2.1 GHz up to 8.2 GHz. The dip within the $S_{11}$ characteristic at about 9.5 GHz is mainly based on a resonance of the PCB and the chip parasitics. The measured conversion gain exhibits a flat frequency response with a peak value of 20 dB at 3.5 GHz. The 3-dB bandwidth can be determined to 8.5 GHz and lies within the matching bandwidth.

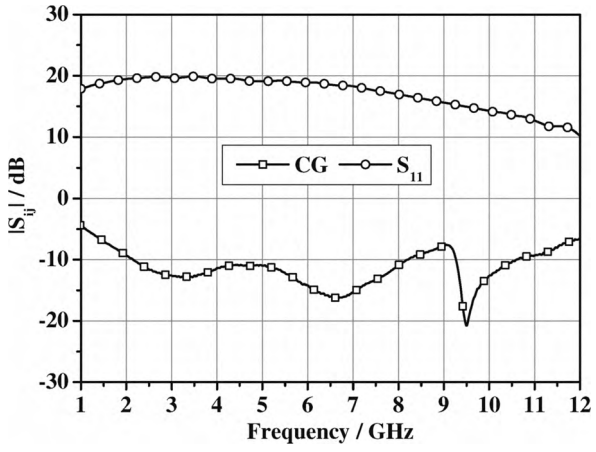



Fig. 6. Inputmatching and CG over frequency

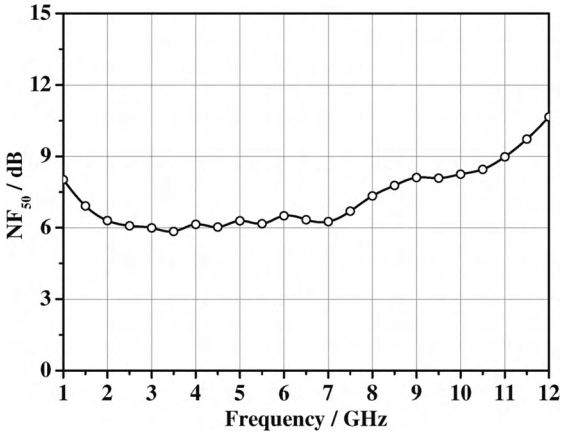



Fig. 7. Noise figure over frequency

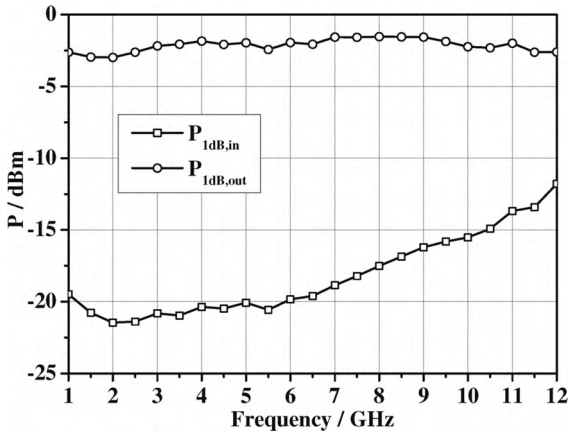



Fig. 8. Input and output referred compression point over frequency

The measured NF is illustrated in Fig. 7 and reveals a minimum of 5.85 dB at 3.5 GHz. Within the whole operational bandwidth, the RX noise figure is kept below 7.5 dB. This noise performance can be seen as adequate compared to the requested 6.6 dB specified by WiMedia for Mode 1 operation. Finally the results concerning the circuit linearity in terms of compression point and intermodulation distortion are investigated. Fig. 8 shows the input and output referred compression point of the front-end. The linearity in terms of $P_{in,1dB}$ increases from -21.5 dBm at 2 GHz up to -16.85 dBm at 8.5 GHz, while the $P_{out,1dB}$ shows nearly constant behavior with a mean value of approximately -2 dBm.

Qualitatively the same behavior can be observed for the iIP3 and oIP3. Fig. 9(a) and Fig. 9(b) show the measurement results for the two tone in-band intermodulation distortion at 3.5 GHz (maximum in gain) and 6.5 GHz (center frequency of whole UWB spectrum), with 1 MHz tone spacing. The complete IP3 performance versus frequency is given in Fig. 10. Here the iIP3 ranges from -11.9 dBm at 3.5 GHz up to -8.3 dBm at 8.5 GHz, whereas the oIP3 is constant at about +7 dBm. All in all the linearity of the circuit shows feasible behavior, although there is still some need for optimization, especially considering the linearity dominating last stage in terms of the mixer.

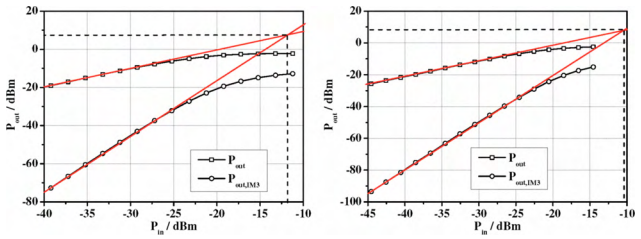
The performance summary in Tab. I compares the proposed topology to previous reported UWB front-ends. In terms of input matching as well as gain bandwidth the circuit covers

TABLE I

PERFORMANCE SUMMARY

| Work | BG | $G_{max}$ / dB | NF / dB | $P_{1dB}$ / dBm | iIP3 / dBm | $S_{11}$ / dB | $P_{DC}$ / mW | Area / mm$^2$ | Techn. /$\mu$m |
|---|---|---|---|---|---|---|---|---|---|
| **[1]**$^{+}$ | 1,2,3 | 32.3 | 6.51-7.87 | >-24.5 | >-12.6 | <-13 | 33.75 | 7.25 (100%) | 0.18 |
| **[2]**$^{*}$ | 1,2,3 | 21.5 | 4.3-6.2 | — | >-17 | <-10 | 19.25 | 1.16 (16%) | 0.18 |
| **[3]**$^{\circ}$ | 1,2,3 | 21.8 | 4.1-6.2 | -23.5 | -12.7 | <-5 | 83.7 | 1.1 (14%) | 0.25 |
| **[4]** | 1,2,3,4,5 | 15.5 | 5.2-5.4 | >-15.5 | -6.6 | <-10 | 14.8 | 1.5 (21%) | 0.13 |
| **[5]** | 1,3 | 23.2 | 5.2-7.7 | >-12.5 | >-3.5 | <-9 | 18 | 1.7 (23%) | 0.18 |
| **[6]** | 1,3 | 26.1 | 4.9-7.7 | >-28.8 | >-20.1 | <-9 | 57.72 | 0.73 (10%) | 0.13 |
| **[7]** | 1,2,3 | 21 | 5-6.57 | — | >-5.6 | — | 44.85 | 0.35 (5%) | 0.18 |
| **[10]** | 1 | 22 | 3.3-4 | >-23 | >-14 | <-10 | 21.6 | 1.65 (23%) | 0.13 |
| **[11]** | 1 | 25.5 | 4.5-6 | — | >-14.9 | <-10 | 47.34 | 0.48 (7%) | 0.18 |
| **This Work** | 1,2,3 | 20 | 5.85-7.5 | >-20.5 | >-12 | <-10 | 47 | 0.05 (0.7%) | 0.065 |

$^{+}$incl. Synth. and Div. $^{*}$Sim. only $^{\circ}$BiCMOS




(a) (b)

Fig. 9. Measured and extrapolated iIP3/oIP3 at (a) 3.5 GHz and (b) 6.5 GHz

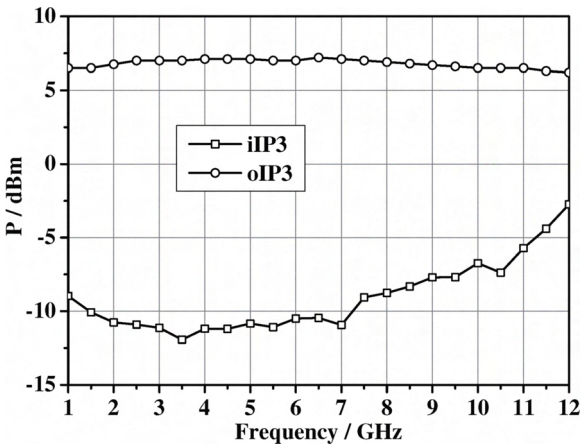



Fig. 10. Input and output referred intercept point over frequency

BG 1,2,3 with an equivalent peak gain compared to the other front-ends. Considering the noise figure, the presented circuit shows good performance, slightly outperformed by [2], [3] and [4] as well as the BG 1 designs [10],[11]. The linearity reveals quite feasible and competative values, even higher than the BG 1 approaches. The power dissipation of 47 mW, mainly dominated by the LNA, seems to be quite high compared to the other designs, which are IQ-based. Nevertheless this is still a manageable value with respect to the fact, that a second mixer stage for the I or Q path would only consume approximately 2 mW. The main advantage of the proposed circuit is the occupied die area, that takes up only 15% of the smallest reference circuit in Tab. I (see [7]).

## IV. CONCLUSION

This work has presented the design of a wideband RF front-end, while the focus was set on an inductorless approach, occupying minimal chip area. The front-end, incorporating a two stage LNA with inverter input stage and source follower based active inductor for gain roll off compensation, has shown very good allover performance with respect to UWB BG 1,2,3. Summarized it can be stated, that the presented wideband RF front-end seems to be an attractive solution for wireless UWB applications, compared to already published state-of-the-art topologies. Additionally the circuit covers the WLAN and Bluetooth frequencies, which is quite interesting in terms of multi-stadard receivers.

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