Experiences With Non-Intrusive Sensors For RF Built-In Test

Louay Abdallah*, Haralampos-G. Stratigopoulos*, Salvador Mir*, and Christophe Kelma†
*TIMA Laboratory (CNRS-Grenoble INP-UJF), 46 Av. Félix Viallet, 38031 Grenoble, France
†NXP Semiconductors, 2 esplanade Anton Philips, Campus Effiscience, Colombelles BP20000, 14906 Caen, France

***Abstract*— This paper discusses a new type of sensors to enable a built-in test in RF circuits. The proposed sensors provide DC or low-frequency measurements, thus they can reduce drastically the testing cost. Their key characteristic is that they are non-intrusive, e.g. they are not connected electrically to the RF circuit. Thus, the performances of the RF circuit are unaffected by the monitoring operation. The sensors function as process monitors and share the same environment with the RF circuit. The underlying principle is that the sensors and the RF circuit are subject to the same process variations, thus shifts in the performances of the RF circuit can be inferred implicitly by shifts in the outputs of the sensors. We present experimental results on fabricated samples that include an LNA with embedded sensors. The samples are collected from different sites of a wafer such that they exhibit process variations. We demonstrate that the performances of the RF circuit can be predicted with sufficient accuracy through the sensors by employing the alternate test paradigm.**

I. Introduction

Testing the RF functions of a System-on-Chip is responsible for the largest fraction of the overall test cost. RF test is very challenging since high-frequency signals are needed to be extracted off-chip with minimum impairment. In addition, there is a large variety of specifications that need to be verified, requiring sequential tests on different test configurations, which results in lengthy switching and settling times, other than the pure electrical test times. In turn, these tests need to be carried out in an environment that is shielded from electromagnetic interference and noise and, furthermore, with regards to the Automatic Test Equipment (ATE), there are stringent requirements for wide frequency range and high linearity.

To alleviate the dependency on sophisticated ATE, it has been proposed to perform an RF-DC conversion on the test board [1]. However, the design and debugging of such test boards can turn out to be a complex task and the overall benefit reduces if the load board is not reusable. A more aggressive approach for test cost reduction is built-in test which consists of performing on-chip some of the test operations, e.g. stimulus generation, measurement extraction and analysis, etc. Built-in test can reduce dramatically the complexity of ATE since it provides digital, DC, or low frequency test signatures, it resolves issues related to electromagnetic interference, it facilitates parallel testing to achieve a high throughput, etc. The main challenges are to maintain a low overhead, to avoid degradation of the performances of the circuit under test (CUT), and to preserve the test accuracy of the standard test approach. Examples of built-in test strategies include loopback test where the transmitter "tests" the receiver [2], [3], [4], [5], oscillation test where the CUT is forced to oscillate and the oscillation frequency is used as an information-rich test signature [6], [7], DC probes to monitor internal nodes of the CUT [8], and sensors to extract low-cost alternative measurements from the CUT that carry RF information. Different sensors have been studied in this context, including envelope detectors [9], [10], [11], power detectors [12], and current sensors [13], [14]. The outputs of the sensors can be used to make a direct Go/No-Go test decision or they can be mapped to the performances based on the alternate test paradigm [15], [16].

The common characteristic of these built-in test strategies is that they degrade the performance of the CUT unless they are carefully co-designed with it. In particular, loopback test requires the addition of RF switches and an attenuator in the signal path, in order to connect the transmitter's output to the receiver's input, oscillation test requires reconfiguring the CUT into an oscillator by adding positive feedback, while DC probes and sensors tap into the signal path of the CUT. In all cases, the impedance matching and the overall performance is degraded requiring co-design. For this reason, designers are rather reluctant to incorporate such built-in test capabilities since the design specifications are stringent and exploit the full capabilities of the technology.

In this work, we envision the scenario shown in Fig. 1, where the sensors are non-intrusive, e.g. they are not connected electrically to the CUT and, thereby, they do not require co-design. The sensors can be either activated on-chip or by applying an external stimulus. The stimuli and the output measurements are digital, DC, or low-frequency, thus a multiplexer and a demultiplexer can be used to occupy only two pins for test purposes. For the sensors that we are studying in this work, it is not required to power on the CUT. The sensors can be of two types, namely dummy circuits and process control monitors (PCMs). Dummy circuits consist of basic analog stages, i.e. current mirrors, gain stages, level shifters, etc., while PCMs consist of basic layout components, i.e. capacitors, transistors, etc. Typically, process variation sensors are accommodated in standard macros that are placed in the scribe lines and are thrown away after dicing. They are used to identify off-target process parameters throughout wafer processing and to study variability [17], [18], [19]. Herein, the sensors are placed instead in close proximity to the CUT. Their operation capitalizes on the undesired phenomenon of

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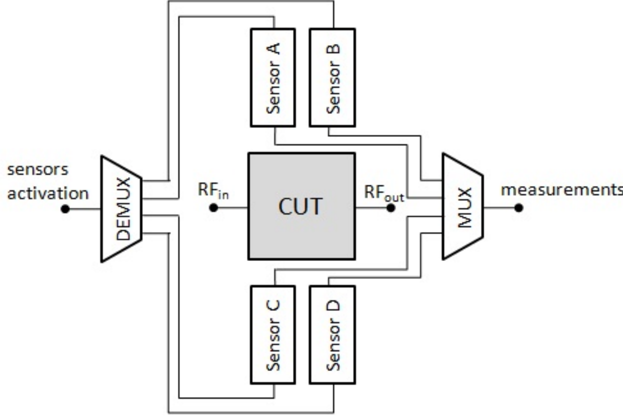

Fig. 1. Circuit with embedded non-intrusive sensors that enable a built-in test.

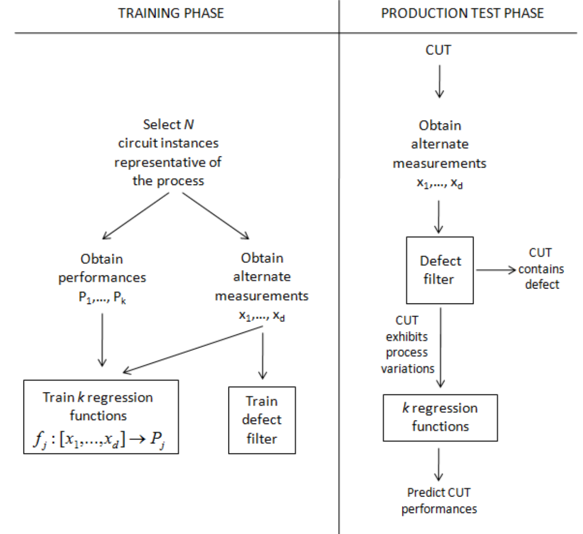

Fig. 2. Alternate test flow.

inter-die process variations. In particular, by virtue of being in close proximity to the CUT, they will be subjected to the same process variations, thus we expect that any shifts in the performances of the CUT will be reflected in the outputs of the sensors. A similar approach was used to monitor sources of error in multi-step ADCs [20]. In a previous paper [21], we demonstrated through post-layout simulations that this approach can be used for predicting the performances of an RF LNA. Herein, we prove for the first time the feasibility of the approach using real measurements on fabricated samples.

Specifically, we designed an LNA with embedded non-intrusive sensors using the 0.25 μm Qubic4+ BiCMOS process by NXP Semiconductors. We fabricated in total 142 samples that were distributed evenly across a wafer. The samples exhibited inter-die variations which allowed us to build the mapping between the outputs of the sensors and the performances of the LNA based on the alternate test paradigm. For this purpose, we used different regression tools, namely feed-forward neural networks (FFNN) and multivariate adaptive regression splines (MARS). We report the mean and worst case error that we commit by predicting the performances of the LNA from sensor measurements. To report a faithful error, we use techniques such as k-fold cross-validation and averaging of the error over different random splits of the samples into training and test sets.

The rest of the paper is structured as follows. Next, we provide a quick overview of the alternate test and we show how the proposed sensors can be used in this context. Section III describes the principle of operation of the sensors. Section IV presents the different sensors that are used for monitoring the LNA. Section V presents details about the fabricated chip and the measurement environment. Section VI discusses the regression techniques and the estimation of prediction errors. Section VII presents the results of the experiment. Section VIII concludes the paper and gives directions for future work.

II. Test approach based on non-intrusive sensors

Let $P_1, \cdots, P_k$ denote the k performances of the CUT that need to be measured during the standard test approach. Let also $X = [x_1, \cdots, x_d]$ denote a pattern of d alternative measurements, e.g. the measurements provided by the sensors in our case. The alternate test paradigm is used to predict the outcome of the standard test approach based solely on X [15], [16], as shown in Fig. 2. Alternate test requires an off-line, preparatory training phase to build the mappings between X and each performance. Let f_j denote the mapping between X and performance P_j, e.g.

$$f_j \ : \ X \to P_j, \quad j = 1, \cdots, k. \tag{1}$$

In the training phase, we collect N circuit instances from different lots, wafers, and sites on the same wafer, such that they are representative of the process variations that may occur. Let X^i and P_j^i denote respectively the alternate measurements and the j-th performance of the i-th instance, $i = 1, \cdots, N$. The pairs $\{X^i, P_j^i\}$ are split into training and test sets. The training set is used to learn the regression function f_j while the test set is used as an independent set to assess the error in predicting the performance P_j from X using f_j. If the set of measurements X yields a low prediction error, the learnt regression functions can be used to provide a fast, low-cost test for new instances coming out of the production line.

The regression functions should be applied only to instances that exhibit process variations and, in particular, to instances whose measurement pattern is within the range defined by the measurement patterns of the instances in the training set. Otherwise, the prediction will be somewhat random. Thus, a defect filter is used to distinguish instances that exhibit process variations from instances that contain defects. In [22], a defect filter based on non-parametric density estimation is proposed. It has the attractive property that it operates as an one-class classifier, that is, it is trained using the alternate measurement patterns of the instances in the training set and no information about defects is required. The instances with process variations

constitute the majority of instances that we will be seen in production, hence the large benefit of alternate test.

The sensors proposed in this work provide a low-cost alternate measurement pattern from which the performances can be predicted with high accuracy. However, they cannot indicate the presence of a defect within the CUT since they are not electrically connected to it. In fact, the test is performed without powering on the CUT. In other words, the proposed sensors provide a measurement pattern that cannot serve as an input to the defect filter. Therefore, more measurements are needed to ensure that the CUT does not contain a defect before applying the regression functions to predict the performances. In [23], a non-intrusive temperature sensor is presented and it is demonstrated that it can detect all defects injected in an LNA. In short, when the CUT is operating, it is self-heated due to its power consumption and, thereby, the temperature in its vicinity changes. If there is a defect in the CUT, then the dissipated power will shift from the expected range of nominal values and this shift will be captured by the temperature sensor through a temperature change. For more details, the interested reader is referred to [23]. The focus of this paper is on non-intrusive sensors to implement the mappings in (1).

III. UNDERLYING PRINCIPLE

During the several manufacturing steps of an integrated circuit, different process parameters may drift from their nominal values, such as the effective channel length, the oxide thickness, the dopant concentration, the transistor width, the inter-layer dielectric thickness, etc. Variations in the process parameters stem from different sources, including lens imperfections, proximity effects, temperature gradients, misalignment of masks, etc. According to their physical range on a die or wafer, variations can be classified into two categories [24]:

- *Die-to-die* (D2D) variations (or inter-die variations): correspond to smooth and slow-varying variations that affect all devices on a die in the same way, i.e. they cause the gate lengths of identical transistors to be all larger or all smaller. D2D variations present a large degree of spatial correlation, that is, neighboring devices on the same die are similarly affected. They include across-wafer, wafer-to-wafer, and lot-to-lot variations. Across-wafer variations reflect spatial characteristics of the process while wafer-to-wafer and lot-to-lot variations reflect both spatial and temporal characteristics of the process.
- *Within-die* (WID) variations (or intra-die variations): correspond to variations rapidly varying over distances smaller than the die dimension. Thus, WID variations can affect differently identical devices that are placed at different locations on the same die, i.e. they cause identical transistors to have smaller or larger gate lengths. It is important to stress that WID variations for some process parameters, such as the effective channel length, show a degree of local spatial correlation.

Consider now sensors such as dummy circuits and PCMs that mimic part of the topology of the CUT and they are placed in close proximity to the CUT. Based on the above discussion, the variation in a performance P_j of the CUT, denoted by ΔP_j, and the variation in the measurement pattern from such sensors, denoted by ΔX, can be expressed as

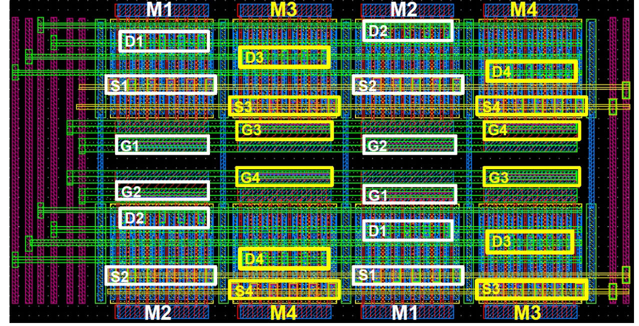

Fig. 3. Example of layout technique to match two current mirrors that are not electrically connected.

$$\Delta P_j = f_1(\Delta p) + r_1 \quad (2)$$

$$\Delta X = f_2(\Delta p) + r_2. \quad (3)$$

where p is the vector of process parameters, Δp is the vector of D2D and WID spatially correlated variations in process parameters, f_1 and f_2 are non-linear functions, and r_1 and r_2 correspond to WID uncorrelated variations. The premise of this work is that variations ΔP_j and ΔX are correlated since they are both subject to Δp and that this correlation is not appreciably affected by r_1 and r_2. Under this scenario, we expect that we can track shifts in P_j by monitoring shifts in X, that is, it is possible to draw a regression function f_j, such that $f_j(X) \simeq P_j$.

The WID uncorrelated variations should be seen principally as a challenge in analog design where it is often required to match two components, i.e. the transistors in a current mirror, the transistors in the input stage of a differential LNA or mixer, the sampling and integrating capacitors in a pipeline ADC, etc. If matching techniques can be applied to achieve satisfactory performance, then the negative effect of r_1 and r_2 in the correlation can be reduced given that the sensors are basic analog stages and layout components that mimic part of the topology of the CUT and, thus, they can be matched to the corresponding stages and components of the CUT. For example, Fig. 3 shows the layout of two matched current mirrors formed respectively by M_1, M_2 and M_3, M_4 that are not electrically connected. D_i, S_i, G_i refer to the drain, source, and gate, respectively, of transistor M_i. Such matched current mirrors are used, for example, in the design of fully differential amplifiers. It should be noted also that the effect of r_1 and r_2 in the correlation is expected to grow large as we move below 100 nm. However, recent studies have shown that D2D variations are still responsible for the largest part of performance variations for 65 nm and 90 nm technologies [25], [26]. Finally, the use of alternate test moderates the residual prediction error that results from random variations

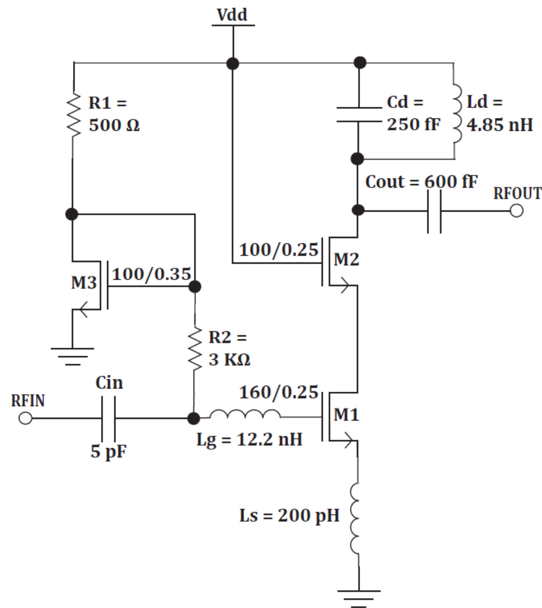

Fig. 4. CMOS inductive degenerated cascode LNA.

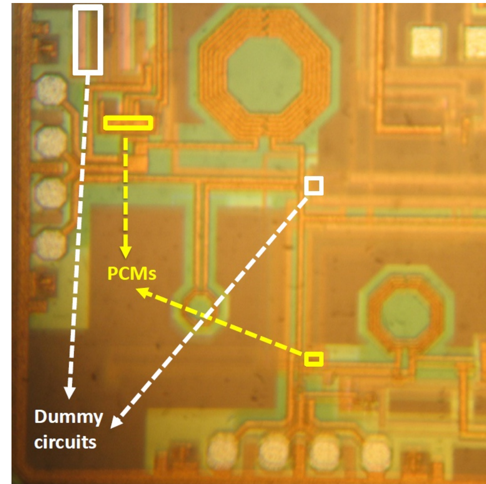

Fig. 5. Photo of the fabricated chip showing the LNA with the embedded dummy circuits and PCMs.

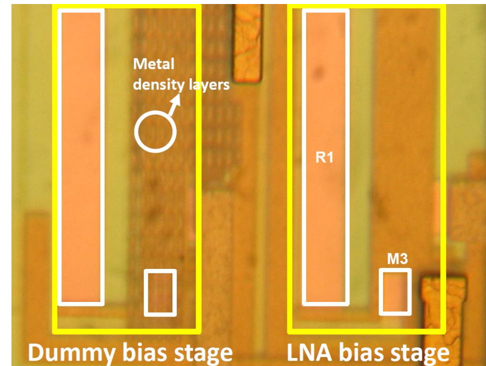

Fig. 6. Photo of a dummy bias stage placed close to the bias stage of the LNA.

since the regression function is calculated in terms of an average over a random quantity.

IV. Non-Intrusive Sensors

Each deployed sensor mimics part of the architecture of the CUT. Consider the LNA of Fig. 4 which plays the role of the CUT in our study (see Section V). The sensors can include (a) a bias stage identical to the bias stage of the LNA formed by transistor M_3 and resistor R_1, (b) a current mirror whose schematic is produced by short-circuiting capacitors and inductors in Fig. 4, (c) a MOS gain stage that mimics the gain stage of the LNA formed by M_1 and cascode transistor M_2, (d) stand-alone capacitors extracted from LNA, and (e) stand-alone transistors extracted from the LNA. The geometry of the components in the sensors, i.e. the length and width of transistors, the area of capacitors, etc., matches the geometry of the corresponding components in the LNA. The sensors are placed in close proximity to the structures in the LNA that they are mimicking, in order to be subjected to similar process variations. It is expected that there will be similar variations in the values of parameters of two identical transistors (i.e. g_m, V_{th}, etc.) and in the values of two identical capacitors that are placed closely to each other. In essence, the sensors capitalize on D2D or WID spatial correlations, in order to track non-intrusively shifts in the performances of the LNA.

Fig. 5 shows a photo of the fabricated chip showing the LNA with the embedded dummy circuits (e.g. bias stage, current mirror, and gain stage) and PCMs (e.g. capacitors and transistors). The sensors do not incur any area overhead since they are placed in areas on the die that otherwise would have been left void, in order to respect design-for-manufacturability (DFM) rules. The inductances are not replicated since this would result in a large area penalty. Fig. 6 zooms in a dummy bias stage that is placed close to the bias stage of the LNA formed by resistor R_1 and transistor M_3. Notice that there are metal density layers on top of the dummy bias stage, in order to respect DFM rules. These metal density layers are added across the die except the RF areas. Fig. 7 zooms in a MOS PCM that is placed close to the transistor M_1 of the gain stage of the LNA.

A test bus based on a multiplexer and demultiplexer, as shown in Fig. 1, is used to activate sequentially the sensors and extract off-chip the measurements. The current mirrors and the bias stages are self-biased by default while the MOS gain stages are self-biased using a voltage divider. These dummy circuits provide DC measurements that correspond to voltage gain, current gain, level-shifting, etc. The capacitors and transistors require AC excitation. The capacitor values are measured by a Wheatstone bridge that is placed on the test board while the transconductance g_m of the MOS transistors is obtained by simple I-V characterization. Notice that all activations and output measurements are low-frequency or DC and that the CUT is not powered on during the test phase.

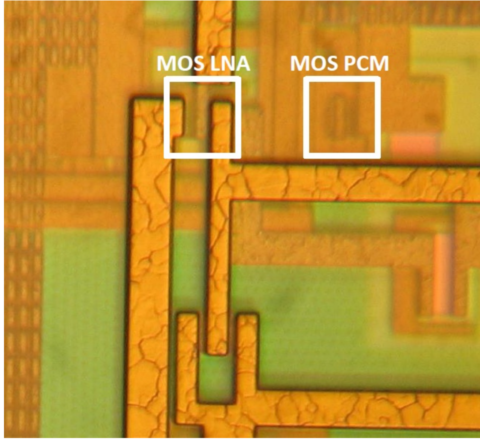

Fig. 7. Photo of a MOS PCM placed close to the transistor of the gain stage of the LNA.

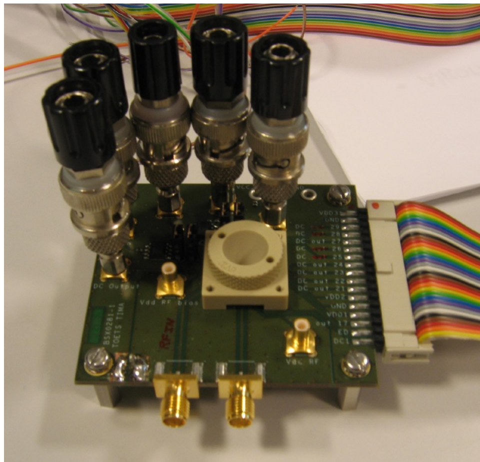

Fig. 8. Photo of the PCB used for measuring the fabricated dies.

V. Chip fabrication and Experimental Set-up

Our case study is a 2.4 GHz inductive degenerated cascode LNA, shown in Fig. 4, which is commonly used in narrow band applications such as Wi-Fi and Bluetooth. The LNA and the embedded sensors are designed using the 0.25 μm Qubic4+ BiCMOS technology by NXP Semiconductors. The design was taped out in a Multi-Project-Wafer (MPW) run. It was placed in different locations in a reticle and the reticle was reproduced over the wafer. In total, we obtained 142 packaged samples that came from different sites on a wafer.

A printed circuit board (PCB), shown in Fig. 8, was fabricated for measuring the fabricated samples. The top and bottom layers of the PCB are reserved to place and route the surface mounted devices and two intermediate layers are dedicated to the DC and RF grounds that are well isolated. The input and output RF lines are appropriately sized to have an impedance of 50 Ohms. The addition of LC matching structures was envisaged, in order to correct the mismatching of the die input and output impedances due to PCB parasitics. The PCB also contains a Wheatstone bridge for measuring capacitor values.

TABLE I

Minimum and maximum values of performances observed across the fabricated samples and measurement repeatability error.

performance	min	max	measurement repeatability error ϵ_r
Gain (in dB)	8.81	9.97	0.2
NF (in dB)	4.33	4.64	0.1
1-dB CP (in dBm)	-9.5	-7.5	0.44
IIP_3 (in dBm)	8.05	10.5	0.4

The 142 samples were fully characterized using benchtop equipment. For each sample, we measured the performances of the LNA that are typically considered in production testing, e.g. gain, noise figure (NF), 1 dB-compression point (1-dB CP), and input third-order intercept point (IIP_3), as well as the sensor outputs. The gain was measured using a vector network analyzer from Rohde and Schwarz (ZVR 1127.8551.61). The NF was measured using a noise figure meter from Agilent Technologies (N8972-90114) and a noise source from Hewlett Packard (346A). The 1-dB CP and the IIP_3 were measured using RF signal generators from Agilent Technologies (8648A) and a spectrum analyzer from Hewlett Packard (8590). The outputs of the sensors were measured using DC multimeters from Agilent Technologies (34401A). The measurement procedure was automated through Labview software using a general purpose interface bus (GPIB). Measuring the performances of the LNA requires three different test configurations while the sensor outputs are extracted using a single test configuration.

Table I shows the observed minimum and maximum values of the LNA performances across the 142 samples, as well as the measurement repeatability error ϵ_r due to the precision of the instruments and the laboratory environment. The measurement repeatability error on a sample is deduced by repeating several times the characterization. We observed that this error practically does not change across the samples, thus the values in Table I can be considered to apply to all samples. This error will be taken into account when analyzing the prediction errors of the regression models. As can be seen from Table I, there exist variations in the available samples and these variations are much larger than the measurement repeatability error. This allows us to analyze correlations that exist between the performances of the LNA and the alternate measurements provided by the sensors.

VI. Regression Tools, Error Definition, and Error Estimation

There are different regression tools that can be used to derive the regression functions $f_j(X)$ in alternate test. In this work, we use two well-known tools, namely a FFNN and MARS [27], [28], [29]. The available samples are split into a training set and a test set and the training set is split further into a learning set and a validation set. The learning set is

used for training the regression function, the validation set is used for controlling its complexity to avoid over-fitting, and the test set is used once training is over to obtain an unbiased estimate of the prediction error.

We consider a FFNN that has two hidden layers of neurons that implement a sigmoidal activation function and a third layer with a single output neuron that implements a linear function. In theory, such a FFNN with three layers of adaptive weights is capable of approximating any arbitrarily non-linear mapping $f_j(X)$. The training of the FFNN is carried out using the backpropagation algorithm. The early stopping technique is used to control the complexity of the regression function. In particular, the backpropagation algorithm uses the learning set and, in the end of each iteration, the prediction error is computed on the validation set. If the error does not reduce for a number of consecutive iterations, then it implies that over-fitting has occurred and the training stops. The model that gave the lowest error on the validation set is used. The disadvantage of a FFNN is that the optimal numbers of neurons in the hidden layers are not known in advance and need to be found through a trial and error approach. The MARS algorithm offers a more automated framework for deriving the regression functions. It uses a forward step that results in a model that typically over-fits the learning set and then a backward step that deletes terms from the model such that the final reduced model has the optimal complexity that maximizes the performance on the validation set.

The efficiency of the regression functions in alternate test is assessed according to (a) the mean error ϵ_{m} observed on the test set and (b) the maximum error ϵ_{max} observed on the test set [16]. The first criterion shows the degree of correlation while the second criterion defines the guard-band that should be placed on a predicted performance. Specifically, if $P_j^{'} = f_j(X)$ denotes the predicted value of performance P_j and assuming that P_j has lower and upper specifications $[s_j^l, s_j^u]$, then we can tell with certainty that the CUT is functional if $P_j^{'} \in [s_j^l + \epsilon_{\mathrm{max}}, s_j^u - \epsilon_{\mathrm{max}}]$. The efficiency of alternate test is deemed to be good if (a) ϵ_{m} is low and (b) ϵ_{max} is comparable with the measurement repeatability error ϵ_r in the standard test approach.

The simplest approach to estimate the errors is to split the available samples randomly into two portions, i.e. 70% in the training set and 30% in the test set. This naive strategy is based on the assumption that both the training and test sets are representative of the fabrication process. While this is usually true for a large number of samples, when the number of samples is small (which is the case in our study), the particular partitioning of the samples into training and test sets, as well as the portion of the samples that is allocated in each set, start to have an impact on the estimated prediction error. In other words, the error will present a large variance across all possible partitions. To report an error that faithfully indicates the actual degree of correlation between performances and alternate measurements, we use the following re-sampling techniques.

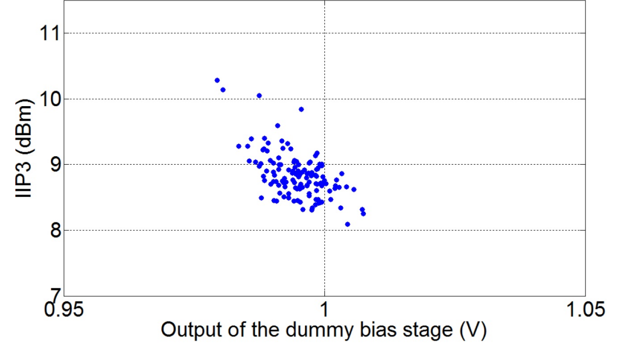

Fig. 9. IIP_3 versus the measurement on a dummy bias stage placed in proximity to the bias stage of the LNA.

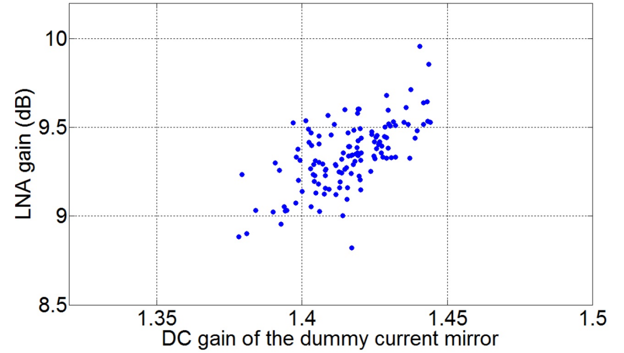

Fig. 10. LNA gain versus DC gain of a current mirror placed in proximity to the LNA.

1) Random sampling: We create several different random splits of the samples into training and test sets and we report the average error on the test set over all splits.

2) k-fold cross validation: We split the samples into k randomly selected disjoint blocks of roughly equal size. The model is trained k times where each time k-1 blocks are assigned to the training set and the remaining block is left out as a test set. Each time a different block plays the role of the test set, thus, in the end, all samples are used in both training and test sets. We finally report the average error over the k models. Typical choices for k are 5, 10, and N, where N is the number of available samples. In the latter case, the technique is called leave-one-out cross validation (LOOCV).

The above re-sampling techniques can be combined, i.e. we can apply k-fold cross validation several times using different random splits of the samples into k blocks and average the errors over all splits.

VII. Results

We first investigated one-to-one correlations between sensor measurements and performances of the LNA. Fig. 9 shows the fabricated samples projected onto the space defined by IIP_3 and the measurement on a dummy bias stage placed in proximity to the bias stage of the LNA. This correlation is expected since IIP_3 depends on the gate to source voltage of transistor M_1 which is fixed by the bias stage M3 and R1. Fig. 10 shows the correlation between the LNA gain and the

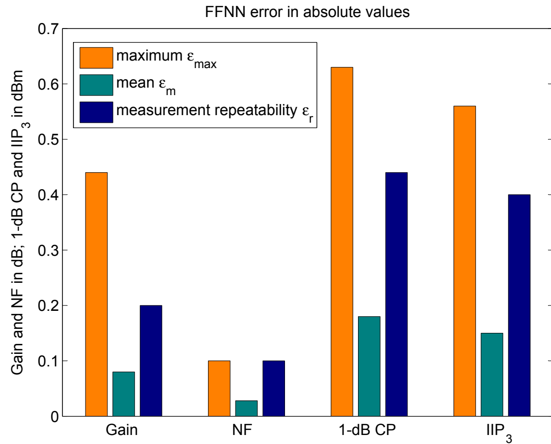

Fig. 11. Mean ϵ_m and maximum ϵ_{max} prediction errors in absolute values using a FFNN showing also the measurement repeatability error ϵ_r.

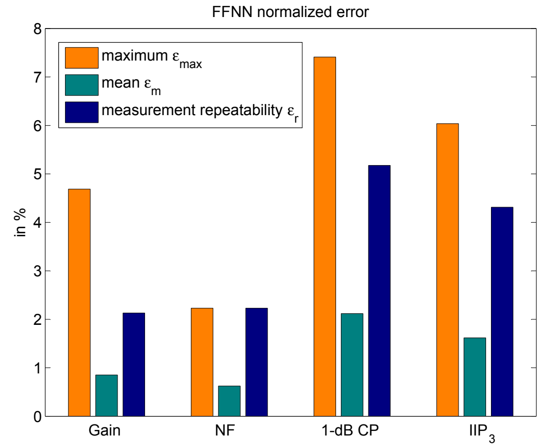

Fig. 13. Mean ϵ_m and maximum ϵ_{max} prediction errors in % using a FFNN showing also the measurement repeatability error ϵ_r.

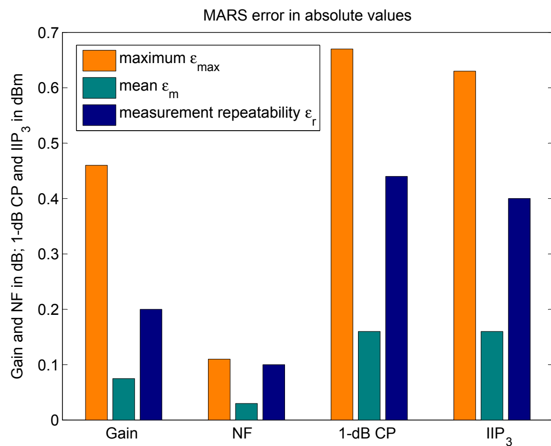

Fig. 12. Mean ϵ_m and maximum ϵ_{max} prediction errors in absolute values using MARS showing also the measurement repeatability error ϵ_r.

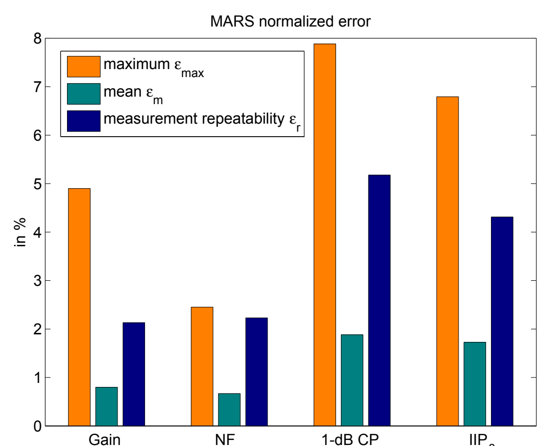

Fig. 14. Mean ϵ_m and maximum ϵ_{max} prediction errors in % using MARS showing also the measurement repeatability error ϵ_r.

DC gain of a current mirror that is placed in proximity to the LNA. The schematic of the current mirror is produced by the schematic of the LNA by short-circuiting all capacitors and inductances. This correlation is expected since both gains are principally defined by the gain of transistor M_1.

Next, we used all sensor measurements to build the regression functions in alternate test. Fig. 11 and 12 show the mean ϵ_m and maximum ϵ_{max} prediction errors in absolute values obtained using the FFNN and MARS together with the measurement repeatability error ϵ_r when measuring the performances using the standard test approach (see Section V). In Fig. 13 and 14, the errors are normalized by the median values extracted from Table I and expressed in percentage. The following observations can be made:

- The prediction errors are practically the same from a statistical point of view when using a FFNN or MARS. This shows that the accuracy of alternate test is independent of the regression tool that is being used as long as, of course, the training is done carefully to moderate the complexity of the regression model.
- The mean prediction error does not exceed 2.2% for all four performances with the NF showing the smallest mean error and the 1-dB compression point showing the largest. This shows that correlations between the performances of the LNA and the sensor measurements are very strong.
- For the gain, the measurement repeatability error is about half the maximum prediction error, whereas for the NF, 1-db CP, and IIP$_3$, this ratio is about two thirds. However, the measurement repeatability error is much larger in an ATE than when using benchtop equipment. Typical measurement repeatability error values in an ATE are larger than 1 dB for the NF and larger than 0.5 dB for gain, 1-db CP, and IIP$_3$. On the other hand, the maximum prediction error in an ATE is not expected to change since the predictions are based on DC or low-

frequency measurements. Thus, in an ATE we expect that the maximum prediction error will be comparable or even smaller than the measurement repeatability error.
- In practice, the maximum and mean prediction errors will be much lower since we will be using a larger set of samples collected across different lots, wafers, and sites on the same wafer that is more representative of the fabrication process.

Based on the above observations we consider that our findings are very promising and demonstrate that RF performances can be predicted by non-intrusive on-chip sensors.

VIII. Conclusions

In this paper, we proposed sensors for extracting low-cost test signatures from RF circuits. The key characteristic of these sensors is that they are transparent to the RF circuit and, thereby, they do not affect its performances. This is a very important attribute because the sensors can be used as plug-ins in the design without needing to resize the RF circuit to meet the performance goals. The sensors consist of basic analog stages that mimic part of the topology of the RF circuit and stand-alone layout components, such as transistors and capacitors, that are copied directly from the layout of the RF circuit. By placing the sensors in close proximity to their counterparts on the layout, we guarantee that the sensors and the RF circuit will witness similar process variations. We demonstrated in the experimental results that the sensor measurements correlate with the performances of the RF circuit, thus shifts in performances can be implicitly inferred by shifts in the sensor measurements. Future work will focus on enhancing the library of non-intrusive sensors.

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