# Can InAlN/GaN be an alternative to high power / high temperature AlGaN/GaN devices?

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## Abstract

The performance of novel AlInN/GaN HEMTs for high power / high temperature applications is discussed. With 0.25 µm gate length the highest maximum output current density of more than 2 A/mm at room temperature and more than 3 A/mm at 77 K have been obtained even with sapphire substrates. Cut-off frequencies were $f_T$ = 50 GHz and $f_{MAX}$ = 60 GHz for 0.15 µm gate length without T-gate. Pulsed measurements reveal a less instable surface than in the case of AlGaN/GaN structures. Although limited by buffer layer leakage, with field plates a maximum drain bias of 100 V has been reached with these devices. The high chemical stability of this unstrained heterostructure and its surface has been demonstrated with successful operation at 1000 °C in vacuum.

## Introduction

The need for higher-power devices in terrestrial and space-based communication systems has stimulated the development of GaN high power, high frequency transistors. The common structure is the AlGaN/GaN heterostructure, which has enabled to obtain extremely high power densities in RF HEMT operation in excess of 30 W/mm [1]. However being a highly strained and polarized heterojunction, stability problems still plague these devices, and they are reliable only when operated well below their limit.
InAlN/GaN is a novel heterostructure [2,3], which can be lattice matched to GaN, and due to a high interfacial 2DEG density of $3\times10^{13}$ $cm^{-2}$, open channel currents up to 3 A/mm have been predicted [4]. However the heterostructure is difficult to grow with smooth interface. A key aspect here [5] has been the insertion of a thin AlN interfacial layer (Fig. 1.a), resulting in high sheet charge density of $2.5\times10^{13}$ $cm^{-2}$, a mobility of 1170 $cm^2$/Vs and a low sheet resistance of 210 Ω/□. The In rate in the barrier has been measured by a typical (0002) high resolution X-ray diffraction (shown in Fig. 1.b). High output currents could recently be indeed demonstrated [6,7]. In this contribution we evaluate the DC current handling capability, the RF small signal performance, the pulse stability and the high temperature stability of this novel materials configuration.

## Growth and processing

An AIXTRON Metalorganic Vapor Phase Epitaxy system has been used to grow AlInN/GaN on 2 inch diameter (0001) sapphire substrate [8]. The studied structure consists of 2 µm thick GaN buffer, 1 nm thick AlN spacer layer and 13 nm thick AlInN barrier layer containing 81% Al. Hall Effect measurements at room temperature and at 77 K give a sheet carrier density $N_S$ = $2.5\times10^{13}$ $cm^{-2}$, a sheet resistance of 210 Ω/□ (RT) and 80 Ω/□ (77 K) with a record electron mobility of 1170 $cm^2$/Vs and 3170 $cm^2$/Vs respectively. MESA isolation has been performed by dry etching in Argon plasma. For the ohmic contacts, a Ti/Al/Ni/Au metal sequence annealed at 890°C for 60 sec has been used. A contact resistance $R_C$ = 0.7 Ω.mm has been obtained, as measured by TLM. The Drain-Source distance is 2.5 µm. Ni/Au Schottky gates have been defined by e-beam lithography.

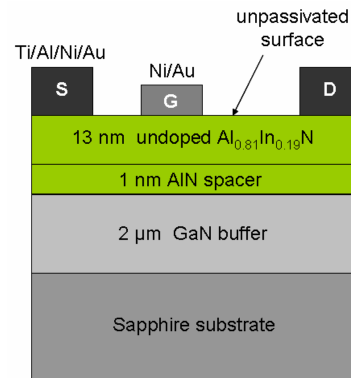


Figure 1.a: Schematic cross section of an AlInN/GaN HEMT structure

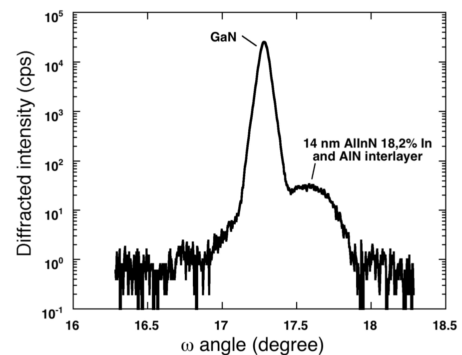


Figure 1.b: high resolution X-ray diffraction curve of the AlInN/GaN HEMT

## DC and pulsed measurements

FET structures with 0.15 µm gate length (and 50 µm gate width) have yielded in a current density of 2.3 A/mm at $V_{GS}$ =

+2.0 V, corresponding to a DC power loss of approx. 1 W (Fig. 2). This is to our knowledge beyond the highest drain current density of any AlGaN/GaN HEMT structure, especially when fabricated on sapphire. The result reflects the high sheet carrier density in this unstrained heterostructure.

Under pulsed conditions this output current increases to 2.8 A/mm (Fig. 3), which shows that we can expect even higher current densities by improving the thermal management and reducing trap effects. Pulse experiments were performed in a routine as used to assess the stability of AlGaN/GaN devices (described with more details elsewhere [9]) with 500 ns pulses. All quiescent bias points ($V_{DS0}$, $V_{GS0}$) are chosen in order to simultaneously eliminate the thermal and trap effects (cold polarization) and to reveal the gate and drain lag effects: ($V_{DS0}$ = 0 V, $V_{GS0}$ = 0 V), ($V_{DS0}$ = 0 V, $V_{GS0}$ = pinch-off voltage) and ($V_{DS0}$ = 10 V, $V_{GS0}$ = pinch-off).

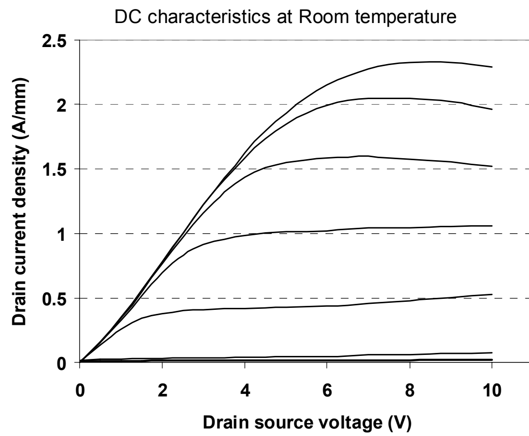


Figure 2: DC output characteristics of a 0.15×50 µm² $Al_{0.81}In_{0.19}N$/GaN HEMT at room temperature. $V_{GS}$ swept from -10 V to 2 V by steps of 2 V

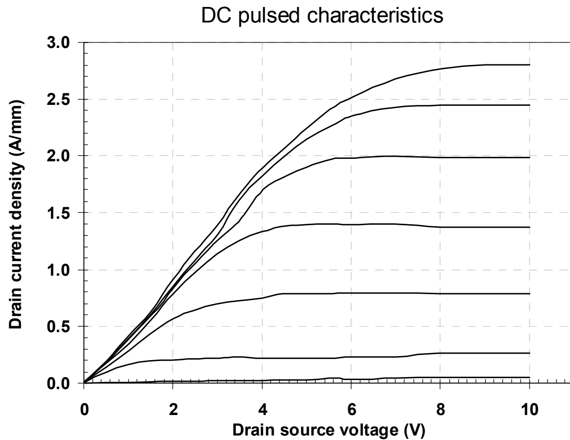


Figure 3: DC pulsed characteristics of a 0.15×50 µm² $Al_{0.81}In_{0.19}N$/GaN HEMT from the following quiescent bias point: ($V_{DS0}$ = 0 V, $V_{GS0}$ = 0 V). $V_{GS}$ swept from -10 V to 2 V by steps of 2 V

In the pulse measurement routine a fixed voltage was applied to the drain while the gate was pulsed to different on-state $V_{GS}$ values (gate lag effect). Then the voltage applied to the gate was fixed, while the drain was pulsed from 0 to 10 V (drain lag effect). In the case of unpassivated AlGaN/GaN HEMTs a significant current collapse is observed under pulsed gate and drain conditions due to AlGaN surface charging effects [10]. A much lower current compression (Fig. 4) was observed in our case, although these devices were still unpassivated, indicating a less instable surface in the case of an AlInN barrier material.

The introduction of a $Si_3N_4$ passivation seems efficient to reduce the parasitic gate and drain lag effects (Fig. 5). However, no improvement of the breakdown voltage has been observed, presumably because the electronic $Si_3N_4$ band gap energy is lower than the one of AlInN containing 17% In (about 5.3 eV).

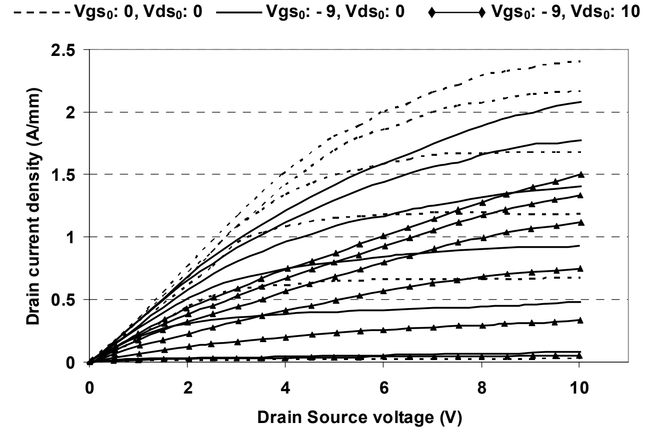


Figure 4: Pulsed $I_D$-$V_{DS}$ characteristics of unpassivated $Al_{0.81}In_{0.19}N$/GaN HEMT with three different quiescent bias points: Cold point: $V_{DS0}$ = 0 V, $V_{GS0}$ = 0 V, gate lag: $V_{DS0}$ = 0 V, $V_{GS0}$ = -9 V and drain lag: $V_{DS0}$ = 10 V, $V_{GS0}$ = -9 V. $V_{GS}$ swept from -9 to 1 V by steps of -2 V

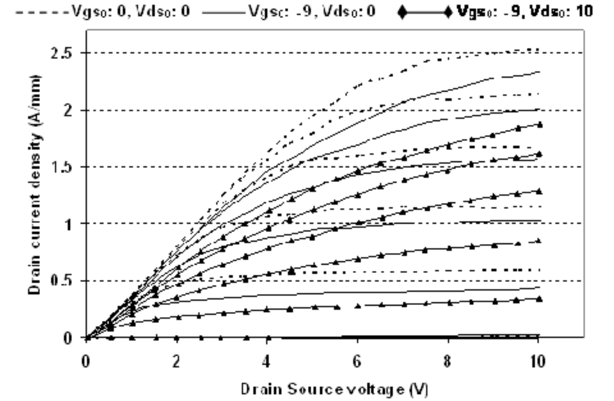


Figure 5: Pulsed $I_D$-$V_{DS}$ characteristics of a SiN passivated with three different quiescent bias points: Cold point: $V_{DS0}$ = 0 V, $V_{GS0}$ = 0 V, gate lag: $V_{DS0}$ = 0 V, $V_{GS0}$ = -9 V and drain lag: $V_{DS0}$ = 10 V, $V_{GS0}$ = -9 V. $V_{GS}$ swept from -9 to 1 V by steps of -2 V

In Fig. 6 the reverse characteristic of the Schottky diode plotted in semi-logarithm without Field Plate and with different Field Plate extensions (FP1 = 0.25 µm, FP2 = 0.6 µm and FP3 = 1 µm) are presented. Without FP, we observe a large leakage current and a breakdown voltage of the Schottky diode around -35 V. To reduce this leakage current and improve the breakdown, we used a Field Plate technology. With FP1 which corresponds more or less to a T gate we note a strong reduction of the Schottky diode leakage current (more than 1 order of magnitude) and approximately the same breakdown voltage. With FP2 and FP3, we obtain a dramatic improvement of the Schottky diode breakdown up to -70 V and more than -100 V respectively.

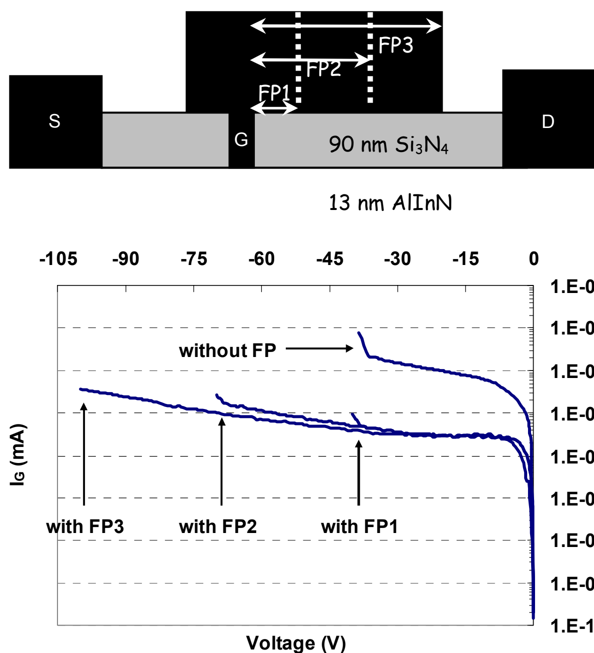


Figure 6: Schematic cross section of the Field Plate technology and reverse characteristic of the Schottky diode without Field Plate and with the different Field Plate extensions (FP1, FP2 and FP3)

## Small signal measurements

0.15×50 µm² HEMT devices were analysed by small signal s-parameters between 0.5 and 40 GHz and have yielded in a cut-off frequency $F_t$ = 50 GHz, resulting in a $F_t$ x $L_g$ product of 7.5 GHz.µm, and a maximum oscillation frequency $F_{max}$ = 60 GHz (Fig. 7) extrapolated from the current gain $H_{21}$ and the maximum available gain (MAG) at $V_{GS}$ = -6.5V and $V_{DS}$ = 10V. No T-gate structure was used, causing the low $F_{max}$ value. These results may still be improved because of the lack of T-gates and relatively high ohmic contact resistances. Nevertheless, we observe a significant increase of the cut-off frequency with reduced gate length (Fig. 8), indicating that parasitics are not totally dominating.

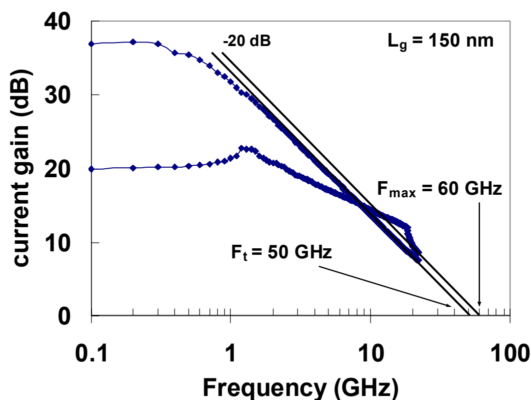


Figure 7: Cut-off and maximum oscillation frequency performances of a 0.15×50 µm² $Al_{0.81}In_{0.19}N/GaN$ HEMT biased at $V_{DS}$ = 10 V

In order to avoid short channel effects, it is necessary to maintain a high structural aspect ratio. Thus, the reduction of the gate length implies the decrease of the barrier thickness. In our case a barrier thickness of only 13 nm was used, compared to typical AlGaN-barrier thicknesses of 25 nm. This will also allow to obtain high transconductances, low output conductances and high gain at mm-wave frequencies for sub-100 nm gate lengths. Recently, cut-off frequency state of the art of GaN based (172 GHz) has been reached by a Japanese group using a 6 nm $Al_{0.86}In_{0.14}N$ barrier thickness and a gate length of 60 nm [11].

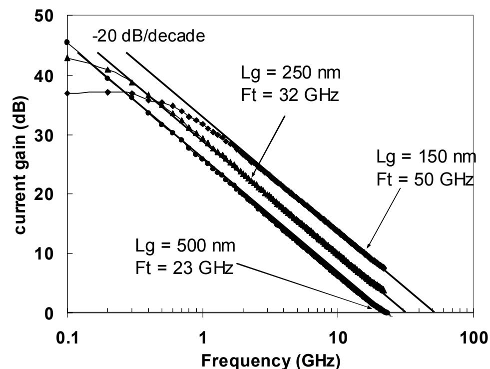


Figure 8: Cut-off frequency performances of $Al_{0.81}In_{0.19}N/GaN$ HEMT biased at $V_{DS}$ = 10 V for different gate lengths

## Temperature measurements

Devices have been tested at low temperature on-chip on a stage cooled to 77 K. The maximum current density increased to 3.1 A/mm (Fig. 9). This extremely high current value shows that, although high current densities are obtained at RT. despite the low thermal conductivity of sapphire, this density can still be increased by improved thermal management.

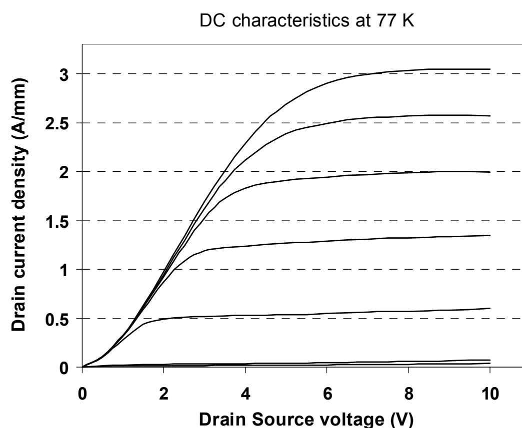


Figure 9: DC output characteristics of a 0.15×50 µm² $Al_{0.81}In_{0.19}N/GaN$ HEMT at 77 K. $V_{GS}$ swept from -10 V to 2 V by step of 2 V

Devices have also been tested on-chip at high temperature in vacuum up to 1000 °C. The temperature stress experiment was performed as follows: In vacuum the samples have been heated in intervals of 100°C and kept at the temperature for 10 min. During this time, the device was continuously tested by on-wafer bias scan. The temperature had been checked carefully by 2-way differential pyrometer, thermocouple reading and melting point measurement of Au (1063°C). Fig. 10 shows a photograph taken during test, illustrating the radiation of the transparent AlInN/GaN/Sapphire chip.

Between each temperature step the sample was cooled down to the Room Temperature and data were taken to evaluate permanent degradation.

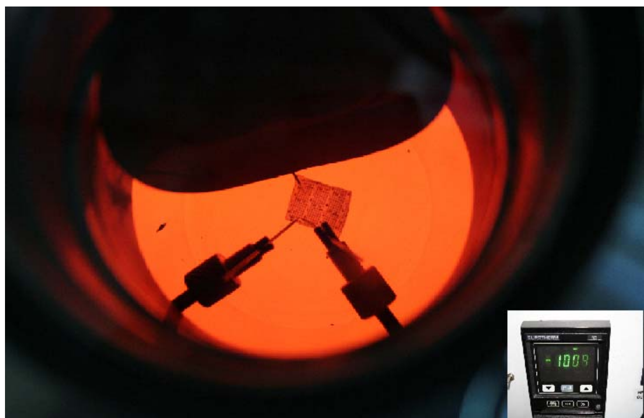

Figure 10: Sample under test at 1000°C

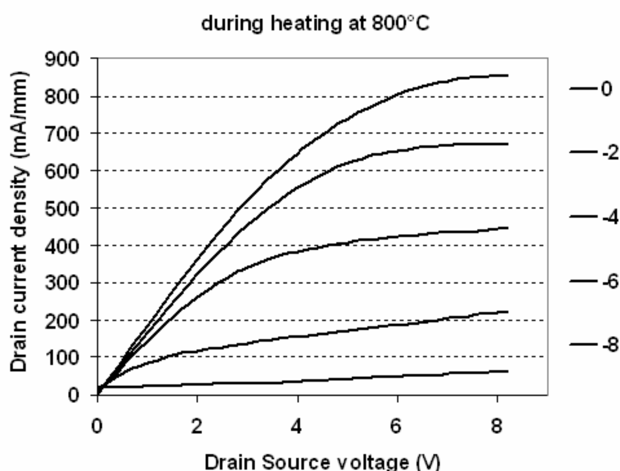


Figure 11: $I_D$-$V_{DS}$ characteristics of a 0.25×50 µm$^2$ AlInN/GaN HEMT during heating at 800°C. $V_{GS}$ swept from -8 V to 0 V by steps of 2 V

At 800°C (Fig. 11) the device presents still a high saturated maximum drain current density and transconductance of about 850 mA/mm and 100 mS/mm respectively. A slight reduction of the pinch-off voltage with temperature is observed. Both, the shift in threshold voltage and the decrease in open channel current translate a decrease of sheet carrier density and mobility at high temperatures. The buffer layer isolation suffers also, indicating the activation of defects in the buffer layer.

At 1000°C more than 600 mA/mm have been measured (Fig. 12). Pinch-off had now been seriously degraded due to buffer layer leakage caused by deep level activation. However, after cooling the original output characteristics could be nearly completely recovered, indicating no permanent degradation. Shortly above this temperature the Au metallization overlay became liquid and measurements at higher temperature were not possible. To our knowledge this is the first semiconductor transistor operation at this temperature.

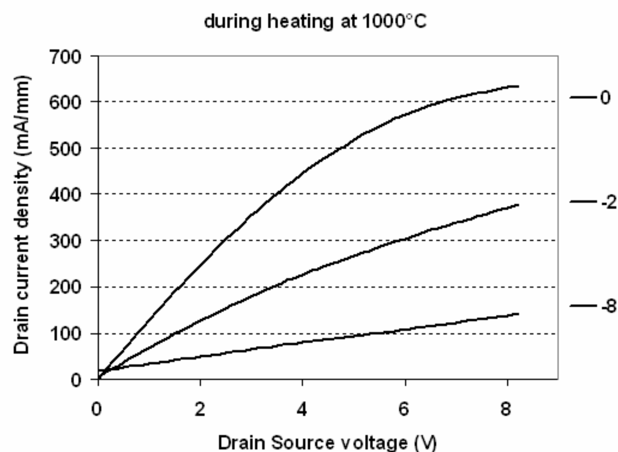


Figure 12: $I_D$-$V_{DS}$ characteristics of a 0.25×50 µm$^2$ AlInN/GaN HEMT during heating at 1000°C. $V_{GS}$ swept from -8 V to 0 V by steps of 4 V

## Conclusion

We have shown the capability of a novel AlInN/GaN heterostructure to deliver higher output current density, to operate at high frequency and to be less instable than AlGaN/GaN structure. Moreover, with these devices we have demonstrated FET operation at 1000°C in vacuum for the first time.

Power measurements will be carried out soon in order to show whether this heterostructure could overcome and definitely be an alternative to AlGaN/GaN devices.

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