5.3 A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection

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Clock and data recovery (CDR) circuits operating in the 10Gb/s range have become attractive for the optical fiber backbone of the Internet. While CDR circuits operating at 10Gb/s have been designed in bipolar technologies, cost and integration issues make it desirable to implement these circuits in standard CMOS processes. This 10Gb/s CDR circuit is realized in 0.18μm CMOS technology. Architecture and circuit techniques circumvent the speed limitations of the devices. In contrast to previous work [1], this design incorporates an LC oscillator to reduce the jitter as well as a phase/frequency detector to achieve a wide capture range.

Shown in Figure 5.3.1, the CDR consists of a phase/frequency detector (PFD), a voltage-controlled oscillator (VCO), a charge pump, and a low-pass filter (LPF). The PFD compares the phase and frequency of the input data to that of a half-rate clock, providing two binary error signals for phase and frequency. The PFD is designed so that, in addition to providing information about the phase error, it retimes the data as well. Consequently, the CDR exhibits no systematic offset, i.e., inherent skews between clock and data edges due to their unidentical paths through the loop do not degrade the quality of detection. The VCO provides four differential half-quadrature phases over the full tuning range. All building blocks are fully differential.

Since the half-rate frequency detector requires clock phases that are integer multiples of 45°, the 5GHz VCO is designed as a ring structure consisting of four LC-tuned stages [Figure 5.3.2a]. If the dc feedback around the ring is positive, all stages operate in-phase at the resonance frequency defined by the LC tanks. On the other hand, if the dc feedback is negative, the frequency shifts by a small amount so as to allow each stage to contribute 45° of phase.

The oscillator topology has two advantages over resistive-load ring oscillators. First, owing to the phase slope (Q) provided by the resonant loads, it exhibits less phase noise. Second, its frequency of oscillation is only a weak function of the number of stages, generating multiple phases with no speed penalty. By comparison, a four-stage resistive-load ring operates at a lower frequency.

Figure 5.3.2b shows the implementation of each stage. The loads are formed using on-chip spiral inductors and MOS varactors. Resistor R1 provides a shift in the output common-mode level, allowing both positive and negative voltages across the varactors and thus maximizing the tuning range. Modeling each tank by a parallel network, the required 45° phase shift slightly detunes the circuit. The oscillation frequency is given by $\omega_0=(LC)^{-0.5}(1-1/Q_0)^{0.5}$, where Q_0 denotes the Q of each stage at resonance.

The phase detector (PD) is derived from the data transition tracking loop described in Reference 2. In this PD, in-phase and quadrature phases of a half-rate clock signal sample the data in two double-edge-triggered flipflops (DETFFs). Figure 5.3.3 shows the implementation of the PD. Two latches operating on opposite clock phases and a multiplexer form a DETFF that samples the data using both the positive and negative transitions of a half-rate clock. The two signals V_1 and V_2 are therefore the in-phase and quadrature samples of data, respectively, and one is used to route the other or its complement.

The phase detector operates at high speeds because it uses a half-rate clock. Since in the locked condition, the rising and falling edges of the quadrature clock coincide with data transitions, the in-phase clock transitions sample the data at its optimum point with no systematic offset, generating a full-rate output stream. Also, since the phase-error signal is reevaluated only at data transitions, it incurs little ripple. Note that the output is independent of the data transition density, resulting in reduction of pattern-dependent jitter.

With the small CDR loop bandwidths specified by optical standards, circuits employing only phase detection suffer from an extremely narrow capture range, e.g., about 1% of the center frequency. For this reason, a means of frequency detection is necessary to guarantee lock to random data. As with other phase detectors, the half-rate PD of Figure 5.3.3 generates a beat frequency equal to the difference between the data rate and twice the VCO frequency. However, it does not provide knowledge of the polarity of this difference. Figure 5.3.4 depicts the half-rate phase and frequency detector introduced in this work. A second PD is added and driven by phases that are 45° away from those in the first PD. The circuit operates as follows. (1) If the clock is slow, V_{PD1} leads V_{PD2}; therefore, if V_{PD2} is sampled by the rising and falling edges of V_{PD1}, the results are negative and positive, respectively. (2) If the clock is fast, V_{PD1} lags V_{PD2}. Therefore, if V_{PD2} is sampled by the rising and falling edges of V_{PD1}, the results are the reverse of the previous case.

The output buffer delivering the 10Gb/s retimed data with high current levels requires a bandwidth of more than 7 GHz. As shown in Figure 5.3.5, the buffer stage employs inductive peaking [3]. The value of the spiral inductors is chosen so as to avoid ripple in the passband. Since the quality factor of the inductors is not critical here, the spiral structures have a linewidth of only 4μm to achieve a high self-resonance frequency.

The CDR circuit is fabricated in a 0.18μm CMOS technology. The circuit is tested in a chip-on-board assembly while operating with a 1.8V supply. The phase noise of the clock in response to a 9.95328Gb/s data sequence of length 2^{23}-1 at 1MHz offset is approximately equal to -107dBc/Hz. Figure 5.3.6a depicts the recovered clock and data. A pseudo-random sequence of length 2^{23}-1 produces 9.9ps of peak-to-peak and 0.8ps rms jitter on the clock signal. The jitter characteristics are measured by the Anritsu MP1777 jitter analyzer. The measured jitter transfer characteristic of the CDR is shown in Figure 5.3.6b. The jitter peaking is 0.04dB and the 3dB bandwidth is 5.2MHz. Despite the small loop bandwidth, the frequency detector provides a capture range of 1.43GHz, obviating the need for external references. The total power consumed by the circuit excluding the output buffers is 91mW from a 1.8V supply. Figure 5.3.7 shows a micrograph of the chip, which occupies 1.75x1.55mm^2.

Acknowledgments:
The authors thank NewPort Communications for fabrication and test support. This work was supported by SRC and Cypress Semiconductor.

References:
[1] J. Savoj and B. Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit," Dig. of Symposium on VLSI Circuits, pp. 136-139, June 2000.
[2] A. W. Buchwald, Design of Integrated Fiber-Optic Receivers Using Heterojunction Bipolar Transistors, Ph.D. Thesis, University of California, Los Angeles, Jan. 1993.
[3] J. Savoj and B. Razavi, "A CMOS Interface Circuit for Detection of 1.2-Gb/s RZ Data," ISSCC Digest of Technical Papers, pp. 278-279, Feb. 1999.

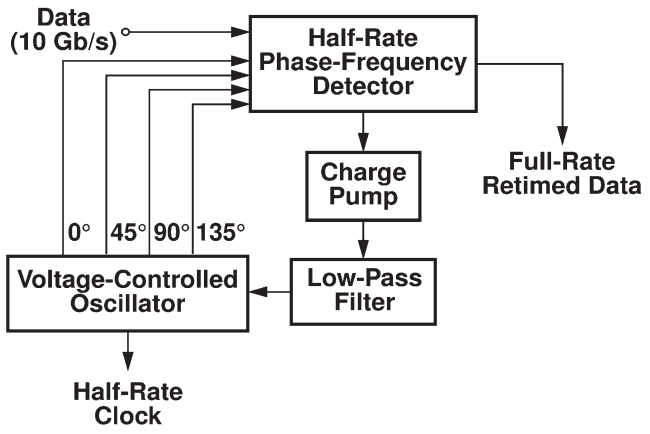


Figure 5.3.1: CDR architecture.

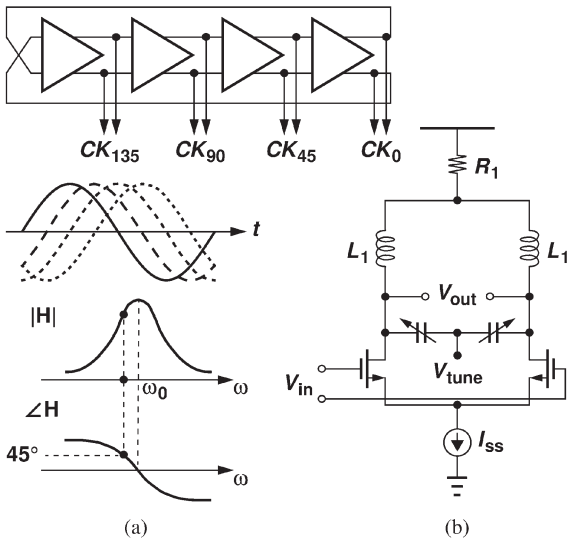


Figure 5.3.2: (a) Four-stage LC-tuned ring oscillator, (b) implementation of one stage.

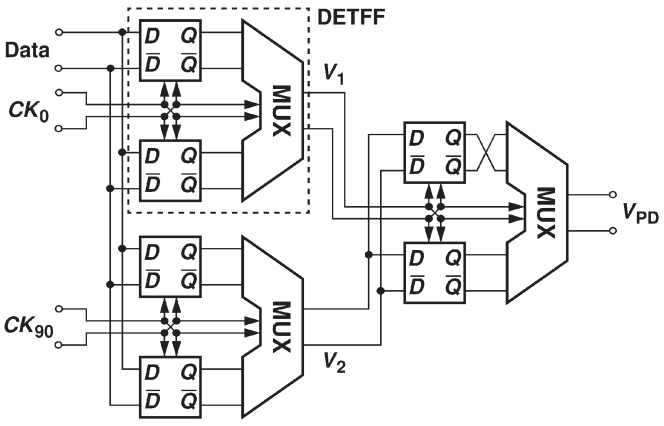


Figure 5.3.3: Phase detector.

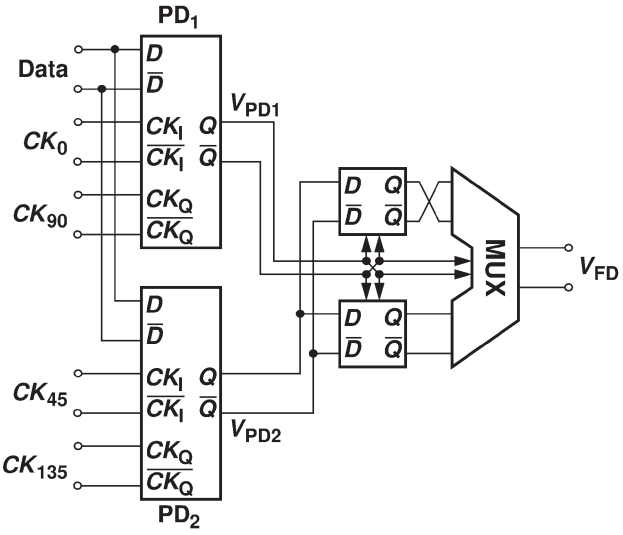


Figure 5.3.4: Phase and frequency detector.

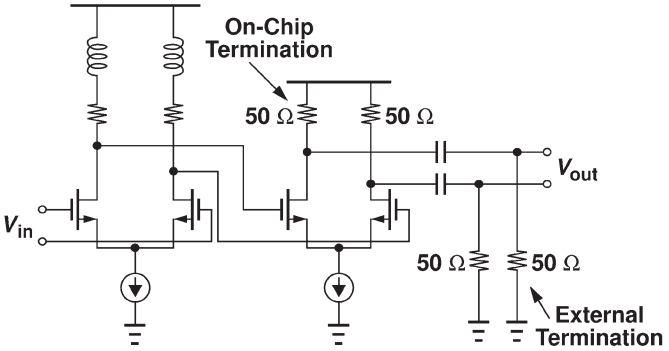


Figure 5.3.5: Output buffer.

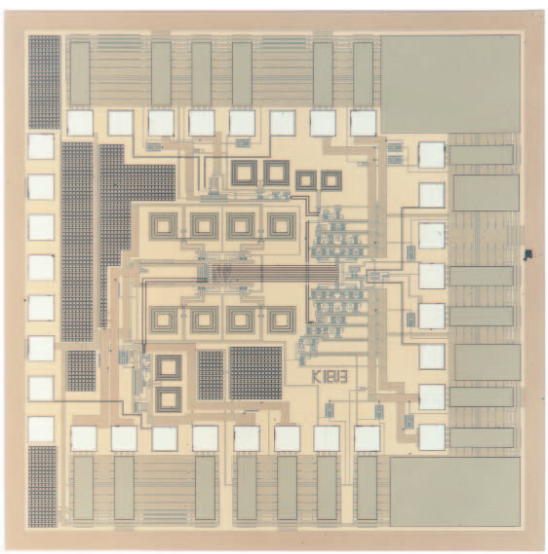
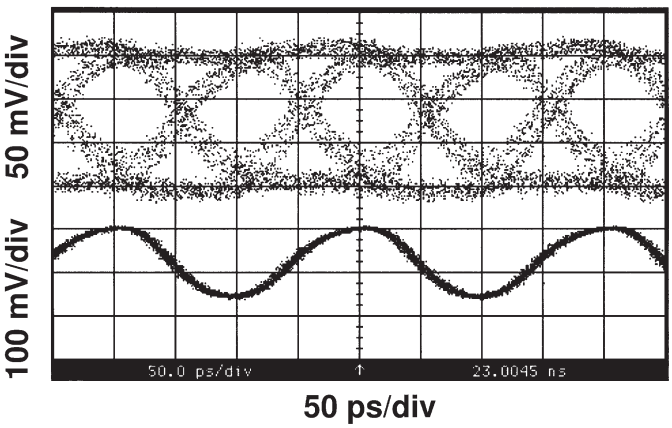
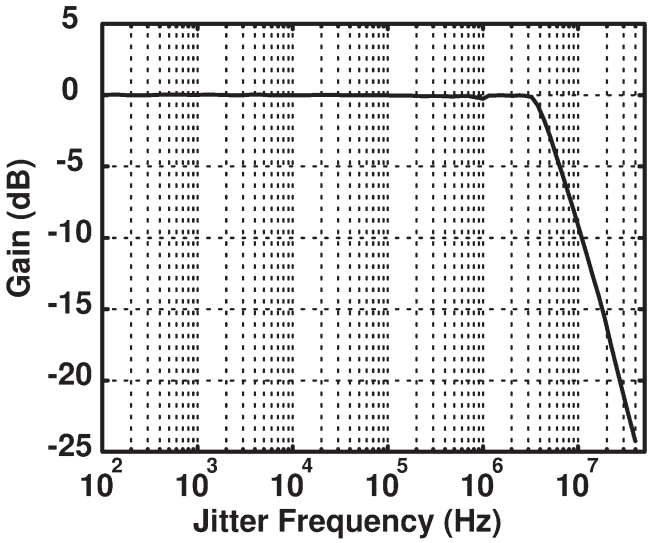


Figure 5.3.7: Die micrograph.



(a)



(b)

Figure 5.3.6: (a) Recovered data and clock, (b) measured jitter transfer characteristics.