Hybrid Phase-Change – Tunnel FET (PC-TFET) Switch with Subthreshold Swing < 10mV/decade and sub-0.1 body factor: digital and analog benchmarking

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***Abstract*—** In this paper we report the first hybrid Phase-Change – Tunnel FET (PC-TFET) device configurations for achieving a deep sub-thermionic steep subthreshold swing at room temperature and subthreshold power savings. The proposed hybrid device feedbacks the steep transition of Metal-Insulator transition in a VO_2 structure into Gate or Source configurations of strained silicon nanowire Tunnel FETs, to achieve a switching with I_{on}/I_{off} better that $5.5x10^6$ and with a subthreshold swing of 4.0 mV/dec at 25 °C. We demonstrate that the principle of PC-TFET switching relates to an internal amplification resulting in a sub-unity body factor, m, which is reduced to values below 0.1 for a current range larger than 2-3 decades. We report a full experimental digital and analog benchmarking of the new device and compare it with Tunnel FETs and CMOS. Remarkably, the PC-TFET can achieve analog figures of merit like g_m/I_d breaking the 40 V^{-1} limit of MOSFETs. We demonstrate and report the first buffered oscillator cell for neuromorphic computing exploiting the gate configuration of PC-TFET.

I. Introduction

The aggressive scaling of CMOS gate length dimensions is facing major challenges in terms of voltage supply scaling, leakage currents, variability and power density. In order to achieve threshold voltage scaling and low subthreshold leakage, steep slope switches are under intense exploration. The goal is to achieve a steep subthreshold swing, S, lower than 60mV/decade, at the transition region between off and on states of an electronic switch. Tunnel FETs (TFETs) exploiting quantum mechanical band-to-band mechanisms [1], negative capacitance FETs and nano-electro-mechanical relays are some of the classes of devices explored for a sub-thermionic swing. More recently, strongly correlated functional oxides exhibiting a metal-insulator transition appeared particularly interesting for beyond CMOS electronics. Particularly, vanadium dioxide (VO_2) holds great potential due to the high contrast in conductivity between the two states and the possibility to induce the phase change by electrical excitations. VO_2-based 2-terminal switches have been thoroughly characterized, showing steep transition characteristics, fast switching time [2], high reliability [3] and low temperature dependence [4]. The development of VO_2-based 3-terminal devices was attempted first with standard MOSFET architectures in which VO_2 is used as the semiconductor material [5], however achieving very low gate transconductance [6]. A 3-terminal device architecture based on III-V FinFETs and VO_2 has been proposed as a more promising approach, but the I_{ON}/I_{OFF} ratio was still limited to unacceptable values and the abrupt switch region was very limited for a really practical use [7].

Here, we propose and present the *phase-change TFET* (PC-TFET) as a hybrid design integration of a 3-terminal TFET and a 2-terminal VO_2 switch, resulting in the first solid-state VO_2-based 3-terminal switch with very low I_{OFF} current, high I_{ON}/I_{OFF} ratio and ultra-steep subthreshold swing. We explain the working mechanism of the device in different configurations and we show its potential for digital and analog applications as well as its use as a buffered oscillator to build neuromorphic computing circuits.

II. Phase-Change – Tunnel FET operation

The main idea of the proposed architecture is to feedback the ultra-abrupt switching in the VO_2 into a TFET characteristic, which serves to control and offer a very low Ioff current. We will show that the main result, is a unique hybrid switch, using BTBT and internal amplification, thus, having a body factor, $m = dV_{GS}/d\psi_S$ much smaller than 1. We call this device combining two switching principles PC-TFET.

The PC-TFET can be built in "gate" and "source" configurations, The "gate" configuration is obtained by connecting a voltage divider formed by a VO_2 switch and a load resistor to ground on the gate of TFET (Fig. 1a). The externally applied gate bias in the "gate" configuration is partitioned between the VO_2 resistance and the gate load. Due to the high resistance of VO_2 in the insulating state, the TFET is not turned on until the increasing gate voltage causes the insulator to metal transition (IMT), which causes a steep transition in the TFET intrinsic gate voltage, V_{GSint}, and, consequently, the drain current. The abrupt change of V_{GSint} has as a consequence a strong reduction of the body factor ($m<<1$). In the "source" configuration (Fig. 1b) the VO_2 switch is connected in-series to the source terminal of the TFET. When a low gate voltage is applied and swept-up, the drain current is limited by the high impedance of the switch until the drain current is high enough to trigger the IMT. The resulting hybrid PC-TFET has a significant abrupt swing and a programmable actuation voltage, V_{act} (Fig. 1c). However, similarly to VO_2 switch, the PC-TFET could exhibit some hysteresis in switching; both the hysteresis and the actuation voltage can be tuned by the device impedance (VO_2 and TFET) design (Fig. 1c).

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III. PC-TFET DIGITAL SWITCH FABRICATION, EXPRIMENTS AND FIGURES OF MERIT

We report the first experimental demonstration of a PC-TFET. Strained Silicon gate-all-around TFETs have been fabricated using dopant segregation from $NiSi_2$ [8] (Fig. 2a); the VO_2 switches were made starting from a reactive sputtering deposited 200 nm thick VO_2 film (Fig. 2b). The transfer characteristics of a p-type TFET with an I_{on}/I_{off} ratio of 9 decades and a VO_2 switch exhibiting IMT below 1 V are shown in Fig. 3. In the gate configuration PC-TFET, the voltage drop on the VO_2 keeps the drain current I_D at low value till the transition, for which we show an abrupt swing of 4 mV/dec (Fig. 5) at room temperature. This is due to the steep voltage transition of the internal gate node V_{Gint}, Fig. 6. Via TCAD simulation using the measured values of the internal node it was possible to extract the body factor *m* of the PC-TFET. We obtained a value of *m* of ~0.05 (<< 1) for more than 2 decades of current range, demonstrating an internal amplification due to phase change in VO_2 (Fig. 7).

In the "source" configured PC-TFET, the off state drain current increases slowly with the gate voltage, limited by the VO_2 insulating state, until the power density is high enough to trigger the IMT and cause the transition to the metal state in VO_2 and $V_{GSint} = V_{GS} - I_D \times R_{VO2}$ to abruptly increase (and so the drain current) due to the lower source resistance (Fig. 8). The mechanism of the transition can be explained by the simultaneous change of the voltages between the internal TFET nodes of gate, source and drain. However when the gate voltage increases the resistance of the channel resistance decreases and thus the voltage drop on the switch starts increasing till the transition occurs, leading to a smaller source resistance and thus to an higher internal V_{GS} applied to the TFET (Fig. 9). Using the two sets of internal voltages, the experimentally extracted body factor shows a less than 0.1 value in the transition region (Fig. 10).

Overall, the "gate" and "source" configurations of PC-TFET show value of S < 10mV/decade, $I_{on}/I_{off} > 10^6$; the abrupt transition (V_{act}) can be triggered at lower and large range of drain currents (10^{-10}–10^{-7} A/um) for the "gate" configuration. This performance is maintained up to around 60°, close to the MIT transition temperature of VO_2.

IV. PC-TFET: ANALOG FIGURES OF MERIT

Such steep slope devices hold additional promise for unique analog performance at very low level of currents/power (such as amplification). We report here the detailed analog figures of merit of PC-TFET in "gate" configuration, which exhibits a large swing in transfer characteristic (Fig. 11) and an excellent current saturation in output characteristic (Fig. 12).

The transconductance, $g_m = dI_D/dV_{GS}$ (Fig.13) shows a very high peak at the transition point of more than 2250 µS/µm for the PC-TFET compared to the 70 µS/um peak of its intrinsic TFET (accessed independently at the internal node); the exceptionally high transconductance value spans for more than two orders of magnitude of drain current (Fig. 14). Consequently also the transconductance efficiency g_m/I_D shows extremely high value for the PC-TFET, breaking the 40 V^{-1} limit of a MOSFET (Fig. 15) because of the exceptionally low swing of our device. The internal gain g_m/g_{ds} is slightly lower than the one of TFET for low gate voltages but shows a higher peak at the transition before going back to the normal TFET behavior.

V. PC-TFET RELAXATION OSCILLATOR CELL

The abrupt phase transition of VO_2 can be exploited for building compact relaxation oscillators by loading a switch with a parallel RC circuit [9]. The oscillation condition is met when the load line intersects the switch characteristic in points that are not part of the stable states (insulating or metallic) (Fig. 17a). The PC-TFET can provide an oscillating signal by properly selecting the gate load resistance where the capacitance of the oscillator is given by the TFET gate. The sustained oscillations in the internal gate of the PC-TFET are reported in the drain inverted due to the common source configuration (Fig. 17b,c,d). Peaks at a central frequency of 100 kHz for both the internal gate and drain oscillations can be seen in the power spectrum (Fig. 17e,f). The PC-TFET in this configuration offers a high output impedance, which uniquely allows to decouple the output load from the oscillating source at the gate, in contrast with previous works on VO_2 oscillators. It is worth noting that such buffered oscillators may be coupled in pairs or tailored for "single-shot" neuron-like operation, enabling development of brain-inspired neuromorphic systems capable of massively parallel processing operations [10].

VI. CONCLUSIONS

We reported for the first time a new hybrid PC-TFET steep slope switch and its thorough characterization. As digital switch, the PC-TFET presents an I_{on}/I_{off} ratio better that 5.5×10^6 and a subthreshold swing of 4.0 mV/dec at room temperature over more than 3 decades of current, opening a new design space beyond alternative steep slope devices (Fig. 18). We showed for the first time that the low swing of such hybrid devices relies on an equivalent body factor m <<1. We explored the analog figures of merit and demonstrated the first VO_2-based buffered oscillator cell for neuromorphic computing.

ACKNOWLEDGEMENTS

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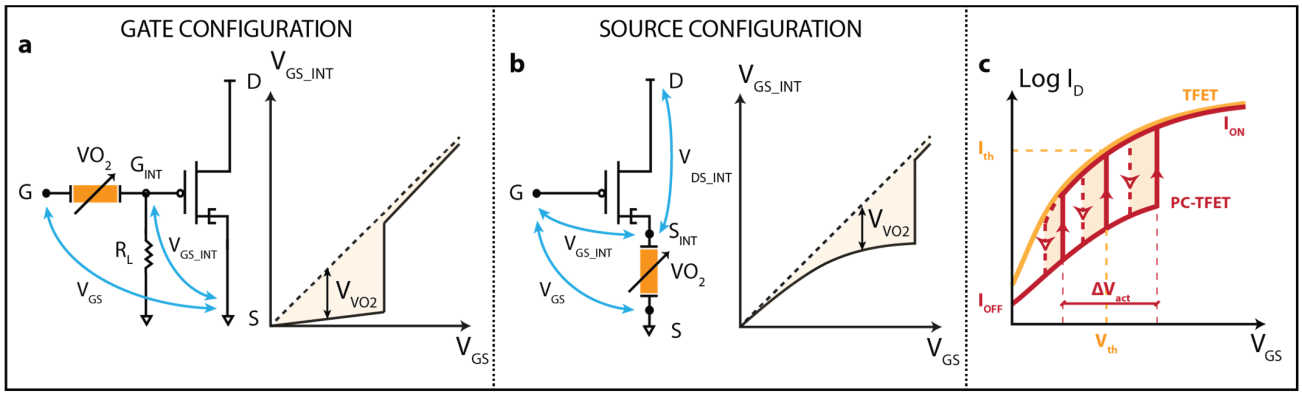

Fig. 1. PC-TFET principle combining VO_2 and TFET in "gate" (a) and "source" (b) configurations, with resulting abrupt switching of the intrinsic gate potential, V_{Gint}; (c) Qualitatively predicted PC-TFET characteristics for different values of the VO_2 switch threshold voltage Vact, compared to the transfer characteristics of a TFET with threshold voltage Vth.

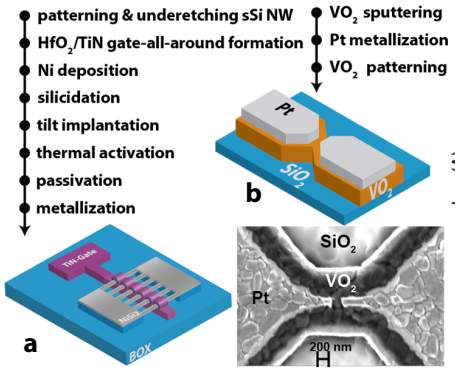

Fig. 2 (a) Main fabrication steps for strained silicon TFET and (b) for VO_2 switches (SEM in inset).

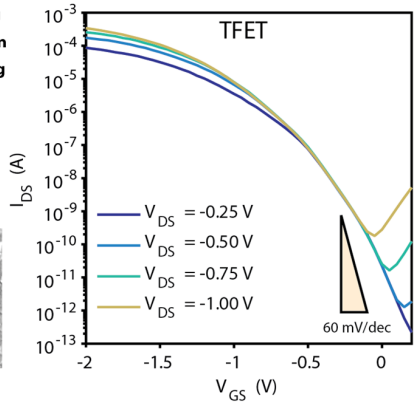

Fig. 3. TFET transfer characteristic at multiple Vds values at 25°C.

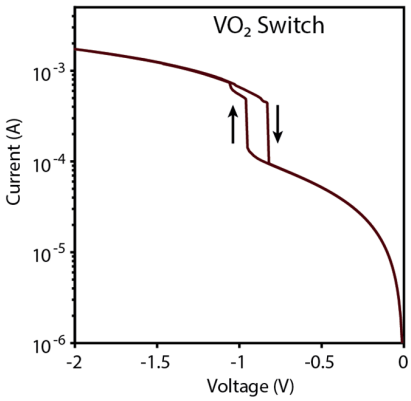

Fig. 4 VO_2 characteristic at 25°C

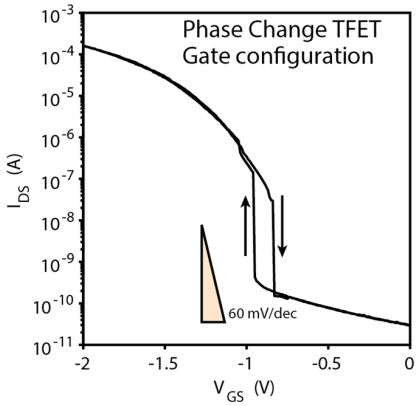

Fig. 5. Transfer characteristic of the PC-TFET in gate configuration

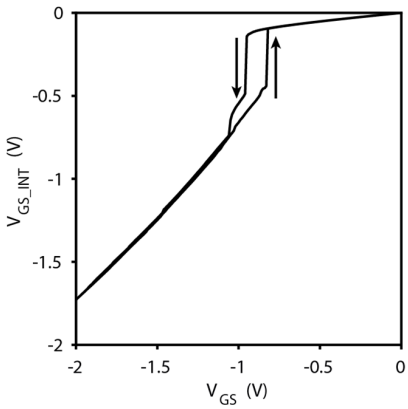

Fig. 6. Internal gate voltage of PCTFET in gate configuration

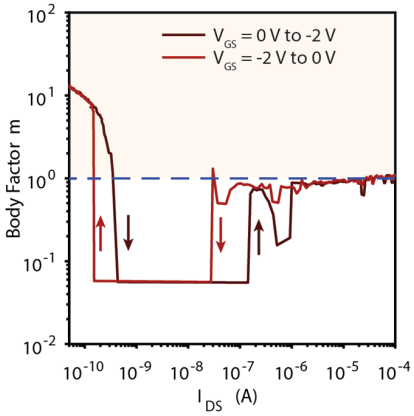

Fig. 7. Extracted body factor for PCTFET in gate configuration.

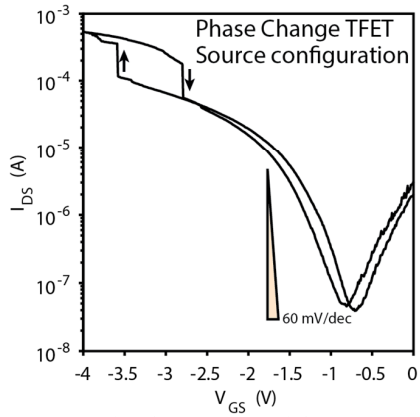

Fig. 8. Transfer characteristic of the PC-TFET in source configuration

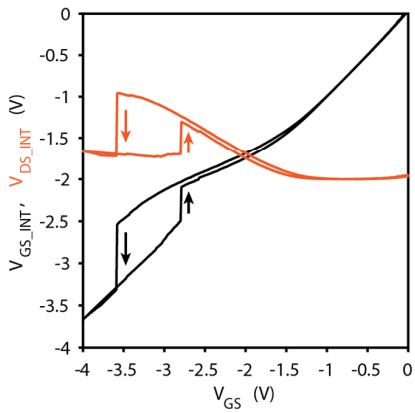

Fig. 9. Internal gate and drain voltages of PCTFET in source configuration

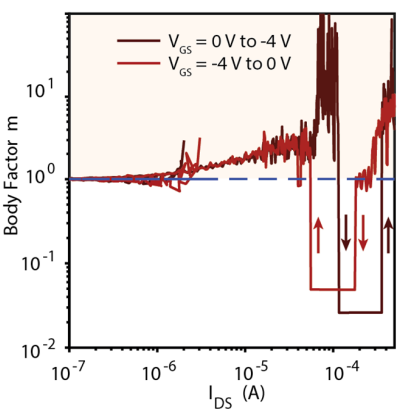

Fig.10. Extracted body factor for PCTFET in source configuration.

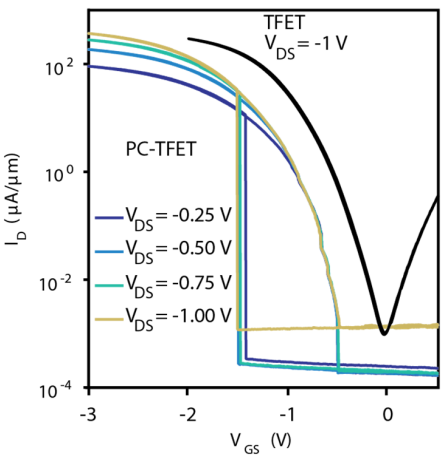

Fig. 11. Transfer characteristic of the TFET and PC-TFET for different bias. PC-TFET characteristic is shifted because of the voltage divider between VO_2 metallic state resistance and load resistance.

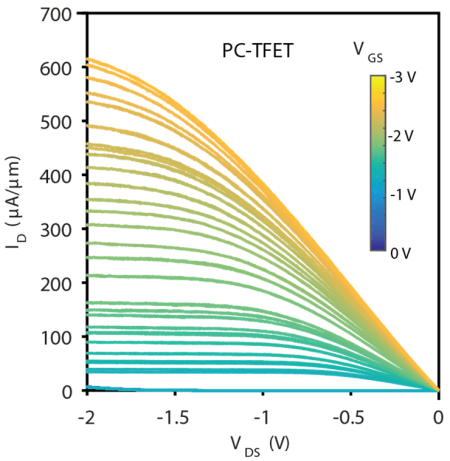

Fig. 12. Output characteristic of the PC-TFET for different gate voltages.

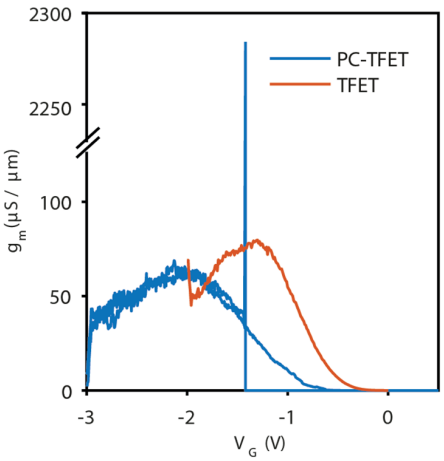

Fig. 13. Gate transconductance vs gate voltage for the TFET and PC-TFET.

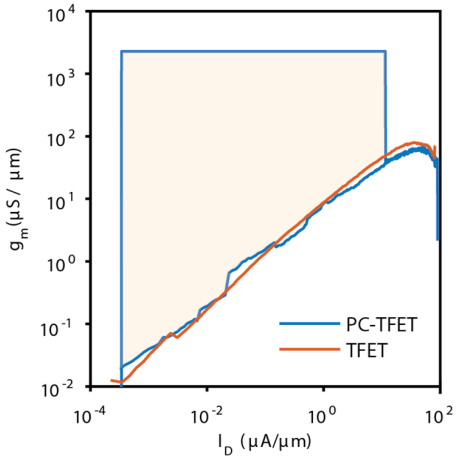

Fig. 14. Gate transconductance vs drain current for the TFET and PC-TFET.

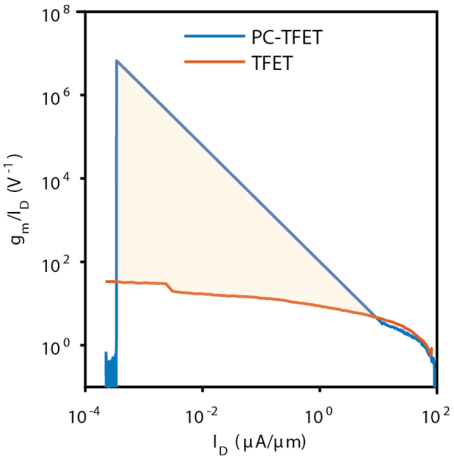

Fig. 15. Transconductance efficiency vs drain current for the TFET and PC-TFET.

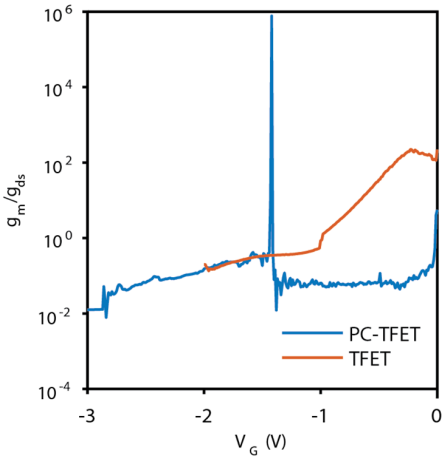

Fig. 16. Intrinsic gain vs gate voltage for the TFET and PC-TFET.

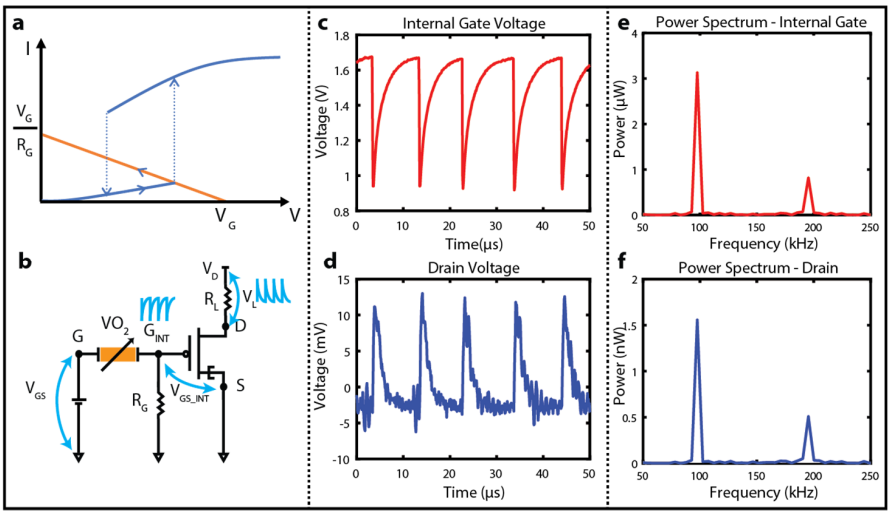

Fig. 17. (a) I-V plot of VO_2 hysteretic characteristic and load line; (b) Schematic of VO_2 relaxation oscillator for neuromorphic applications, with TFET in common source configuration as capacitive load; (c) and (d) time domain plots of V_{GS_INT} and V_L; e)-f) power spectral content of V_{GS_INT} and V_L signals delivered respectively on R_G and R_L.

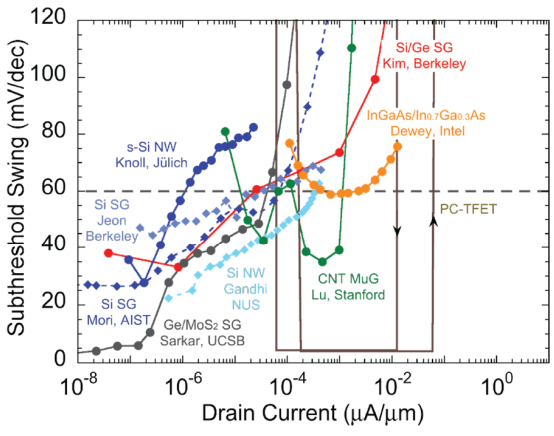

Fig. 18. Steep slope switches benchmarking in terms of subthreshold swing versus drain current, pointing out the deep sub-thermionic swing of the PC-TFET compared to all classes of TFETs.