4.5 A 13.5dBm Fully Integrated 200-to-255GHz Power Amplifier with a 4-Way Power Combiner in SiGe:C BiCMOS

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In order to efficiently utilize the frequency band above 200GHz for radar and communication applications, enough transmitted output power is essential to overcome the elevated path loss. For silicon-based technologies, the available output power at this frequency range is limited. The enlarging of the transistor size and so the corresponding power handling leads to a reduced output impedance. This causes the impedance transformation ratio to increase allowing only for narrow-band designs. Power combining of multiple single power amplifiers (PAs) is a common approach to achieve high output power alleviating the need to enlarge the devices size [1]. In this paper, we present a fully integrated PA that combines the power of 4 differential PA units using a 4-way zero-degree combiner and a 4-way active splitter to feed the 4 PA units.

Different approaches are possible for power combining. Although Wilkinson power combiners guarantee certain isolation between the PA units, the expected achievable power-added efficiency (PAE) decreases due to the losses of the Wilkinson passive structure. Other approaches are to combine using transformers or T-Lines. In these cases, the combining structure is also utilized as the matching network, achieving better PAE compared to the Wilkinson power combiner. The T-line, or also called zero-degree power combiner, is more efficient compared to the transformer based combining as the targeted frequency increases. This is due to the more complex structure of the transformer-based combining network and the reduced mutual coupling for a few turns [2]. Both such combiners were designed and electromagnetically (EM) simulated. The 2-way T-line combiner simulation shows a loss of 0.4dB. This is a better performance than a 1.5dB loss for the transformer based 2-way combiner. In this work, we combine 4 differential PA units with a zero-degree power-combining structure, which is also the output matching of the single PA units.

In previous works, the power combiners were also utilized as the power distributing networks [1-3]. Instead, in this work a 2-cascaded 1-to-2 active power splitters are implemented. This enhances the overall PA bandwidth by optimizing the inter-stage matching between the stages so that the PA performance is not limited by the 4-way distribution network.

The schematic of the single PA unit, together with the circuit-core EM 3D view and its bias circuit, is shown in Fig. 4.5.1. The PA unit consists of a differential cascode amplifier. All transistors are biased at the maximum f_T bias conditions. The parasitic inductance at the bases of the cascode devices is minimized to guarantee unconditional stability of the PA unit. The bases of Q_3 and Q_4 are connected to guarantee a virtual ground and so to maximize the differential gain. The base capacitance (C_1) is still integrated to assure the bases are grounded across process and mismatch variations. The cascode base is connected to the bottom plate of C_1 to reduce the routing inductance, and then the upper plate is connected to the ground shield. S-parameters and load pulling simulations showed output impedance (Z_{out}) of (6-j42)Ω and the maximum saturated output power (P_{sat}) for Z^*_{opt} of (20-j32)Ω at 250GHz. Output matching is performed as a compromise between P_{sat} and S_{22}. For such impedance range, a short stub followed by a series transmission line is an optimal matching network.

Figure 4.5.2 shows the block diagram of the 4-way PA. To keep low impedance transformation ratios while combining, the impedance transformation is performed by TL_s and TL_1 before the first 2-to-1 combining and by TL_2 before the second 2-to-1 combining, as shown in the Smith chart in Fig. 4.5.2 at a chosen frequency of 250GHz. The 1-to-2 power splitters are also utilized as matching networks between the stages and are optimized for wideband response. The cross-overs within the zero-degree combiners and splitters were optimized to reduce the systematic mismatches by equalizing the electrical length of the differential signal as much as possible.

One bias circuit for each stage is implemented to avoid cross-coupling across the stages. For multi-stage designs, the supply and ground connections are critical to guarantee stability, especially since the k-factor simulated for the multi-stage amplifier is not sufficient to assure unconditional stability. For stability considerations, a small supply decoupling capacitor of 200fF is integrated in close proximity of each PA unit. Then larger capacitors, de-Q'ed with small resistors, are integrated as traces approach the DC-pads where supplies are combined.

Utilizing such power combining, power splitting, and PA-unit architectures, a fully integrated power amplifier was implemented in a 0.13µm SiGe:C BiCMOS technology with $f_t\backslash f_{max}$=300\500GHz. The PA was characterized on wafer using two test structures. The first test structure is the standalone 4-way PA circuit, utilized to measure the 2-port S-parameters and the output 1dB compression point (OP1dB). While the second test structure is an integrated multiplier-by-8 chain driving the PA with enough power to measure P_{sat}.

In the first setup, waveguide probes (WR4.3), frequency extenders (RPG ZC260), and two DC probes for supply were used. Input and output Marchand baluns are integrated to allow for single-ended measurements. Measured loss of the Marchand balun and a pad is 1.5dB at each side.

Small-signal S-parameters in Fig. 4.5.3 show the maximum gain of 12.5dB across a 3dB bandwidth of 55GHz from 200 to 255GHz. This is shifted by approximately 4% from the simulation results mostly due to inaccuracies in the transistor models or the parasitic extractions. The input return loss (S_{11}) is centered on purpose at higher frequencies to enhance the gain flatness. As the design is meant for fully differential systems the S_{11} and S_{22} degradation due to the pad and balun are not compensated for. Stability k-factor is plotted showing values above 1 across the whole band. An important parameter for communication applications is the group-delay variation, which was measured to be only ±5ps across the whole band as plotted in Fig. 4.5.4, where the simulated and measured OP1dB are also plotted showing the maximum value of 9dBm. It becomes 10.5dBm after calibrating for the output balun and pad loss, which is equivalent to a power-added efficiency (PAE) at OP1dB of 1.47%.

Although the delivered power from the ZC260 was enough to measure the OP1dB, it was not enough to measure P_{sat}. Therefore, the second setup and a test structure were used where a 30GHz signal is delivered to the on-chip multiplier-by-8 chain, which then drives the PA with differential power of approximately 2dBm. The simulated and measured P_{sat} of the multiplier chain cascaded with the PA is shown in Fig. 4.5.5 across frequency, exhibiting a saturated output power of 12dBm. This becomes 13.5dBm, when omitting the losses of the output balun and the pad, leading to the drain efficiency (η_d) of 3%. Simulations results for 25°C and 40°C temperatures are plotted to highlight the effect of the elevated on-chip temperature on the performance.

Figure 4.5.6 summarizes the design parameters of the presented PA, together with the prior-art integrated PAs in silicon technologies above 200GHz. Very good performance can be observed when compared to the prior art. The maximum measured OP1dB of 9dBm is 5dB higher than the maximum achieved in designs reported in Fig. 4.5.6 with 7-times better PAE at OP1dB. The measured P_{sat} is approximately 2 times higher than the reported silicon-based power-combined PAs above 200GHz with 4 times higher drain efficiency [1]. All these results are achieved across a 55GHz of 3dB linear bandwidth, which is 1.8 times higher than the widest bandwidth reported in Fig. 4.5.6. The die micrograph of the integrated PA is shown in Fig. 4.5.7, where the different parts of the design are highlighted.

Acknowledgement:
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References:
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[5] M. Eissa et al., "216 - 256 GHz Fully Differential Frequency Multiplier-by-8 Chain with 0 dBm Output Power," *EuMIC*, pp. 201–204, Oct. 2017.

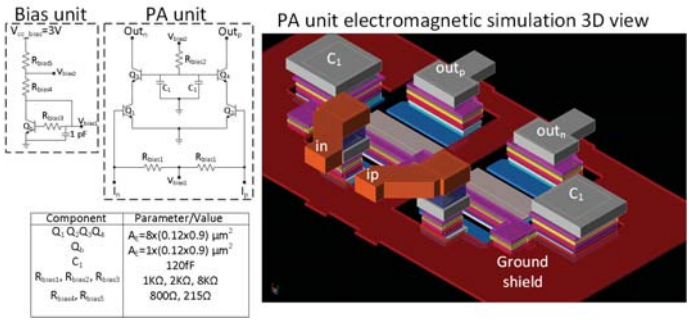

Figure 4.5.1: Schematic of the PA unit, the bias circuit, and the electromagnetic view for the transistor core.

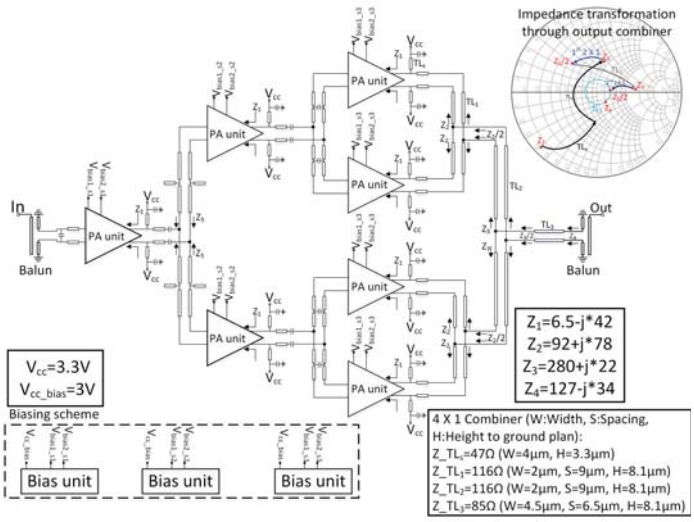

Figure 4.5.2: Block diagram of the 4-way power-combined PA.

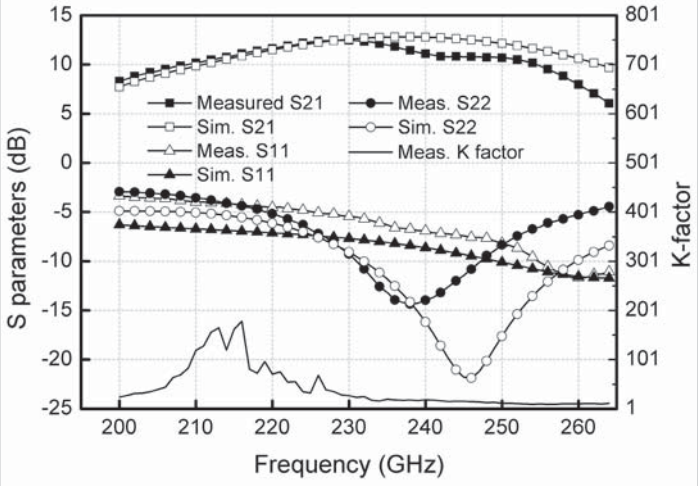

Figure 4.5.3: Simulated and measured S-parameters for the 4-way PA.

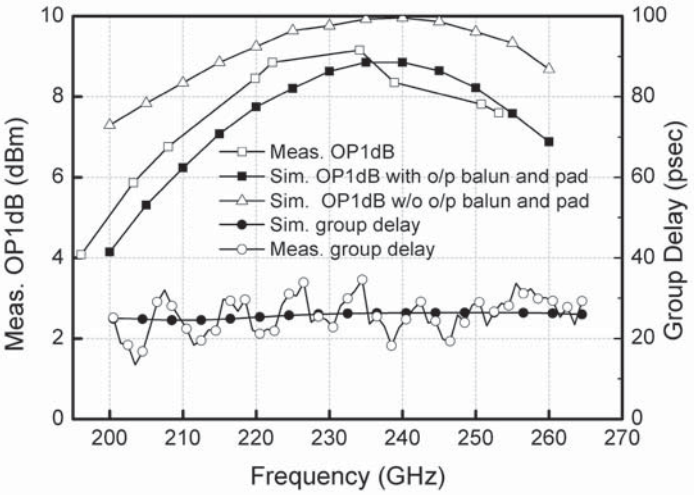

Figure 4.5.4: Simulated and measured output 1dB compression point and group delay variations across frequency.

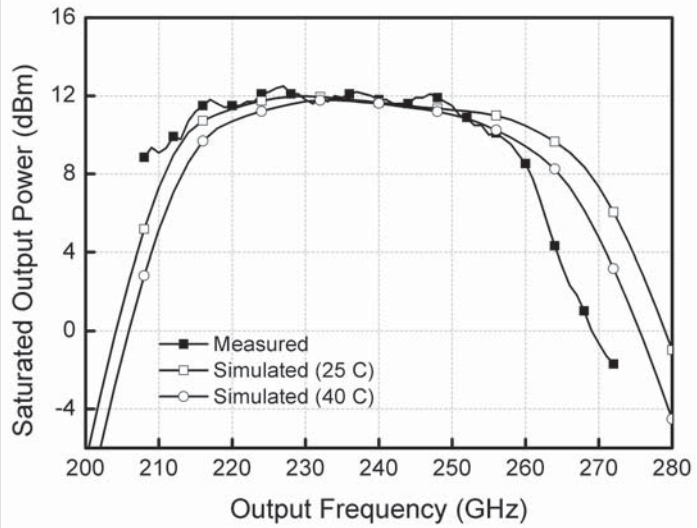

Figure 4.5.5: Simulated and measured saturated output power across frequency.

Reference	[1]	[3]	[4]	[5]	This work
Technology	130nm BiCMOS	65 nm CMOS	130nm BiCMOS	130nm BiCMOS	130nm BiCMOS
f_T/f_{max}	250/370	--	350/550	300/500	300/500
Power combinning Distributing structure	4-way zero-degree combiner Passive splitter	No	No	No	4-way zero-degree combiner Active splitter
-3dB BW (GHz)	200-220	251-263	228-258	208-258	200-255
Gain (dB)	25	9.2	10	9*	12.5* (15.5**)
Psat (dBm)	9.6	-3.9	5	0*	12* (13.5**)
OP1dB (dBm)	4	-5.5	--	-2.5	9* (10.5**)
DC Power (mW)	1824[1]	27.6	400	100	740
PAE at OP1dB (%)	0.14	0.89	--	0.5	1* (1.47**)
Max. Drain efficiency (%)	0.5	1.35	0.8[X]	1*	2.14* (3**)

*With no calibration for input and output baluns and pads.

** After calibration of input and output baluns and pads. (1.5dB for input and 1.5dB for output)

[1] Calculated from reported efficiency and saturate output power.

[X] Calculated from reported power consumption and saturated output power.

Figure 4.5.6: Performance comparison of silicon integrated PAs above 200 GHz.

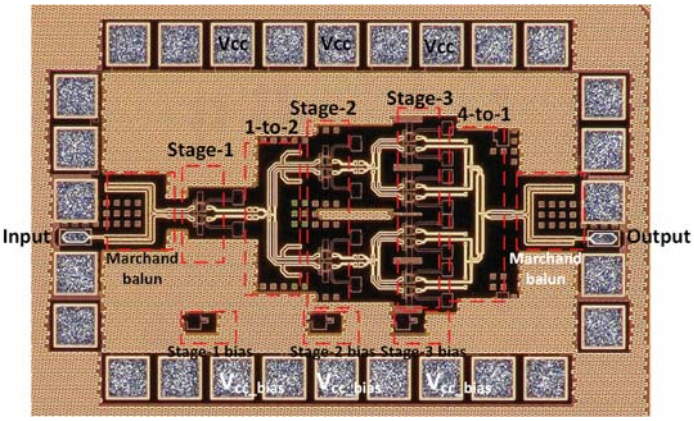

Figure 4.5.7: Die micrograph of the 4-way PA (Die area=0.83mm²).

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