6.5 A 64×64-Pixel Digital Silicon Photomultiplier Direct ToF Sensor with 100MPhotons/s/pixel Background Rejection and Imaging/Altimeter Mode with 0.14% Precision up to 6km for Spacecraft Navigation and Landing

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Recent technology surveys identified flash light detection and ranging technology as the best choice for the navigation and landing of spacecrafts in extraplanetary missions, working from single-point altimeter to range-imaging camera mode. Among all available technologies for a 2D array of direct time-of-flight (DTOF) pixels, CMOS single-photon avalanche diodes (SPADs) represent the ideal candidate due to their rugged design and electronics integration. However, state-of-the-art SPAD imagers are not designed for operation over a wide variety of scenarios, including variable background light, very long to short range, or fast relative movement.

A typical DTOF imager consists of a per-pixel time-to-digital converter (TDC) capturing the timestamp of the first detected photon [1]. However, in presence of background light, high dark-count rate (DCR), or long observation time, the probability of catching an unwanted event instead of the light echo becomes very high and the creation of pixel timing histograms is extremely inefficient. Delta-sigma operation as a method of filtering out the illumination signal [2] or very-low-DCR SPAD devices [3] mitigate the issue, but the light echo photons are still not identified. This is addressed in [4] by means of detection of photons occurring closely in time, but the required circuitry size does not allow implementation of this scheme in a 2D array structure, as needed for fast-moving spacecraft applications. Time gating is also a mitigating solution [5].

The proposed image sensor implements a pixel based on a digital silicon-photomultiplier (dSiPM), i.e., a set of SPADs providing on a single output a stream of short pulses corresponding to each avalanche, coupled to a smart triggering logic for concurrent-event detection, allowing uniquely correlated photons' time-stamping and counting.

The pixel architecture is sketched in Fig. 6.5.1: 8 SPADs with NMOS quenching and inverter front-end are combined together in a dSiPM, using monostables followed by an OR tree. The monostable pulse width determines the lower bound below which the events are merged and become undistinguishable. The circuit shown in Fig. 6.5.1 (inset), differently from the one used in [4], produces minimum-size pulses ensuring complete settling in all process corners thanks to the feedback loop, in a very small footprint. The OR tree is composed of alternating NAND and NOR gates for area saving and its output can be inhibited by a gating signal. The dSiPM output is analyzed by smart triggering logic, detailed in Fig. 6.5.1 (inset), which produces the stimulus for the TDC and counter. The TDC has two operating modes: (a) one for short range where an 8b ripple counter coarsely counts the global clock cycles and a ring-oscillator-based TDC finely measures the time from the event to the first clock edge after validation, and (b) one for long range where the 7b and 8b counters are chained and measure the number of clock cycles until the event detection.

The overall architecture of the 64×64 imager shown in Fig. 6.5.2 reveals a compact peripheral circuit, with decoders and serializers for byte-serialized 3×8-bit digital output. An additional row of pixels acting only as DCR monitors, with dSiPM output directly fed into an 8b counter increases testability and monitoring of SPAD DCR. Eventually, a PLL with a TDC replica is used to lock the pixel TDCs to a stable reference voltage. The imager operation can be described with the waveforms of Fig. 6.5.2: all pixels are reset and clocked simultaneously, and the pulses are optionally inhibited by the GATE signal for an initial period so as to reduce potential atmospheric and dust backscattering. Independent for each pixel, the dSiPM pulses activate the beginning of an asynchronous observation window, represented by the TRIG signal. The fine-resolution TDC is immediately started, while at each subsequent dSiPM pulse, the smart triggering logic compares the configured N_{ph} value to the number of pulses falling into the TRIG pulse width. If the threshold is reached, a validation signal TRIGOK is produced: the logic stops the TDC on the first global clock edge and inhibits the pixel operation until readout and reset. Otherwise, at the end of the observation window, TRIG returns to zero and a short RESINT pulse resets TDC and counter for subsequent triggers.

The chip, shown in the micrograph of Fig. 6.5.7, is fabricated in standard 0.15μm CMOS: SPADs are implemented with pplus on nwell diodes using non-minimum guardrings, a choice guaranteeing low crosstalk. In order to optimize the fill-factor, pixels are mirrored, sharing the deep nwell implant, and obtaining a pitch of 60mm with a fill-factor of 26.5%.

The final target system is schematically shown on the left of Fig. 6.5.3: the imaging mode employs flood illumination of the scene through a high-power laser at a wavelength of 532nm and images are acquired so as to characterize the surface before spacecraft landing. In the navigation phase, at a large distance from the surface, the laser is focused to implement the altimeter mode, where the sensor sees a spot of about 2×2 pixels in size. In both cases, a narrowband filter removes part of the background light. In order to reproduce this condition, a setup involving a delayed low-power laser at 470nm wavelength (where used SPADs have similar quantum efficiency with respect to 532nm) and a set of neutral-density filters with an additional background light source is tuned based on the final system specifications. The calculated power density, shown in the graph of Fig. 6.5.3, is employed in the following measurements.

Due to the high relative speed of the spacecraft, a measurement is composed of only 250 acquisitions, resulting in a very sparse histogram. Although very complex algorithms can be used, Fig. 6.5.4 shows the simple benchmarking method adopted, which provides a baseline for comparison of the sensor configurations: the histogram is first filtered with a moving average, which lowers isolated events, and then identifies the maximum. Its position in the histogram is then the center of a weighted average that takes into account the width of the laser echo. The rightmost part of Fig. 6.5.4 shows the images obtained with a distance measurement of 250 acquisitions, with an emulated echo at ≈164m, with different N_{ph} and background: it can be noted that N_{ph} = 1 fails dramatically with the 100Mph/s/pixel background, while correlation of 2 or 3 photons guarantees reliable operation. The smaller spot size for increasing N_{ph} is due to the Gaussian distribution of the intensity, lowering the probability of having 2 or 3 correlated photons at the periphery.

By applying the calculated attenuations and delays, the reliability of the measurement can be evaluated in almost the whole expected range: Fig. 6.5.5 reports the results of 10 distance measurements at 250 acquisitions, on a 8×8-pixel region at the center of the laser spot, in imaging and altimeter modes. The data processing is then applied to each single pixel in imaging mode, while in altimeter mode a 2×2 cluster is considered: when the algorithm did not obtain a maximum in the histogram, the measurement was discarded. The average precision and the accuracy of all valid measurements for each pixel or cluster is computed and shows reliable operation up to the specification of the operating modes, although with reduced measurement efficiency at the higher end of the range for high background conditions. In the altimeter mode with background, the whole range can be covered by setting N_{ph} = 3.

The power consumption of the digital electronics amounts to 47.7mW and is mainly determined by the distribution of the clock and the TDC counters, while the SPAD high-voltage supply consumes 45.8mW in typical operation, and depends on the illumination conditions. The chip performance is summarized in Fig. 6.5.6.

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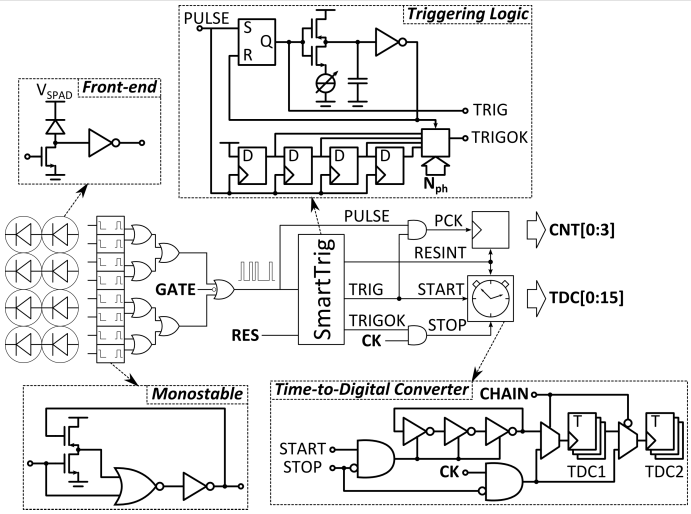

Figure 6.5.1: Pixel high-level schematic with detailed insets for the main blocks: SPAD front-end, monostable, smart triggering logic, time-to-digital converter.

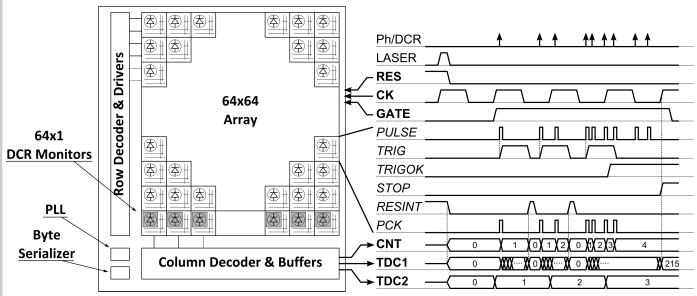

Figure 6.5.2: Architecture of the imager and waveforms describing the sensor operation: in bold, externally driven/readable global signals, while the italic names are pixel internal signals. The example is given for 3 correlated photons in the short-range operating mode.

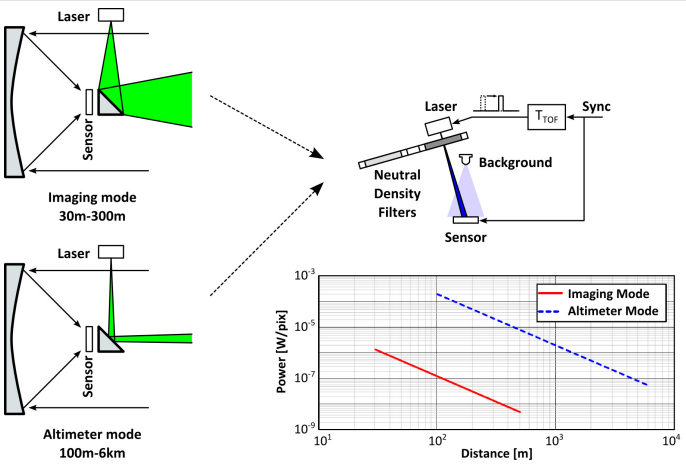

Figure 6.5.3: Characterization of the sensor: the final system configuration is shown, with the two operating modes, and the laboratory setup used to reproduce the same power density and pulse delay conditions. The graph shows the power density on the pixel for a 50% reflectivity target.

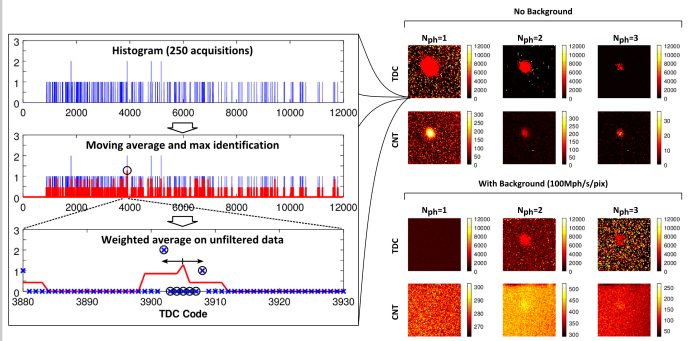

Figure 6.5.4: Sensor data acquisition and processing in imaging mode. In the inset, a pictorial description of the algorithm applied on 250 acquisitions. Images show the resulting TDC and intensity of the laser spot, with and without strong background of 100Mph/pixel.

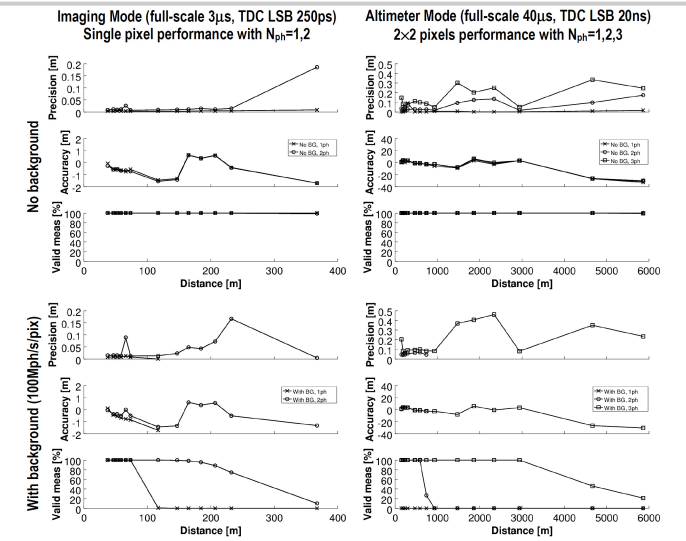

Figure 6.5.5: Results of range measurement with the emulated laser attenuation and delay for a 50% reflectivity diffusive target.

Parameter	Note	Value	Unit
Chip characteristics			
Array resolution		64×64	
Technology		CMOS 150nm 6M	
Chip size		4.4×4.4	mm^2
Pixel pitch		60	µm
Pixel fill-factor		26.5	%
SPAD operating voltage	V_{exc}=3.0V	21.8	V
SPAD median DCR	V_{exc}=3.0V	6.8	kHz
TDC resolution	Imaging mode Altimeter mode	250 20	ps ns
TDC depth	Imaging mode Altimeter mode	16 15	bit bit
Max frame rate (1 point)		1920	fps
Frame rate (250 points)	Imaging mode Altimeter mode	7.68 7.16	fps fps
Power consumption	Digital 1.8V, 3.3V SPAD 21.8V	47.7 45.8	mW mW
Emulated distance measurement performance			
Distance range	Imaging mode Altimeter mode	367 5862	m m
Precision (σ)	Imaging mode Altimeter mode 	<0.2 <0.13 <0.5 <0.14	m % m %
Accuracy	Imaging mode Altimeter mode 	<1.5 <0.37 <35 <1.9	m % m %
Background flux		100	Mph/s/pix

Figure 6.5.6: Chip performance summary table.

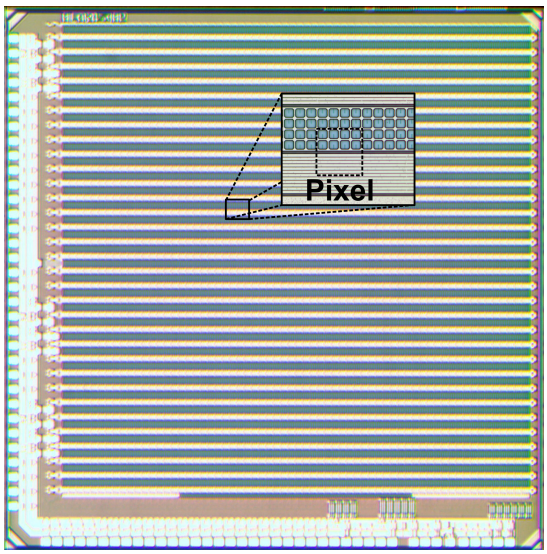

Figure 6.5.7: Chip micrograph.

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