Understanding the Regenerative Comparator Circuit

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***Abstract*—The regenerative comparator circuit which lies at the heart of A/D conversion, slicer circuits, and memory sensing, is unstable, time-varying, nonlinear, and with multiple equilibria. That does not mean, as this paper shows, that it cannot be understood with simple equivalent circuits that reveal its dynamics completely, and enable it to be designed to specifications on static and dynamic offset and noise. The analysis is applied to the StrongArm latch.**

I. Introduction

Flip-flops used as regenerative amplifiers are found everywhere in electronic circuits. It is well-understood that they have two stable states, and that given sufficient time, the circuit will regenerate an input voltage unbalance to reach one of these states.

The latched comparator must be symmetric by its very nature, since its binary states are symmetrical. Practical unbalances in the circuit arising from transistor and load mismatch lead to uncertainty in the regenerated binary output when a small analog input is applied. This problem of offset is well-known to circuit designers, and since the observed offsets can be much larger than in simple linear amplifiers, a certain mystery attends to "dynamic offsets" that appear only in a latched comparator.

This paper clears much of the mystery by visualizing regeneration. By using one trajectory as a frame of reference, circuit unbalances can in most cases be modelled by a sequence of linear, time-varying equivalent circuits that capture, piecewise, the variation of the circuit with time. Thus, simple expressions are obtained for all offsets, and a straightforward method emerges to null them to a desired accuracy at very small cost in power or chip area.

II. The Static Latch

Any discussion of a regenerative amplifier must start with the CMOS static latch (Fig. 1). This is a classic circuit: simple, uncluttered, and therefore easily understood. The only choice lies in the method whereby a small analog input is coupled into the latch without disturbing regeneration. Here, the two load capacitors C_L are pre-charged to a common voltage, on which is superposed a small differential voltage. That is, the voltage V_{O1} is slightly larger than V_{O2}, while their average voltage, in this example, is chosen slightly lower than V_{DD}. The pre-charged capacitors are switched into the latch (it will be seen that there are *only* two nodes in the circuit), and the circuit regenerates this difference to the voltage rails. The regeneration waveform (Fig. 1) is familiar to almost everyone who designs circuits. The existing literature does not give a satisfactory explanation for the one striking feature of every

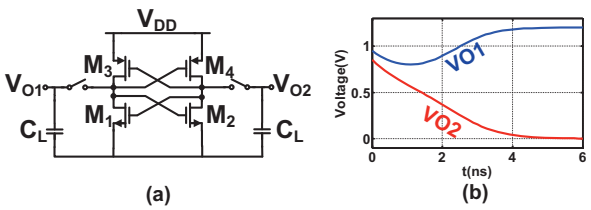

Fig. 1. (a) Schematic of a static latch; (b) Voltage waveforms in a static latch.

regenerative waveform: Why do V_{O1} and V_{O2} fall together, and then at some critical time, they peel away and separate? To find the answer we create a phase portrait of this circuit [1, Ch. 11]. The independent capacitors define two state variables, but using the capacitor voltages as state variables can obscure the essential properties. Instead, we take the average of the capacitor voltages as one state variable, the common-mode voltage V_{OC}, and their difference V_{OD} as the other. These are orthogonal quantities, in the sense that one can change while the other remains constant. The phase plane has been used before to investigate latch dynamics [2], [3], but not defined by the circuit modes. As will soon be clear, this choice makes all the difference.

A. Phase Plane

The phase plane is defined by axes V_{OC} vs. V_{OD} (Fig. 3). It is covered by a *vector field* that is signified at every point (V_{OD}, V_{OC}) on the plane by an arrow with the magnitude and direction of the ratio $(dV_{OC}/dt) \div (dV_{OD}/dt)$, where each time derivative at that point is obtained from the circuit equations. Starting from any initial condition in the plane, there develops by connecting the vector field a unique integral curve which depicts graphically how the state variables will change with time.

The vector field that fills the phase plane can equally well describe a nonlinear differential equation, or a linear one. Sometimes linearity will apply in a limited region of the plane. In that region any integral curve can be decomposed into a superposition of two eigenvectors. In turn, each eigenvector can be associated with the natural response of some linear circuit. For the static latch, as it turns out, linearity is a very good assumption over much of the excursion of V_{O1}, V_{O2}, particularly over the *one* integral curve that will interest us. If $\beta_N = \beta_P$ where $\beta \triangleq \mu C'_{ox} W/L$ for the CMOS inverters, then the overall G_m of the inverter remains almost constant except near $\frac{1}{2}V_{DD}$. At low V_{DD} this appears a small local deviation. The equivalent circuit that is produced by replacing each CMOS inverter with a constant G_m voltage-controlled current source Fig. 2 resembles a differential amplifier, but the cross-coupled controlling voltages identify it as a flip-flop. C_p

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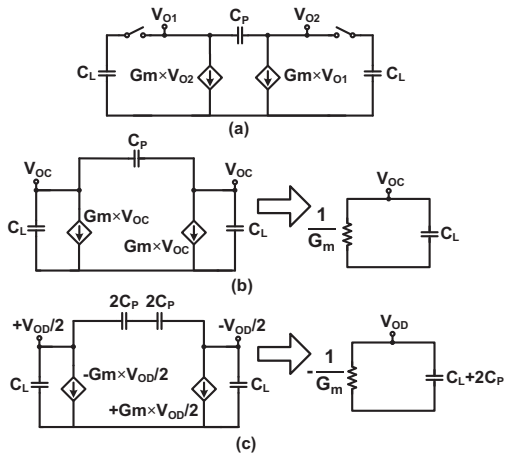

Fig. 2. (a) Equivalent circuit of a static latch; (b) Common-mode equivalent circuit; (c) Differential mode equivalent circuit.

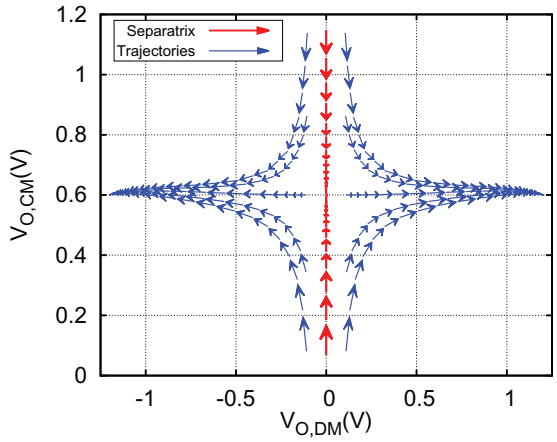

Fig. 3. Phase plane plot of a static latch. V_{DD}=1.1 V.

is a net cross-coupling capacitor between the two nodes arising from FET capacitance. We have deliberately left out the output conductance g_{ds} of the FETs since it makes little difference to the analysis that now follows.

B. Equivalent Circuits for Modes

A decomposition into common-mode and differential mode will also guide the search for meaningful equivalent circuits. Since these modes are independent, any response of this linear circuit can be decomposed into a superposition of the two modes. If the symmetric equivalent circuit (Fig. 2) is operating purely in common mode, then $V_{O1}(t) = V_{O2}(t)$. Since by symmetry no currents will flow through C_p, the circuit can be bisected into two half circuits. It is clear that the natural response of the two halves of the circuit in common mode is stable, with a pole located at $s_C = -G_m/C_L$. On the other hand, if the symmetric circuit is operating purely in differential mode, then $V_{O1}(t) = -V_{O2}(t)$. Symmetry now dictates that the mid-plate potential in the capacitor C_P remains zero. After bisection into half circuits, each half consists of a capacitance $C_L + 2C_P$ across a negative conductance $-G_m$. Now the natural response of the two halves is *unstable*, defined by a pole located at $s_D = +G_m/(C_L + 2C_P)$.

Each mode will be stimulated by its own initial condition. Therefore the time response to any initial condition $V(0) = V_{OC}(0) + V_{OD}(0)$ may be expressed as a superposition of the common and differential modes that are stimulated:

$$V_{O1,2}(t) = V_{OC}(0)\exp\left(-\frac{G_m t}{C_L}\right) \pm \frac{1}{2}V_{OD}(0)\exp\left(+\frac{G_m t}{C_L + 2C_P}\right) \quad (1)$$

This expression lends understanding to the example integral curves plotted on the phase plane. The vertical trajectories start from an initial condition $V_{O1} = V_{O2}$ that does not stimulate the differential mode. The trajectories lead into an equilibrium point at the coordinates $(0, \frac{1}{2}V_{DD})$. On the other hand if the output nodes are initialized so that $V_{OD} \neq 0$ but $V_{OC} = \frac{1}{2}V_{DD}$, that is, the circuit is released from an initial condition that is in purely differential mode, the horizontal trajectory in the phase plane accelerates away from this equilibrium point. If the circuit were truly linear this trajectory head towards $V_{OD} \to \pm\infty$. But in the actual circuit the node voltages cannot exceed the supply or ground, so as these trajectories approach the coordinates $(+V_{DD}, \frac{1}{2}V_{DD})$ and $(-V_{DD}, \frac{1}{2}V_{DD})$ they slow down to come to rest at one of these two equilibrium points. These last two equilibria are *stable*. However, the equilibrium at $(0, \frac{1}{2}V_{DD})$ is *metastable*: only if the circuit is initialized along the common-mode axis will it approach the equilibrium; otherwise, for any other initial condition, it will be deflected away from it towards one of the two stable equilibria. In phase plane terminology, the metastable equilibrium defines a saddle point.

Using the phase plane, we are able to understand the characteristic time-domain waveforms of a static latch. In a typical use, the latch is initialized with both nodes connected to, or biased close in voltage to, the power supply. This defines a large initial common mode. A small differential voltage is superimposed to direct the latch regeneration. On the phase plane this may correspond to the initial condition of the trajectory on the upper right. The large initial common mode will decay towards the metastable point, but the small differential mode will grow exponentially. The resulting trajectory is a superposition of the stable eigenvector which lies on the vertical axis, and the unstable eigenvector on the horizontal axis. Because of the large initial condition, the stable eigenvector dominates at first causing V_{O1} and V_{O2} to decay together. Then, as the unstable eigenvector grows, the differential voltage becomes dominant, causing the two voltages to split apart until the circuit reaches a stable equilibrium point. The turnaround point in the $V_{O1}(t)$ waveform, defined by its minimum value, corresponds to that point on the phase plane trajectory where the slope of the vector field is 0.5 in magnitude.

C. Circuit Imbalances

Offsets are important when the latched comparator is used in analog-to-digital conversion. Indeed, even in memory sense applications, offsets in the sense amplifier can be so large as to pose a threat to reliable readout. In a nominally symmetric circuit, offsets arise from parameter mismatch in corresponding pairs of elements, such as in the threshold voltage V_t of

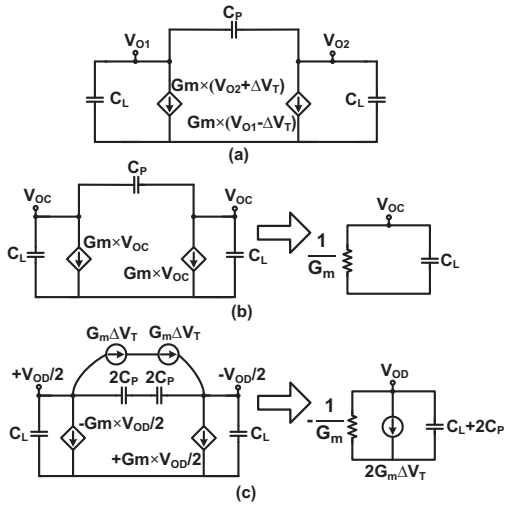

Fig. 4. (a) Equivalent circuit of a static latch with ΔV_T; (b) Common-mode equivalent circuit; (c) Differential mode equivalent circuit.

the NMOS pair, or in the capacitance of the loads C_L. All unbalances appear as an input-referred offset voltage, which we now seek to estimate by simple analysis.

As we investigate the effects of unbalances, it is desirable to continue analysis in terms of half circuits. Middlebrook shows how to treat parameter unbalances in *static* symmetric circuits [4] as equivalent half circuits; we extend this to *dynamic* circuits.

1) Mismatched Trip Points: Let us denote the nominal trip point of each inverter as V_T. This is the point on its static I/O characteristic at which the input and output voltages are equal. In a well-designed inverter, $V_T = \frac{1}{2}V_{DD}$. Suppose that due to random spreads in threshold voltages, the trip points of the two inverters are unequal. Without loss of generality, we ascribe a deviation $+\Delta V_T$ to the trip point of one inverter and $-\Delta V_T$ to the other. The latch comprising these mismatched inverters has its metastable point at $V_{OC} = \frac{1}{2}V_{DD}$ but $|V_{OD}| = 2\Delta V_T$. That is, the metastable point is translated from its nominal position on the phase plane. Next we show how this mismatch will affect the vector field on the entire phase plane. First we identify the *separatrix* trajectory that leads into the metastable point. This we can do with the aid of equivalent circuits. To the first order the transconductance G_m of the two inverters remains matched for small ΔV_T. Now the linear equivalent circuit is as shown in Fig. 4. If the outputs are separated into modes, this circuit is equivalent to two circuits, one for the common mode and the other for the differential mode. The main point is that $2\Delta V_T$ appears *only* in the circuit for the differential mode an *independent* current source. By definition, the separatrix is that trajectory on the phase plane along which the unstable mode is *not stimulated*. The unstable mode, which results in a growing exponential, arises in this circuit when the negative resistor $(-1/G_m)$ exchanges energy, or interacts, with a capacitor. But suppose the capacitors C_L were precharged (with the appropriate sign) to $2\Delta V_T$. Then the independent current source would find a return path through the two negative resistors, and no current flows through the capacitors. The unstable mode is not excited. Therefore, if the circuit

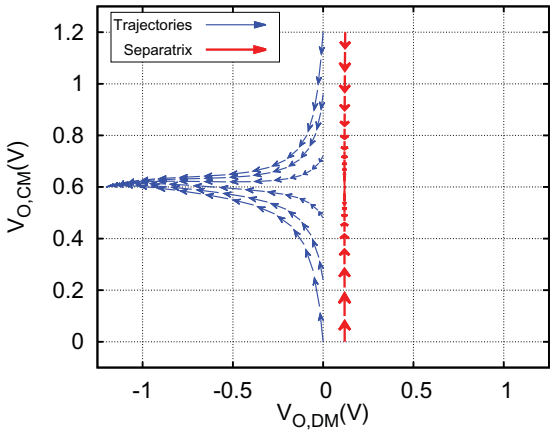

Fig. 5. Phase plane of a static latch with V_T mismatch

is released from an initial condition with any common-mode voltage but a differential voltage of $2\Delta V_T$, the common mode will decay into the metastable point and the differential voltage will remain constant for all time. In short, the separatrix that in the balanced circuit was vertical and coincident with the axis $V_{OD} = 0$ is now, in the presence of mismatched trip points, *translated* by $2\Delta V_T$. An offset of this amount has appeared in the circuit.

2) Mismatch in G_m: Random spreads in FET β will cause mismatch in the transconductance of the two inverters. Writing the transconductances as $G_m \pm \Delta\frac{1}{2}G_m$, we use equivalent circuits to examine the effects of this mismatch. We will assume that the trip points are matched, which means that the metastable point remains at the same location on the phase plane as for the balanced circuit.

In the common-mode equivalent circuit (Fig. 6), this mismatch introduces an error current $\Delta\frac{1}{2}G_m V_{OC}(t)$ connected in a way that is itself clearly *not* in common-mode. The error current source belongs in the differential mode circuit. Removing this current source restores symmetry to the common-mode circuit, and it is readily seen that if the circuit is initialized with some common mode voltage $V_{OC}(0)$, this will decay into the metastable equilibrium value with a time constant set by the real pole $s_C = -G_m/C_L$.

The current owing to the mismatch ΔG_m appears in the differential mode equivalent circuit as an *independent* source because it is not affected by any of the variables in this circuit. It acts to *cross-couple* the modes [4]. The source waveform must follow the decay of the common mode. We ignore the small perturbation of ΔG_m on $-G_m$. The differential mode's natural response is unstable, caused by a negative conductance charging the shunt capacitance $C_L + 2C_P$. However if at every instant the independent current source carries exactly the sum of the currents through these two elements, then they will not interact and the unstable mode will not be excited. The states of the circuit will follow the separatrix into the metastable point. This requires that the differential voltage is initialized to a $V_{OD}(0)$ such that

$$(-G_m - s_C(C_L + 2C_P))\,V_{OD}(0)e^{-s_C t} = \Delta G_m V_{OC}(0)e^{-s_C t}. \quad (2)$$

Assuming $2C_p \ll C_L$, this condition relates the initial condi-

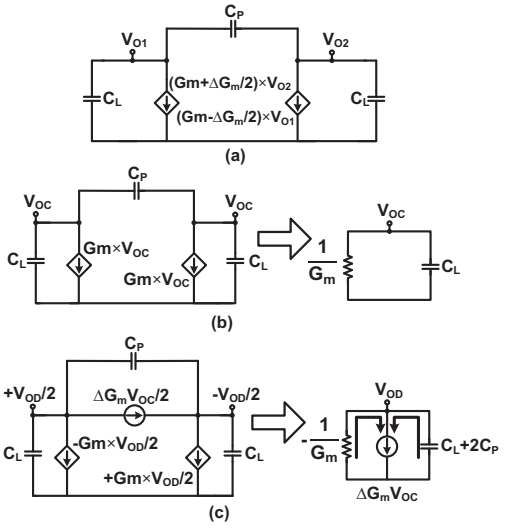

Fig. 6. (a) Equivalent circuit of a static latch with ΔG_m; (b) Common-mode equivalent circuit; (c) Differential mode equivalent circuit with coupled source from common mode circuit.

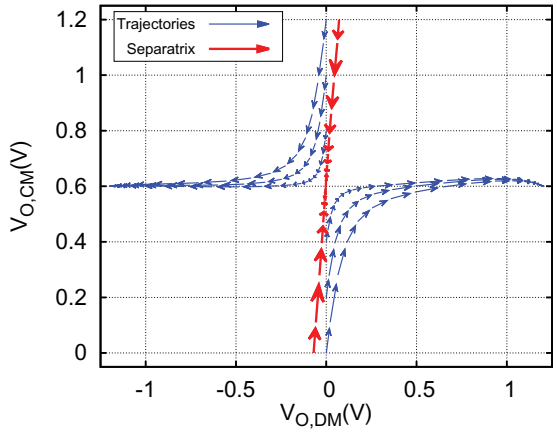

Fig. 7. Phase plane of a static latch with G_m mismatch

tions:

$$V_{OD}(0) \simeq (\Delta G_m/2G_m)\, V_{OC}(0) \tag{3}$$

If the output nodes are initially pulled up to the supply voltage, then $V_{OC}(0) = V_{DD}$. For the latch not to regenerate to '1' or '0', an initial differential voltage given by (3) must be applied at the same time. *This is the offset caused by mismatch in* G_m. It is called a *dynamic* offset because it changes with the initial common mode forced at reset, which here depends on the supply voltage. On the phase plane, this means that the separatrix is *rotated* from a vertical line (Fig. 7).

3) Mismatch in Capacitors: Suppose all corresponding pairs of FETs are matched, but the load capacitors are mismatched. This is modelled by unequal capacitors $C_L \pm \frac{1}{2}\Delta C_L$ connected to the two outputs.

Again, this capacitor unbalance will introduce a cross-coupling current source that cross-couples the common mode waveform into the differential mode with a magnitude of $s\Delta C_L V_{OC}(s)$. Its effect, just like for G_m unbalance, is to rotate the separatrix, and to introduce an offset which depends on

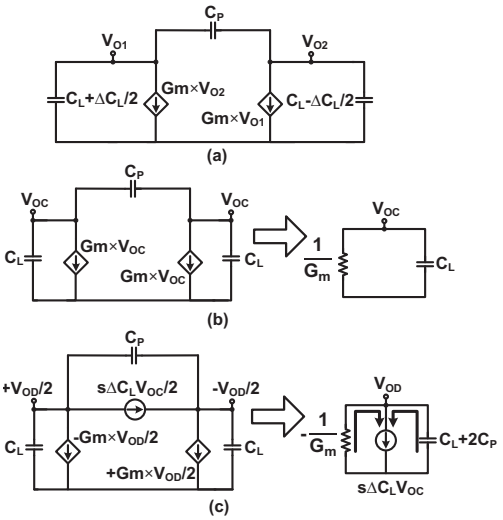

Fig. 8. (a) Equivalent circuit of a static latch with ΔC_L;(b) Common-mode equivalent circuit;(c) Differential mode equivalent circuit with coupled source from common mode circuit.

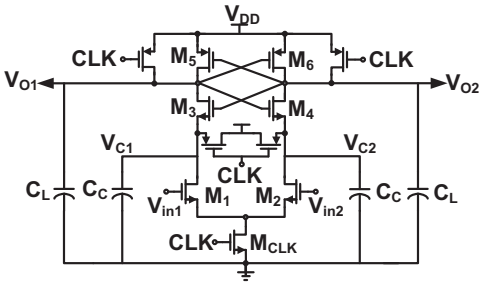

Fig. 9. Schematic of the StrongARM latch.

the initial value of the common-mode voltage as determined by the reset action:

$$\frac{V_{OD}(0)}{V_{OC}(0)} \simeq \frac{\Delta C_L}{2C_L + 2C_P} \tag{4}$$

This is another dynamic offset. (4) is consistent with [5], but here this result is arrived at much more straightforwardly.

III. StrongArm Latch

This widely used latching comparator circuit in Fig. 9 was originally presented as part of a suite of low-power digital circuits [6]. It offers a convenient method to couple a voltage to be regenerated into a pair of cross-coupled inverters—the main weakness of the CMOS static latch—while guaranteeing zero static power consumption when regeneration is complete. It gained widespread attention after it was used in the StrongARM microprocessor.

A survey of the literature suggests that in spite of widespread use, the detailed action of the StrongARM latch is, even now, poorly understood. Without a full understanding it cannot be used properly as a low offset comparator. Therefore, we will first explain how, in correct operation, the circuit traverses two phases over which the applied voltage is amplified before regeneration will start. When poorly designed, an internal regeneration can be triggered as early as in the

second phase, but with the undesired consequence of a larger offset.

A. Overall Operation

We will describe the circuit in terms of how its operation is most widely understood.

The difference between two input voltages, as measured with respect to ground, is coupled into the latch through the NMOS pair M1-M2. The pair is activated by the tail FET, M_{CLK}, which is assumed to act like a switch. The input voltage common-mode (V_{IC}) must lie above the threshold voltage of M1,M2 to set the bias current.

The bias current also flows through the cross-coupled inverters, M3-M5 and M4-M6, that are stacked in series. Differential current produced by M1-M2 "unbalances" the inverter, causing it to regenerate on this unbalance. Regeneration forces one FET in each inverter to turn OFF, thus choking off a current flow path through both M1 and M2. Thus M1, M2, and the tail current FET are all forced into deep triode with $V_{DS} = 0$ where they no longer conduct current. The comparator consumes no static power in its regenerated state.

This description is sufficient to see why the StrongARM latch is popular today. A closer analysis is needed to understand aspects such as the circuit's inherent latency before it regenerates, and how unbalances in the circuit elements will cause static and dynamic offsets.

B. Operational Phases

The circuit's operation should be divided into three discrete phases, with regeneration understandably taking place in the last phase. In the first two phases, sampling and propagation, the circuit amplifies the applied differential voltage on to internal nodes, as we now explain.

1) Reset State: The phases are most clearly identified when the comparator is released from a well-defined state. The circuit is defined by four state variables, the voltages on two grounded capacitors C_C and on two load capacitors C_L. But it is a time-varying circuit, and in the second and third phases the capacitors exchange charge, collapsing the number of states to two. Be that as it may, the circuit must be initialized with all four states at a predetermined and fixed value so as to erase memory of the previous regeneration. A convenient initialization is to precharge all four capacitor voltages through FET switches to the supply voltage V_{DD}. This initializes the source and drain terminals of M3-M6 all to the same potential.

2) Sampling Phase: The input voltages V_{in1} and V_{in2} are being applied when the tail current transistor M_{CLK} is initialized. The average input voltage sets the bias current (I) through M1 and M2. This common-mode current will be forced to discharge C_{C1} and C_{C2}. M3 and M4 will remain OFF until the capacitors have discharged by an amount equal to the threshold voltage V_{tN}. This period of time defines the sampling phase,

$$T_{smp} = C_C V_{tN} / I \tag{5}$$

Over this period the difference in the input voltages V_{ID}, which creates a differential current $g_{m1} V_{ID}$, integrates a differential voltage across the capacitors C_C of

$$v_{smp} = (g_{m1} V_{ID} \times T_{smp}) \div (½ C_C) \tag{6}$$

This differential voltage serves as the initial condition for the next phase, propagation.

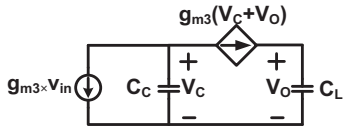

Fig. 10. Differential half circuit during propagation phase of the StrongARM latch.

3) Propagation Phase: In propagation phase, M3 and M4 will turn ON, and by the end of this phase the common mode (bias) current flowing through them will have discharged both output voltages V_{O1} and V_{O2} by V_{tP} to turn on the cross-coupled PMOS pair M5, M6. During this phase M1,M2 and M3,M4 are ON. The voltages on capacitors C_C and C_L will ramp down together, separated by the constant difference of $V_{GS3} (= V_{GS4})$. Thus,

$$T_{prp} = (C_L + C_C)|V_{tP}|/I \tag{7}$$

Although the gates of M3,M4 are cross-coupled to the drains, in common mode the pair of gates follows the same voltage waveform as the pair of drains, as if each FET was diode connected. The cross-coupling becomes evident in differential mode. A cross-coupled pair of transistors will only regenerate if the loop gain is greater than one. This is not so when, as we have assumed, M1,M2 remain in saturation through the propagation phase, and $C_C < C_L$. This is readily proved by replacing M3,M4 with a transconductance g_{M3} in the linearized equivalent circuit of Fig. 10, and representing M1,M2 with a constant current source. The cross-coupling shows in the control variable of g_{M3}, which instead of being the familiar difference of two voltages, each measured with respect to ground, is now their sum. The voltages v_C and v_O are the differential voltages across C_C and C_L, respectively. The two capacitors in this equivalent circuit are in series and it has a single pole in the left half s-plane at

$$s_{prp,dm} = -g_{M3} \div ((C_L C_C)/(C_L - C_C)) \tag{8}$$

When $C_C < C_L$, this cross-coupled NMOS pair will act as a stable amplifier. This simple circuit of Fig. 10 can amplify because the cross-coupling introduces a controlled amount of positive feedback, which, as we have just shown, stops short of outright regeneration.

Provided M1,M2 remain in saturation, the dominant effect over the propagation phase arises from the transimpedance that converts the input pair current, $g_{M1} v_{in}$, to the output voltage v_O. This is defined by integration of a current on to the load capacitor C_L over a time window defined by T_{prp}, with a boost provided by the cross-coupled NMOS pair M3,M4. In addition there is a redistribution of the charge acquired at the end of the sampling phase, through the cross-coupled M3.M4 into C_L. This last effect accounts for the coefficient of 2 in the numerator of the expression for output voltage:

$$V_{OD} = \left(\frac{C_L + 2C_C}{C_L - C_C} \right) \left(\frac{V_{tN}}{I} g_{M1} \right) V_{ID} \tag{9}$$

4) Regeneration Phase: At the end of the propagation phase, the cross-coupled PMOS pair, M5,M6, turns ON and, since the sources are shorted, it will regenerate the differential voltage present at the output nodes. This voltage is, to a very good estimate, given by (9). The pole for PMOS pair lies in the right-half s-plane, and is given by

$$s_{reg} = +g_{M5}/C_L \tag{10}$$

The regenerated output voltages will grow to control all the FETs in the entire latch. At one of the two stable equilibria, one output voltage will reach V_{DD} and the other ground. No static current will flow on either side of the circuit. If the PMOS pair were to dwell at the metastable equilibrium and the supply voltage was large enough, then the output voltages would be equal $V_{O1} = V_{O2} = V_{DD} - V_{GS}(M5,6)$.

5) StrongARM Latch in Summary: This detailed analysis shows that the StrongARM latch, with all internal nodes initialized to V_{DD}, undergoes two phases of common-mode discharge before it regenerates. These phases amount to a delay of $(T_{smp} + T_{prp})$ before the circuit regenerates with the time constant given by the inverse of the pole frequency (10). Others have noticed that the StrongARM latch regenerates after some latency, or waiting period [7]. But our analysis shows that over this period of latency a useful internal amplification will take place. For the applied input voltage V_{ID}, the gain to the point of onset of regeneration is

$$\frac{V_{OD}}{V_{ID}} = 2\frac{C_L + C_C}{C_L - C_C}\frac{V_{tN}}{V_{P1,2}} \tag{11}$$

where $V_{P1,2}$ is the pinchoff, or overdrive, gate voltage on M1,M2. By substituting typical values into the two terms above, this gain is about $5 \sim 10$.

C. FET Mismatch

The internal gain is important for estmating offset because it amplifies unbalances in the input differential pair most, usually to the point that they will dominate all other FET imbalances in the circuit. This helps to identify the principal source of offset, and then to focus design effort for its mitigation. Both V_t and β mismatch in the input pair will appear at the comparator input as an effective V_{ID}.

D. Capacitor Mismatch

C_C and C_L, both grounded capacitors, are vulnerable to mismatch. To model their contribution to dynamic offset in the simplest way, we follow the method shown in the static latch analysis where capacitor mismatch induces a coupling from common-mode to differential-mode. Since the StrogArm latch operates by discharging both C_C from their reset condition by V_{tN} over the sampling mode, and then, by discharging C_L and C_C by $|V_{tP}|$ over the propagation phase, we expect small mismatch between corresponding pairs of these capacitors to induce significant (differential) mismatch over the large excursions of common mode.

The analysis is simplified considerably if the FETs M1,M2 are assumed to act like current sources throughout the propagation phase, because then we are dealing with a circuit with a cutset of capacitors only, which forms a dissipation-less conservative system. Conservative circuits are fully specified by the initial and final state, without regard to how the state changes in time. Thus, at the end of the sampling phase, because mismatch in the internal capacitors C_C introduces coupling between common and differential modes, a differential offset voltage appears across the C_C's of $(\Delta C_C/C_C)V_{tN}$. Then, during propagation, charge will exchange with the C_L capacitors through the cross-coupled pair M3,M4, and when $C_C < C_L$ (as is usual), the output will settle stably to a *voltage* that is amplified by $(1 - C_C/C_L)^{-1} > 1$, while total *charge*, of course, is conserved.

Thus, assuming $V_{tN} = |V_{tP}| = V_t$, the final offset due to capacitor mismatch alone is

$$v_{OD} = \frac{V_t}{(1 - C_C/C_L)}\left[\frac{\Delta C_L + 2\Delta C_C}{C_L}\right] \tag{12}$$

The term V_t at the head of the left-hand side reminds us that this is a dynamic offset induced by a common-mode excursion across an unbalanced circuit. The term $2C_C$ arises because C_C undergoes a common-mode voltage excursion of $V_{tN} + |V_{tP}|$, almost twice the excursion of the voltage on C_L. Fortunately this circuit rejects typical bounce in supply voltage, so its regeneration time, static offset, and dynamic offset all remain independent of V_{DD}.

E. Offset Compensation

With this background, we can explain comprehensively, and for the first time, how the offset calibration strategies first proposed in [8] for latched comparators will work. We have established that with zero differential input, mismatch in the threshold voltage and β of the pair M1,M2 will usually create the offset voltage at the output nodes according to (9), dominating contributions from mismatch in all other FETs. Now if the capacitances C_C and C_L are fine tuned in closed loop under digital control to create an almost equal offset but opposite in sign according to (12), the algebraic sum of the two offsets will cancel. So by introducing a deliberate and measured mismatch in the capacitors, the comparator may be made to appear offset-free even with random mismatch in the FETs .

The process is readily automated by applying a common-mode voltage to the two inputs of the comparator (zero differential input), which, due to inherent mismatches will cause the comparator to repeatedly produce either a '0' or a '1', then searching through binary-weighted arrays of small capacitors attached to C_C and C_L until the output of the latch changes state. That setting can be held in a register dedicated to each latch.

The expression (12) also shows a benefit of resetting the initial voltages across C_C to V_{DD}. In many practical cases the internal nodes at the drains of M1,M2 are not reset, but are instead pulled up to $V_{DD} - V_{tN}$ by the output nodes when they are reset. Indeed, resetting these nodes to V_{DD} prolongs the latency period by T_{smp} (see (5)), which seems undesirable. But (12) reveals that as a result of this delay ΔC_C is twice as effective in compensating offset. Thus, at the expense of

a larger latency, a lighter capacitor loading may be used for offset compensation.

But doesn't the greater latency annul the benefit of a lighter capacitor loading? To answer this question, we examine the critical comparator in an A/D converter. A comparator is in critical condition when it is resolving an input so close to a threshold that regeneration may not complete in the allotted clock phase; that is, the converter would make a metastability error. This is limited by the regeneration time constant, seldom latency. In the StrongARM latch it is the PMOS pair M5,M6 that regenerates, and in the initial part of the regeneration transient it is loaded only by C_L. When C_C shoulders the larger burden of compensating latch offset, the latch regeneration time constant is essentially unchanged. When the offsets are large, a better balance between latency and regeneration may require that the calibration arrays are more evenly distributed between the C_C and C_L nodes.

F. Range of Input Common Mode

Our survey of the published uses of the StrongARM latch shows that in most circuit realizations, the input common mode voltage is chosen poorly. This can degrade offset quite considerably for the reasons that we will now explain. This was observed experimentally in an early use of the latch as an SRAM sense amplifier [7].

Over the sampling and propagation phases, the input common-mode voltage (V_{IC}) sets the bias current through M1-M4, but also determines whether or not these FETs operate in saturation. This is best understood in a perfectly balanced, offset-free latch with zero differential input, which upon release from reset should travel into its metastable state. It is sufficient to examine the state of the circuit when the regenerative pair M5,M6 starts to conduct, i.e. when $V_{O1} = V_{O2}$ reach $V_{DD} - |V_{tP}|$. Since this excursion is purely in common mode, M3,M4 will behave as if they are diode connected and therefore they will operate in their saturation region. But for the input pair M1,M2 to operate in saturation, V_{IC} must not exceed the upper limit

$$V_t < V_{IC} < V_{DD} - V_{GS}(\text{M3,M4}) \tag{13}$$

What if V_{IC} is larger? Then at some point during the propagation phase M1,M2 will be pushed into their triode region. Now consider that an input differential voltage, V_{ID}, is being applied—this may well represent an equivalent offset—and divide the propagation phase into two sub-phases: over the first sub-phase M1,M2 appear like a differential current source $g_m V_{ID}$; and over the second sub-phase they appear like a resistor $1/g_m$. This is a piecewise simplification of a circuit that, over time, is pushed from saturation into deep triode, and it is captured by two different equivalent circuits over the sub-phases (Fig. 11). They show that the benefits of an internal amplification in the latch, as we have argued above, are now eroded in two ways: the integration window while M1,M2 remain in saturation is now only a fraction of T_{prp}, which lowers the amplification; and the integrated voltage stored on C_C, also shared by C_L, leaks away through the resistor during the second sub-phase. Now mismatches in M3,M4 and M5,M6

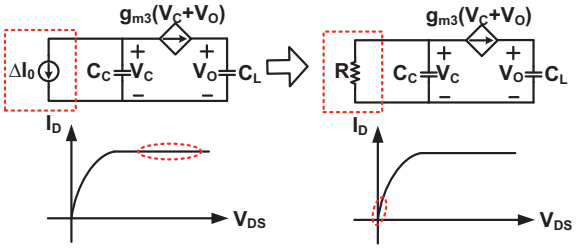

Fig. 11. Equivalent differential circuit during propagation phase when $M1\,\&\,2$ transit from saturation to triode region.

will add significantly to the mismatches of M1,M3, causing the total offset to double or more.

IV. Thermal Noise

Comparators are mainly limited by random or systematic offsets. But long-standing methods to circumvent offsets, such as overranging and digital error correction in multi-step A/D converters, are now running up against limits posed by low supply voltages. And although it might not be apparent today that thermal noise poses a bottleneck to performance, we expect it to be so once offset compensation in comparators is better understood and being widely practiced.

There is some published work to model noise in the StrongARM latch [9], [10]. [10] identifies the operational phases of this circuit correctly, but it uses a method of noise analysis that is too indirect to yield some key insights: for instance, that the input common mode must be chosen correctly (see Section III-F above) in order to minimize noise.

Our analysis of offset in the StrongARM latch, on the other hand, extends straightforwardly to a prediction of thermal noise. But first we must describe how noise will randomly trigger regeneration around the metastable point. In a perfectly balanced comparator with zero input applied, the noise current in the input pair M1,M2 will integrate on C_C during the sampling phase, and continue to integrate and amplify on C_L during the propagation phase. The random voltage integrated on C_L will trigger regeneration to '0' or '1'. Now integration of a white noise current with single-sided spectral density S_{in} on a capacitor C over a known time window T, for example T_{prp}, produces a voltage with variance [11, p. 331]

$$\langle v_n^2 \rangle = S_{in}\left(T/2C^2\right) \tag{14}$$

If the input common-mode does not exceed the limit in (13), the noise of the input pair will experience the largest amplification and it will account for most of the input-referred noise. Otherwise, for two reasons, the input-referred noise will grow larger: first, because of the lower g_m of M1,M2 since they are in triode region; and second, because M3,M4 will now contribute substantially to the total noise.

V. Comparison with Measured Data

All the expressions relating to static and dynamic offsets closely match the offset derived from transient simulations of the StrongARM latch as its input is swept. On the other hand, it is surprisingly difficult to find measured data in the many publications on this comparator in a form that could

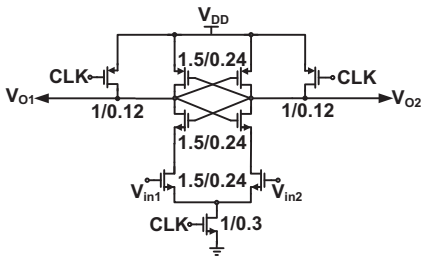

Fig. 12. Test circuit in [7]. All dimensions in μm, V_{DD}=1.5 V.

be used to validate the analysis developed in this paper: [7] is the exception, because it provides histograms measured across 45 samples of a latch realized in 130-nm CMOS. Notably the measured offset grows by more than $2\times$ when the input common-mode exceeds the limit specified by (13). The circuit in question is shown in Fig. 12. Table I shows that the measured RMS offset at two common-mode levels agrees very well with predictions from our analysis. This is more than a matter of making the numbers come out close; our predictions were made to verify certain hypotheses. Although Infineon fabricated the circuit being measured, we use publicly available mismatch coefficients taken from the TSMC 130 nm process.

For $V_{IC} = 0.7V_{DD}$ which lies within the range in (13), we assume that offset arises *only* from V_t mismatch and β mismatch in M1,M2. Since our prediction is very close (for this size of population) to the total measured offset, it verifies the hypothesis that due to internal amplification, M3-M6 will not contribute appreciably to mismatch. For $V_{IC} = V_{DD}$ the analysis is somewhat more complicated because the gain $V_{O1,2}/V_{ID}$ changes over the two sub-phases described in Section III-F. We use the simple mathematical device of averaging the gain over the two sub-phases, and including the offset from V_t mismatch in M3,M4 (β mismatch doesn't matter because these FETs are in series with M1,M2). The prediction in this case is accurate. In spite of the lower internal amplification, mismatch in M5,M6 still does not contribute. However, it is clear that too large a V_{IC} will worsen the comparator's offset considerably.

VI. Conclusion

We have developed a simple, physically-based analysis for the internal workings of a regenerative comparator. It recognizes the symmetry of the circuit, by identifying common mode and differential mode. The large-signal behaviour is readily understood by plotting equilibria and trajectories in the phase plane *defined by these modes*. It is most fruitful to consider comparator offset and noise as perturbations on the separatrix, the phase plane trajectory that leads from the initial reset condition into the metastable equilibrium. This brings clarity to long-debated distinctions between static and dynamic offsets in regenerative comparators. Simple equivalent circuits are shown to capture all time-varying aspects. For small offsets, nonlinearity in FET g_m does not change the shapes of the trajectories.

These insights guide design of the widely used StrongARM comparator. Following reset, three phases of operation are identified, with the role of pairs of FETs. An internal amplification is revealed, and from it follows the need to choose the input common-mode voltage correctly, for uses where the offset and noise should be kept very small. Most importantly, it is shown how by using a small array of switched capacitors, a dynamic offset can be made to cancel the static offset with little penalty on speedt. This calibration is robust against supply fluctuations.

Predictions from the analysis are validated against measurements taken on a prototype StrongArm comparator. The measurements illustrate the major design considerations to emerge from the analysis. Our analysis of offset and its implications on design is much more direct than previous work on the topic, such as [12].

We are grateful to Professor Bernhard Wicht of Reutlingen University, Germany, who shared sizes of the FETs in the SRAM sense amplifier that he had reported in a perceptive early work.

	$V_{IC} = 1.05V$	$V_{IC} = 1.5V$
Measured Offset	8.5 mV	19.0 mV
Calculated Offset	9.5 mV	19.1 mV
Due to $\Delta V_{t1,2}$	5.8 mV	5.8 mV
Due to $\Delta\beta_{1,2}$	7.4 mV	14.0 mV
Due to $\Delta V_{t3,4}$	2.0 mV	11.6 mV

TABLE I
MEASURED RMS OFFSET VS. CALCULATED. FET MISMATCH PARAMETERS: $A_{Vt} = 3.5\text{mV}\cdot\mu\text{m}$, $A_\beta = 2.5\%\cdot\mu\text{m}$.

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