6.8 A 90nm CMOS 60GHz Radio

Stephane Pinel, Saikat Sarkar, Padmanava Sen, Bevin Perumana, David Yeh, Debasis Dawn, Joy Laskar

Georgia Institute of Technology, Atlanta, GA

CMOS-based circuits operating at mm-wave frequencies have emerged in the past few years [1,2]. This paper discusses the integration of a 60GHz CMOS single-chip transmitter and a single-chip receiver using a standard 90nm CMOS technology demonstrating a reliable solution for 60GHz single-chip radio. Proper transistor layout, complete and accurate modeling and optimized parasitic extraction method enabled the robust design of the wideband super-heterodyne architecture to support the entire 57-to-66GHz band. The analog radio front-end is controlled by a serial digital interface and has been co-designed and integrated together with a high-speed digital signal processor including analog-to-digital conversion, high speed PHY signal processing such as frequency-offset compensation, phase tracking, FIR and DFE, to support both advanced OFDM and SCBT modulation scheme as shown in Fig. 6.8.1. The resulting single-chip solution enables data throughputs exceeding 7Gb/s (QPSK) and 15Gb/s (16QAM) for a total DC power budget of below 200mW in TDD operation. In combination with a low-cost FR4-based packaging technology (Fig. 6.8.1) [3], it provides a high-performance cost-effective solution for a wide range of high volume consumer electronic applications.

The 57-to-66GHz band is divided in 4 channels of 2160MHz, thus to support ultra-high throughput using 2 to 3 channel bonding, the IF frequency needs to be high enough, from 7 to 13GHz to avoid spectrum aliasing. Millimeter-wave low-loss micro-strip lines are modeled and provide lower loss than their coplanar waveguide (CPW) counterpart. In addition, bended micro-strip lines are chosen to enable more compact design while ensuring wideband performance and robustness to process variations.

In the single-chip transmitter, the baseband signal is first upconverted to IF using a double-balanced quadrature Gilbert-cell mixer (a differential inductor is used as the tuned load) and a quadrature VCO (controlled by a fixed PLL). An active differential-to-single-ended converter and a common-source digitally controlled VGA are driving a mm-wave resistive upconverter mixer to ensure good stability and good linearity up to 3dBm output P_{1dB} at the mm-wave mixer input for a measured total DC power consumption of 59mW. A push-push VCO, using 20µm width devices, is chosen to provide the LO frequency. The measured performance exhibit a wide tuning range from 49 to 55GHz (Fig. 6.8.2), and a phase noise of –95dBc/Hz at 1MHz offset. The DC power consumption of the VCO core and the VCO buffer is 30mW. High-frequency static master-slave dividers chain is used, then, below-1GHz conventional digital circuits are used to implement additional divider stages for the frequency-selection PLL consuming an additional 30mW. A three-stage power amplifier is implemented using 40 and 60µm width devices. A cascode topology is followed by a two-stage common-source to provide 17db gain at 60GHz. The power amplifier delivers +5.1dBm output P_{1dB} with 54mW DC power consumption, and has a 5.8% PAE and +8.4dBm saturated output power. The total DC power consumption is measured to be 173mW under 1.8V for an output power of 5dBm at 60GHz. The single-chip transmitter occupies 1.75×1.5mm^2 die area. The die micrograph, the simplified schematics of mm-wave PA and the push-push VCO are shown in Fig. 6.8.3. The performance summary of the transmitter is provided in Figure 6.8.4.

In the single-chip receiver, the two-stage single-ended cascode LNA exhibits a measured gain of 16dB over a 1dB bandwidth superior to 7GHz, a minimum noise figure of 6dB, output P_{1dB} of 1dBm for a DC power consumption of 29mW (Fig. 6.8.2). The LNA and the push-push VCO are combined with a dual-gate mixer, a cascode IF amplifier followed by a single-ended-to-differential amplifier and a differential wideband digitally controlled variable gain IF amplifier, providing a measured total conversion gain of 32dB on the quadrature demodulator capacitive load. The quadrature demodulator uses a double balanced Gilbert cell mixer pair in conjunction with a QVCO (controlled by a fixed PLL) and differential baseband amplifiers, providing an additional 19dB of gain. A high-speed low-power digital signal processor, not discussed in this paper, is integrated with the receiver and includes analog-to-digital conversion, high-speed PHY signal processing such as frequency-offset compensation, phase tracking, FIR and DFE, SCBT demodulation as well as advanced OFDM systems. The measured receiver exhibits a total conversion gain of 51dB for a noise figure of 9dB (from RF input to I/Q output) and total power consumption of 189mW. The single-chip receiver occupies 2.25×1.7mm^2 of die area. The die micrograph, simplified schematics of the mm-wave LNA and the QVCO are shown in Fig. 6.8.5. The performance summary of the receiver is provided in Fig. 6.8.6. An example of 7Gb/s QPSK demodulated measured eye diagram (I channel only), when activating the signal processor, is shown in Fig. 6.8.7. The analog transmitter and receiver front-ends are controlled (gain control, frequency and phase control, idle mode, …) by a serial digital interface.

Acknowledgements:
Authors would like to acknowledge DARPA for their support in this work. This material is based upon work supported by DARPA and SPAWAR under Award No. N66001-06-1-2033." Any opinions, findings, and conclusions or recommendations expressed in this publication are those of the authors and do not necessarily reflect the views of the SPAWAR.

References:
[1] T. Yao, M.Q. Gordon, K. K. W. Tang et al., "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044-1057, May 2007.
[2] S. Emami, C. H. Doan, A. M. Niknejad and R. W. Brodersen, "A Highly Integrated 60GHz CMOS Front-End Receiver," *ISSCC Dig. Tech Papers*, pp 190-191, Feb. 2007.
[3] J. Laskar, S. Pinel, D. Dawn, S. Sarkar, B. Perumana and P. Sen, "The Next Wireless Wave is a Millimeter Wave," *Microwave Journal*, vol. 50, no. 8, pp. 22-36, August 2007.

 978-1-4244-2011-7/08/$25.00

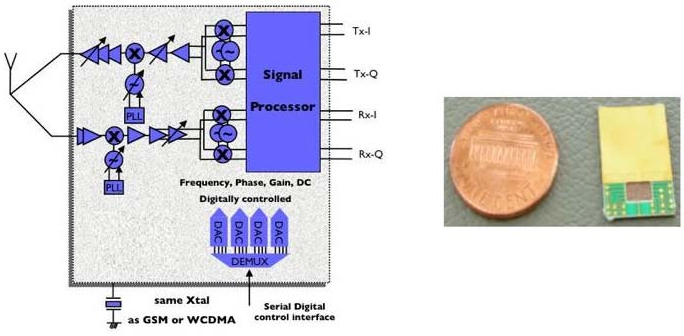

Figure 6.8.1: 60GHz CMOS single chip radio block diagram and FR4-based integrated antenna module solution.

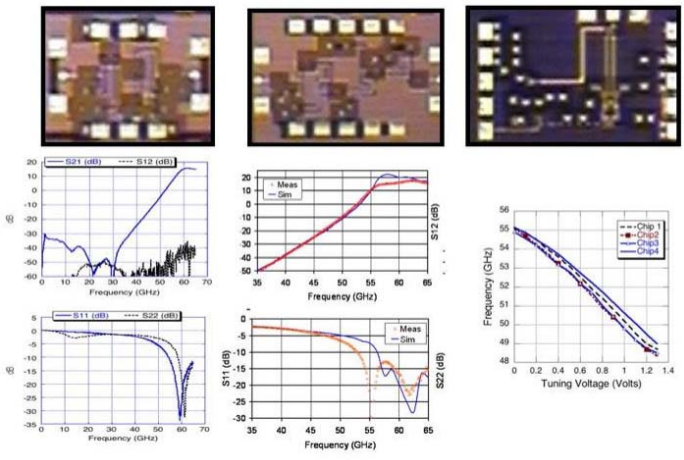

Figure 6.8.2: 60GHz CMOS LNA, PA and VCO test die micrographs and measured performances.

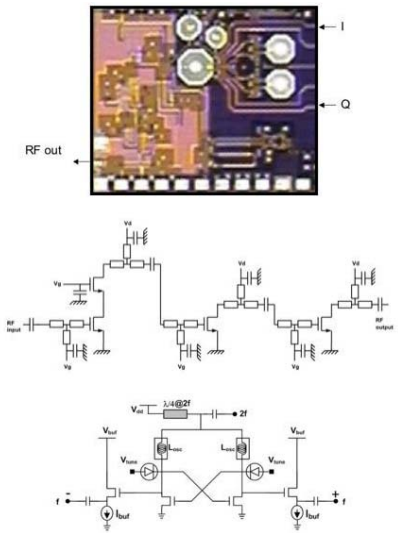

Figure 6.8.3: 60GHz CMOS single-chip transmitter die micrograph, and schematics of the three-stage power amplifier and the push-push VCO.

Transmitter Blocks	PA	VCO/PLL	IQ modulator-buffer /QVCO/PLL
Frequency	57 to 65GHz	49 to 55GHz	7 to 13GHz
Gain	17dB	-	-
Psat	8.4dBm	-	-
P_{1dB}	5.1dBm (out)	-	3dBm
S_{11}/ S_{22}	<−12 dB	-	<−25dB
S_{12}	<−40dB	-	-
Phase noise @1MHz Offset	-	−95dBc/Hz	−95dBc/Hz
DC Power consumption	54mW	30+30mW	17+22+20mW
Total DC Power consumption	173mW		

Figure 6.8.4: Measured performance summary of the 60GHz single-chip transmitter.

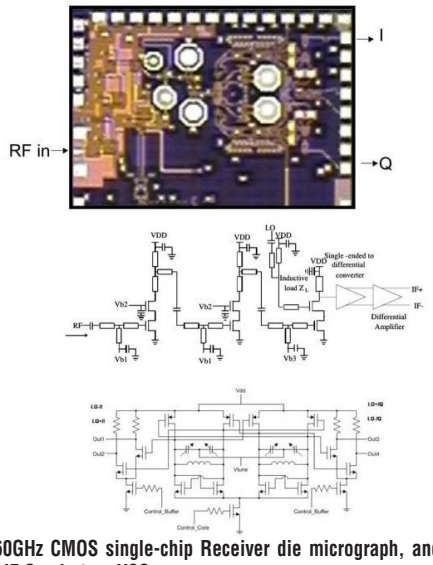

Figure 6.8.5: 60GHz CMOS single-chip Receiver die micrograph, and schematics of LNA-mixer and IF Quadrature VCO.

Receiver Blocks	LNA/Mixer /IF amplifier	VCO/PLL	IQ Demodulator-buffer /QVCO/PLL
Frequency	57-66 GHz	49-55 GHz	7-13GHz
Gain	32dB	-	19dB
NF	8dB	-	-
P1dB	-30 dBm (in)	-	-
S11/ S22	< -15 dB	-	-
S12	< -40dB	-	-
Phase noise @1MHz Offset	-	-95dBc/Hz	-95dBc/Hz
DC Power consumption	70mW	30+30 mW	19+20+20 mW
Total DC Power consumption	189 mW		

Figure 6.8.6: Measured performance summary of the 60GHz single-chip receiver.

Continued on Page 601

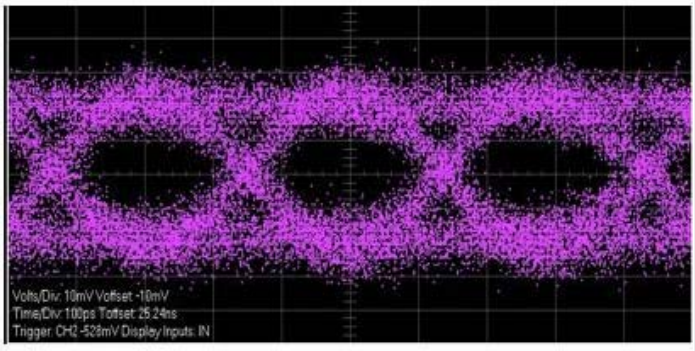

Figure 6.8.7: Measured eye diagram (I channel only) of a demodulated 7Gb/s QPSK signal.

 978-1-4244-2011-7/08/$25.00