7.8 Design Issues and Considerations for Low-Cost 3D TSV IC Technology

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3D TSV (through silicon via) technologies promise increased system integration at lower cost and reduced footprint [1]. Different variants of 3D technologies have recently been introduced in application areas such as DRAM stacking [2], imagers [3][4], SSDs (Solid-StateDrives) [5]. In this paper we investigate the design issues and solutions of a low cost 3D TSV Stacked-IC technology. This technology offers a 10 µm TSV pitch that enables applications such as logic-on-logic, DRAM-on-logic and RF-on-logic. We present experimental data on key issues such as impact of TSV on MOS devices and back-end-of-line (BEOL), reliability, thermal hot spots, ESD, signal integrity and circuit performance. Furthermore, we point out where changes in current design practices are required to realize the low-cost potential of the technology.

The proposed 3D stacked IC (3D-SIC) approach leverages existing IC foundry infrastructure to fabricate TSVs after the FEOL processing and prior to BEOL processing [6]. In a 200 mm/130 nm FEOL CMOS technology with Cu/SiO2 BEOL, TSVs are fabricated with 5 µm diameter and a minimum pitch of 10 µm, Fig. 7.8.1. After the TSV is etched, an isolation layer is deposited followed by the Cu metallization of the TSV. The wafers then go through the standard BEOL process. To enable interconnections using TSVs, the wafer is thinned down to ~25 µm and next TSVs are exposed to a height of ~700 nm. The thinned wafers are then diced and the dice are stacked face-up on the regular thickness landing wafer with a collective hybrid bonding process in a die-to-wafer approach [7]. This approach reduces the cycle time by the parallel processing of the relatively long Cu-Cu thermo-compression step and the die-to-wafer configuration allows the selection of Known Good Die prior to stacking, both reducing overall cost of the 3D processing.

4-point resistance measurement of single TSVs with 10 µm pitch, show an R_{TSV} ~20 mΩ in the corners and in the center of each die; the spread over 17 dies is limited (Fig. 7.8.2a). C-V measurements of TSV capacitance @ 1 MHz (Fig. 7.8.2b), show a C_{TSV} ~ 37 fF in depletion and a C_{TSV} ~ 92 fF in accumulation mode. Arrays of 6x6 TSV, each TSV measured individually for connectivity, show good yield over 17 dies for 20 µm pitch, Fig. 7.8.2c. Single TSV leakage, measured in the same array, is below 1 pA in depletion and accumulation modes (Fig. 7.8.2d).

The impact of TSV proximity on the active device electrical performance has been investigated for a wide range of physical gate lengths. It is observed that the transistors figures of merits like the threshold voltage and the drive current are affected by the presence of a TSV. The threshold voltage shows up to 10 mV shift for the 1 µm gate length devices of n-type (Fig. 7.8.3). Similar threshold shift has been measured for p-type devices with longer channel lengths. To avoid large keep out areas (areas in which no devices are placed) and increase cost of the use of 3D TSV technology, models and tools to design for TSV impact on devices are recommended [8].

Due to the difference in thermal expansion coefficient of Cu and Si, the TSV induces stress on its surroundings, potentially leading to reliability problems [9]. To detect reliability problems, back-end-of-line structures such as vias and serpentine wires have been added next to and on top of TSVs. The test structures have been subjected to thermal cycling. After 1000 cycles of 30 min between -55° and 125°C no failures have been observed on 17 samples.

Unless the power dissipation is carefully managed across the tiers in a 3D stack, hot spots may occur due to the reduced thermal spreading in the thinned die and the poorly conductive adhesives. To study the thermal impact of hot spot size and power density on 3D stack design, thermal finite element simulations were performed, calibrated with a test structure that consists of heaters integrated with thermal sensors (diodes). The heaters are located in the metal 2 layer of the BEOL in the top tier of the 3D chip-stack, as well as in a 2D reference die. Figure 7.8.4 shows a match between measured peak temperatures and model of 10%. The simulation results (Fig. 7.8.4) indicate that power dissipation in 3D approximately has a ~3 times higher maximum temperature increase than 2D, requiring thermal-aware floor-planning to avoid thermal problems in the stack.

The potential need to protect each TSV for ESD may increase the footprint of 3D connections and hence increase cost of using 3D technology. Experimental results in the presented technology indicate that no ESD protection is needed and that sufficient safe-guarding during 3D process steps is all that is required. ESD monitors have been included in a test chip where both unprotected and protected MOS gates are connected via TSV's in various connection schemes (Fig. 7.8.5). Gate-leakage is observed to monitor ESD events, no increase is found (Fig. 7.8.5).

Experimental results indicate that substrate noise isolation between stacked tiers is 20 dB superior compared to 2D, creating significant opportunities for mixed-signal and RF applications. A 60 GHz voltage controlled oscillator (VCO) circuit has been implemented both in 2D and on the top tier in a 3D stack (Fig. 7.8.6). VCO performance (center frequency, phase noise) is unaffected by the stacking operation. Both on the 2D chip and the bottom tier of the 3D stack a controlled "substrate noise" signal (a sine wave) is injected to measure noise coupling. This substrate noise signal emulates the switching activity of a digital circuit. The substrate noise signal couples to the output of the VCO as a spur. The 3D version exhibits a 20 dB lower level of spur power than the 2D SoC variant (Fig. 7.8.6).

To verify the feasibility of 3D circuits and the impact of TSV on digital signaling and circuit operation, 2D and 3D ring oscillator (RO) circuits with varying number of stages and inverter sizes are compared. 21 and 41-stage 3D ring oscillators with 1 TSV/stage and without TSVs are implemented, Fig. 7.8.7. Measured power-delay characteristics of the functional RO implementation are in agreement with the simulations, by using calibrated device models for the transistors and with lumped RC "T" model for the TSV calibrated with measured R_{TSV} and C_{TSV} values, Fig. 7.8.7. This validates that the model and extracted values are sufficient to build a digital design library and drivers circuits capable of driving high-speed signals through TSVs.

In this paper we presented key findings based on experimental data for design issues such as TSV impact on devices and BEOL, reliability, thermal hot spots, ESD and signal integrity in a 3D Cu-TSV Stacked-IC technology with Cu-Cu die-to-wafer bonding. We identified thermal and TSV proximity impact on MOS devices as key challenges requiring changes in design practices, while improved noise isolation in 3D design offers opportunities for mixed-signal systems. Additional challenges are design for test (DfT) and packaging of the 3D chip-stacks, as well as further reliability testing to prove viability of this technology.

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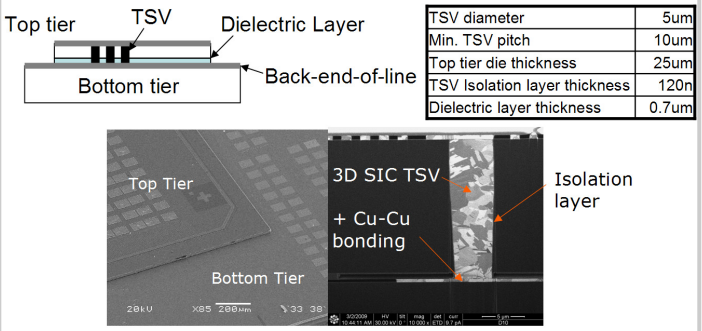


TSV diameter	5um
Min. TSV pitch	10um
Top tier die thickness	25um
TSV Isolation layer thickness	120n
Dielectric layer thickness	0.7um

Figure 7.8.1: 3D Stacked-IC technology with 10 μm TSV pitch and key technology parameters.

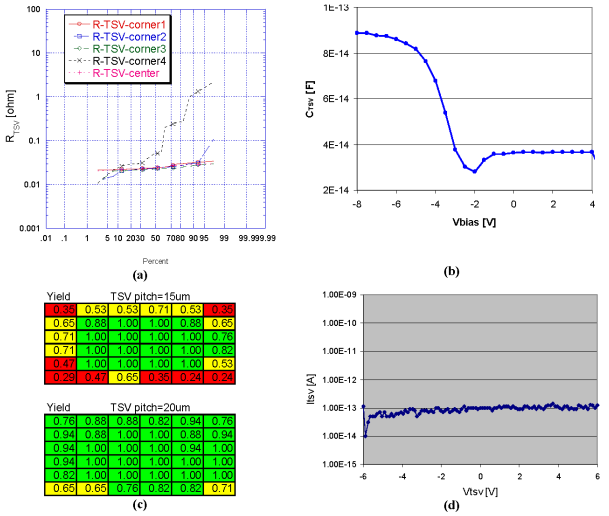


Figure 7.8.2: Resistance of single TSV (10 μm pitch) 20 mOhm (a), C-V of TSV capacitance: 37 fF@2 V (b), TSV yield 6x6 array for 15 μm and 20 μm pitch (c), leakage current of a single TSV is well below 1 pA (d).

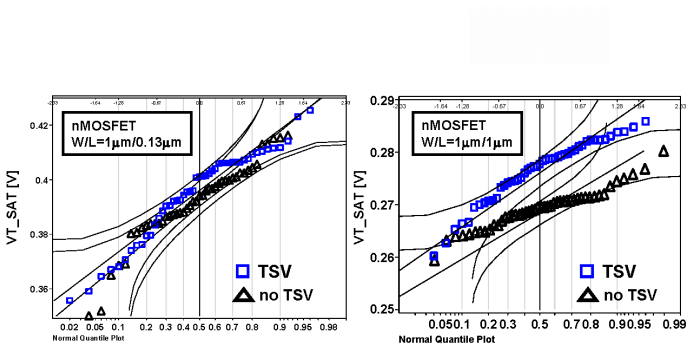


Figure 7.8.3: Cumulative probability plot of the saturation voltage for a short and long n-type device with and without a TSV (TSV edge at a distance of 2.5 μm from device), the long length device V_T changes by up to 10 mV.

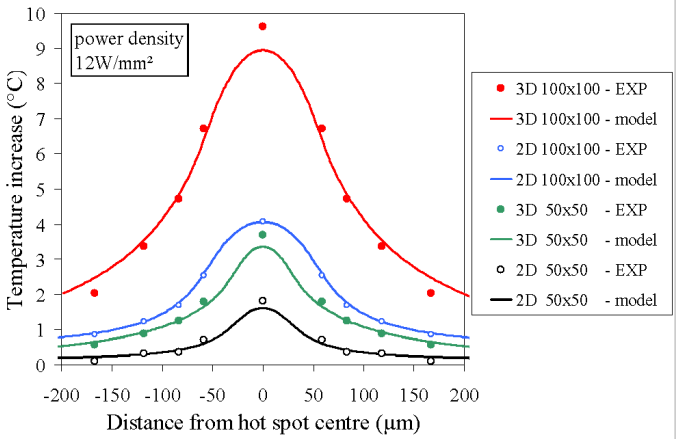


Figure 7.8.4: Modeling and experimental results of the temperature profile in the bulk of the Si below heaters for hot spot sizes of 50x50 μm and 100x100 μm for the thin top die of a 3D stack (3D) and a single full thickness die (2D).

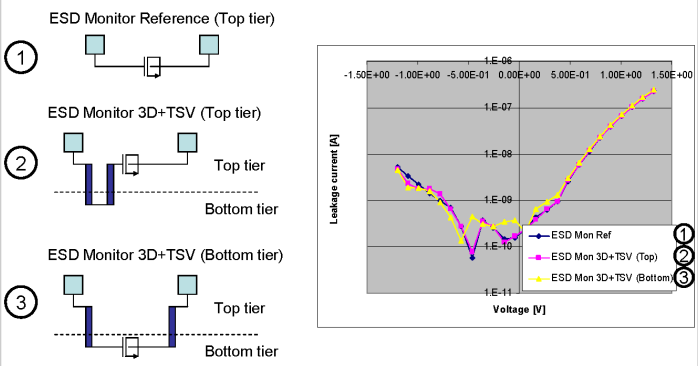


Figure 7.8.5: The leakage currents of ESD monitors (Ref, Top and Bottom) after stacking: monitors connected through TSVs see no failures (gate shorts) and no significant change versus reference structure (without TSV).

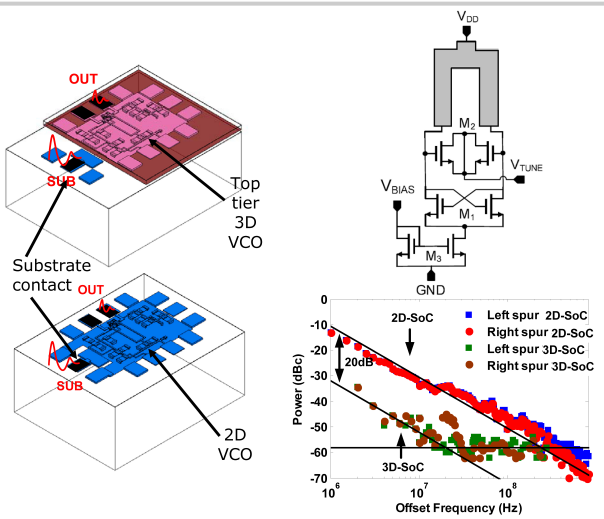
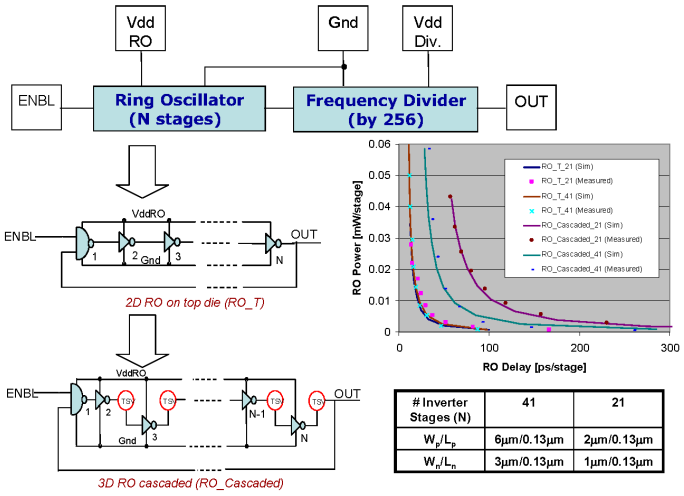


Figure 7.8.6: 2D and 3D mmWave VCO implementation and schematic, 20 dB reduction of noise coupling in 3D versus 2D is observed.



# Inverter Stages (N)	41	21
W_p/L_p	6µm/0.13µm	2µm/0.13µm
W_n/L_n	3µm/0.13µm	1µm/0.13µm

Figure 7.8.7: Ring oscillator schematic and sizing and comparison 2D versus 3D measurements and simulations.

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