Leakage Mechanism and Optimized Conditions of Co Salicide Process for Deep-Submicron CMOS Devices

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Abstract

For high performance deep-submicron CMOS devices, the TiN capped Co salicide process is one of the most attractive candidate to reduce the sheet resistances of the narrow gate, source, and drain regions. However, the increased leakage current for a very shallow p-n junction is a serious problem. We clarified a new leakage mechanism of the Co salicided junction. Measurements and simulated results of the leakage current revealed that the leakage current flows from many localized points. These leakage points were caused by CoSi spikes growing from the silicide film, which we observed by TEM analysis. We then optimized the Co salicide process conditions to reduce the leakage current in the ultra-shallow junctions of deep-submicron CMOS devices.

Introduction

In deep-submicron CMOS devices with gate lengths down to 0.1 μm, reduction of gate, source and drain parasitic resistance without a junction leakage problem is a key issue [1,2]. The conventional Ti salicide process dose not lead to significant junction leakage (Fig. 1-a), but it is difficult to achieve a low gate resistance in narrow regions (Fig. 2)[1,2]. This is because it is difficult to transform the crystal phase from high resistivity C49 to low resistivity C54 [2]. The TiN capped Co salicide process can successfully reduce the gate resistance even for a gate length of 0.075 μm (Fig. 2) [1,2,3]. However, the Co salicide process has a junction leakage problem (Fig. 1-b), which becomes increasingly serious in the ultra-shallow junctions necessary for deep-submicron devices. Although many studies have been made on the leakage current of Co salicide, little is known about leakage mechanism [2,4,5].

In this paper, we clarified the origin of the leakage current for the first time by statistical analysis of the leakage current and direct TEM observation, resulting in the development of a high performance Co salicide process for deep-submicron CMOS devices.

Experiment

In this study, n+/p shallow junction diodes were fabricated by using a conventional LOCOS process, and implanting with boron ions under the same conditions as n-MOSFET channel fabrication. Then a 0.1 μm deep ultra-shallow n+/p junction was formed by As implantation at 40 keV and subsequent 1000°C, 10 sec Rapid Thermal Annealing (RTA). After HF treatment, we sputtered 10-nm-thick Co and 30-nm-thick TiN. This Co forms 35 to 40-nm-thick $CoSi_2$ with a sheet resistance of about 5 ohm/sq. We tested various 1st RTA temperatures (400-550°C for 30 sec) to form Co_2Si and/or CoSi, and then the TiN and unreacted Co films were chemically removed. We then fixed the 1st RTA temperature at 550°C and performed a 2nd RTA at various temperatures (750-900°C for 30 sec) to analyze the leakage mechanism.

Electrical and simulated results

The cumulative probability of the leakage current was measured for diodes with various peripheral lengths and areas, as shown in Fig. 3 and 4. The leakage current after the 2nd RTA at 750°C, which was enough to reduce the sheet resistance of the Co silicide, was found to be independent of the junction periphery, but to be dominantly dependent on the junction area. The leakage current flow at not the junction periphery but the junction area. Furthermore, it is noteworthy that all junctions with large area (r=300 μm) show widely distributed leakage currents, on the other hand, scaling the junction size with the radius of 100 μm and 50 μm, 50% and 80% of junctions, respectively, still remain at the same low leakage level as that without Co salicide process. These results suggests that the leakage current induced by Co salicide do not flow uniformly in the junction area, but flow at some localized points which are randomly distributed in the junction area.

To verify this junction leakage model we simulated the leakage current with the Monte Carlo method. In addition to leakage currents without the Co salicide process, localized leakage currents are assumed to flow at random points in the junction area as schematically illustrated in Fig. 5. In this simulation one localized leakage current was assumed to have a Gaussian distribution (Fig. 6).

As shown in Fig. 4, our simulated results correspond

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well with the experimental data, which strongly supports our localized leakage model. This simulation also suggested the characteristic of localized leakage currents. Fitting all simulated data of different junction areas to experimental ones, fitting parameters of the simulation could be uniquely fixed., that is, the density, the average, and the standard deviation of localized leakage currents at RTA temperature of 750°C were 7000 points/cm^2, 1x10^{-12} A/point and 4 orders, respectively (Fig. 7). As we show later, it is interesting that except 900°C, the average and the standard deviation resulted always the same, despite different RTA temperatures, and only the density changed.

Origin of localized leakage

Next we describe the origin of localized leakage induced by the Co salicide. The temperature dependence of the junction leakage current indicates that the leakage current drastically increased at a temperature just around 450°C (Fig. 7), in which the Co_2Si changes phase to CoSi (Fig. 9). The density of localized leakage points in this sample was calculated to be 100000/cm^2 (Fig. 7). We discovered several spikes with this CoSi film by using cross-sectional TEM observation (Fig. 10-a). These spikes were assumed to be a kind of Co silicide because a Co signal was detected by EDX analysis (Fig. 10). The length of the CoSi spikes ranged 20 nm to 100 nm, which might be enough to break a shallow p-n junction. After 550°C annealing, which induces the $CoSi_2$ phase transition, the spikes became roundish and their density was much reduced (Fig. 7 anf Rig. 10-b). After the 2nd annealing at more than 750°C, the spikes were hardly observed (Fig. 10-c). The temperature dependence of the leakage current corresponds with the behavior of the CoSi spikes. Therefore, the origin of localized leakage current is the CoSi spikes. Though more than 900°C annealing increased the leakage current again, due to the Co diffusion into the Si substrate observed by SIMS analysis, the 2nd RTA at between 800°C and 850°C drastically reduced the leakage current (Fig. 8 and Fig. 12). This optimized condition resulted in a density of localized leakage point and an average current of each spot leakage estimated by the Monte Carlo simulation of 50-100/cm^2 and 1x10^{-12} A/point, respectively (Fig. 7), which never affects the device characteristics.

Conclusion

We clarified the leakage mechanism and the optimized conditions of the Co salicide process. The junction area dependence of leakage current together with the Monte Carlo simulation and the TEM observation indicates that a leakage current of about 1x10^{-12} A flows through many localized points, and the origin of these leakage points are the CoSi spikes. Using the above findings, we developed a high performance Co salicide process which can be applicable to deep-submicron CMOS devices.

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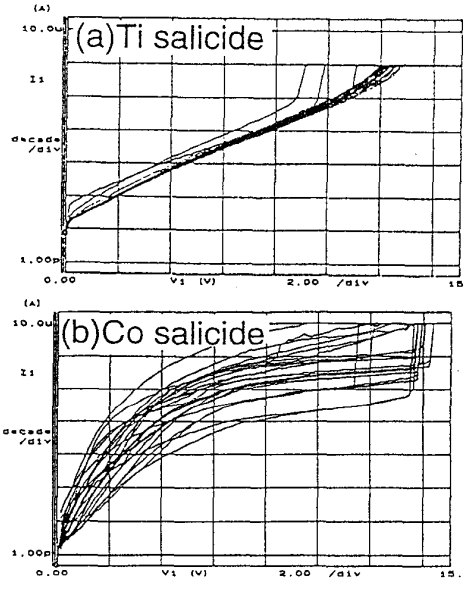


Fig.1. Typical leakage characteristic of (a)Ti salicide and (b) TiN capped Co salicide at 750°C 2nd RTA.

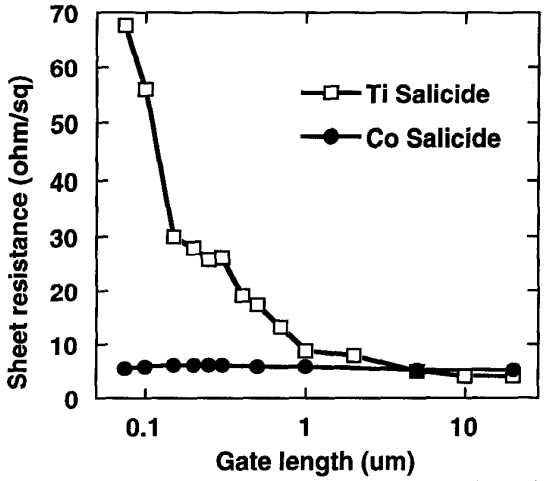


Fig.2. Gate sheet resistance of conventional Ti salicide and TiN capped Co salicide as a function of gate length.

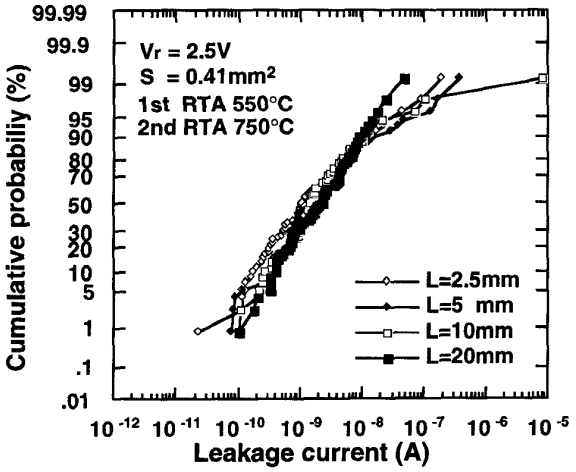


Fig.3. Cumulative probability of the leakage current at 2nd RTA 750°C for various peripheral lengths.

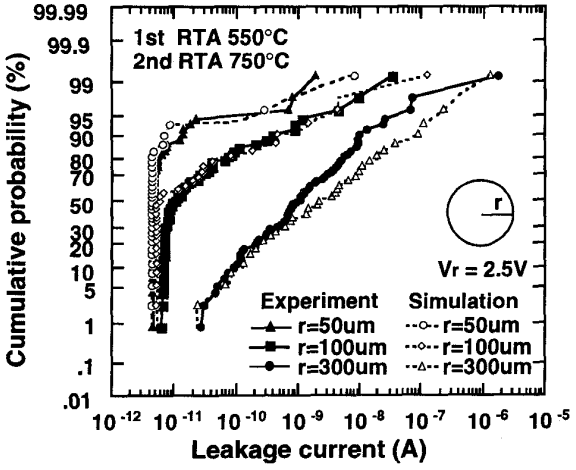


Fig.4. Cumulative probability of the experimental and simulated leakage current at 2nd RTA 750°C for various junction areas.

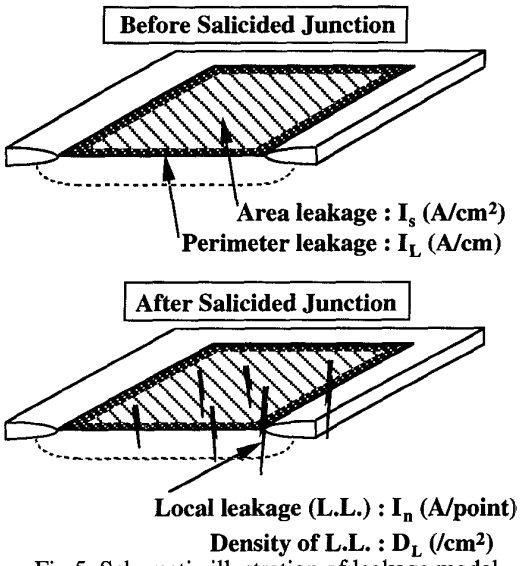
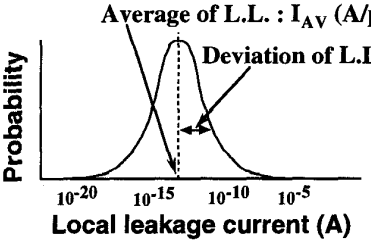


Fig.5. Schematic illustration of leakage model before and after salicide.



$$I = S \times I_S + L \times I_L + \sum_{n=1}^{D_L \times S} I_n(I_{AV}, \sigma^2)$$

Fig.6. Gaussian distribution of local leakage current and formula of total leakage current considering local leakage model.

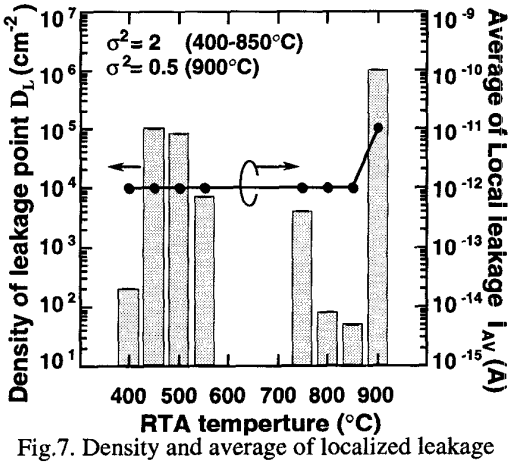


Fig.7. Density and average of localized leakage as a function of RTA temperature.

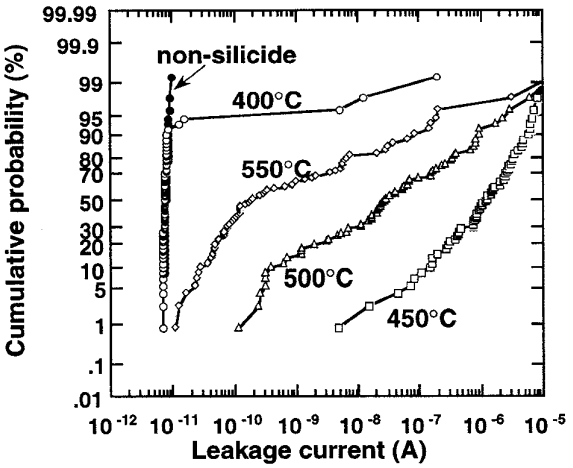


Fig.7 Cumulative probability of the leakage current with various 1st RTA temperature.

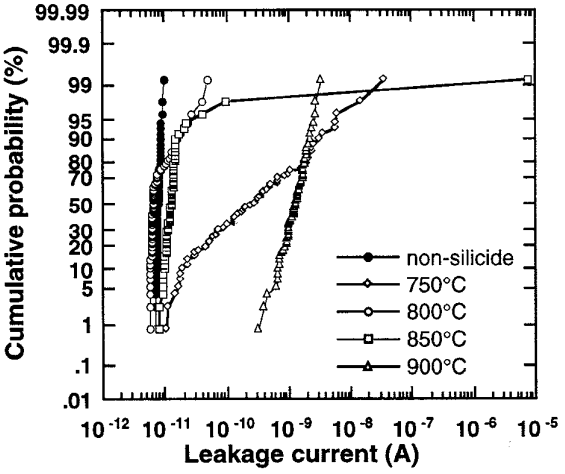


Fig.8. Cumulative probability of the leakage current for various 2nd RTA temperatures.

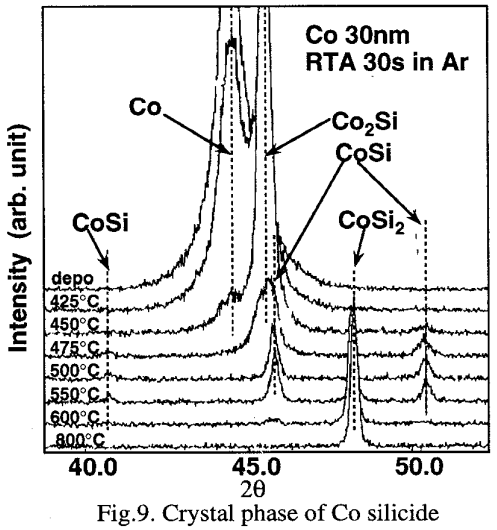


Fig.9. Crystal phase of Co silicide and RTA temperature.

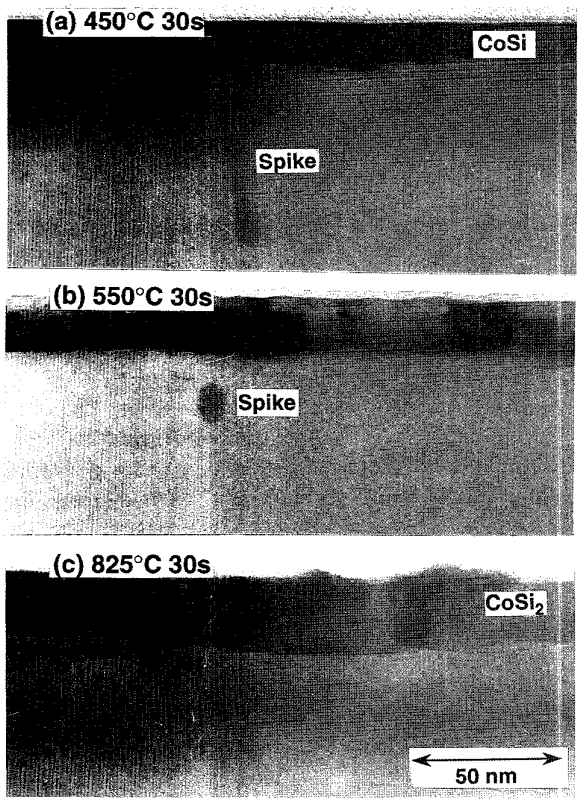


Fig.10 CoSi spike by TEM observation at (a) 450°C ,(b)550°C, and (c)825°C.

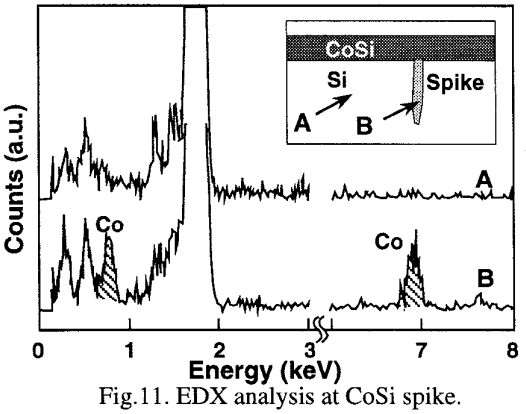


Fig.11. EDX analysis at CoSi spike.

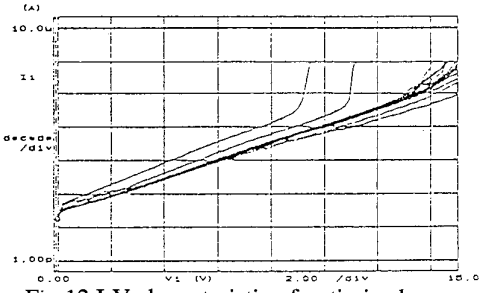


Fig.12 I-V characteristic of optimized Co salicide prosess with 2nd RTA at850°C .