Characterization and understanding of slow traps in GeO_x-based n-Ge MOS interfaces

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***Abstract*—** The properties of slow electron traps in n-Ge MOS interfaces over a wide range of electrical field across gate oxides (E_{ox}) are systematically investigated. It is found through careful examination of the C-V hysteresis that slow trapping under low E_{ox} conditions is attributed only to electron trapping into existing slow traps. Under large E_{ox} conditions, on the other hand, generation of slow electron traps and hole trapping are found to additionally affect the slow trapping characteristics. We propose a new measurement scheme to discriminate existing and generated slow electron traps and apply this method to the three different GeO_x-based MOS interfaces in order to clarify the nature of slow traps. It is revealed from this analysis that a pre-plasma oxidation process reduces existing slow electron traps and improves slow trapping in low E_{ox}. On the other hand, ultrathin Y_2O_3 insertion reduces generation of slow electron traps and improves slow trapping in high E_{ox}.

I. Introduction

One of the key technologies for realizing Ge CMOS is the formation of gate stacks with low defect densities. In order to reduce fast interface states, $(HfO_2)/Al_2O_3/GeO_x/Ge$ interfaces realized by post plasma oxidation (Post-PO) are promising [1, 2]. However, a remaining critical issue is the existence of a large amount of slow traps [3-5], which can be an inherent problem for Ge gate stacks. It has been reported that Y-doped GeO_x interfaces and $Al_2O_3/GeO_x/Ge$ formed by pre plasma oxidation (pre-PO) can reduce slow trap density (N_{st}) [6-8]. However, reduction in N_{st} is not sufficient yet, particularly for electrons. Thus, understanding of physical origins of the slow electron traps and the carrier trapping properties is strongly required to establish a guideline for further reduction in N_{st} and a method of the oxide reliability prediction for Ge MOS interfaces. Here, an evaluation method of slow traps is an important issue for the proper understanding. One of the simple ways of evaluating N_{st} is to use hysteresis of C-V curves. Thus, full utilization of this evaluation method is effective in obtaining information of carrier trapping behaviors. However, such an investigation has not been performed yet.

In this study, we examine the physical meaning of the present hysteresis measurement for slow electron traps in n-Ge MOS interfaces. Then, it is found that the applied electric field during this measurement strongly affects the electron trapping properties and that hole trapping also occurs in the electric field higher than a critical one. We propose a new method to discriminate existing and generated electron traps and hole traps. By utilizing this technique, we examine the difference in the slow electron trap properties among three promising GeO_x-based MOS interfaces Finally, we also touch on the slow carrier trapping behaviors by using Ge n-MOSFETs.

II. Device Fabrication

Fig. 1 shows the process flows of fabricated MOS structures The first and third structures have 1.5-nm-thick Al_2O_3 only and 0.7-nm-thick Y_2O_3, 1.5-nm-thick Al_2O_3 by ALD at 300°C, respectively, followed by ECR post-PO. The second sample has pre-PO GeO_x, followed by 1.5-nm-thick Al_2O_3 ALD at 300°C. PDA was performed for 30 min at 400 °C in N_2 ambient, followed by 100-nm-thick Au gate electrodes [7-8]. Fig. 2 shows the C-V curves of these capacitors. We also fabricated Ge n-MOSFETs with $Al_2O_3/GeO_x/Ge$ gate stacks by using the fabrication process described in ref. [9].

III. Slow trap properties under low V_g (E_{ox}) conditions

Recently, a simple and effective method to estimate N_{st} responsible for BTI reliability from MOS capacitors has been proposed [4, 5]. Fig. 3 schematically shows the procedure. Here, V_g is repeatedly scanned between the minimum voltage (V_{start}) and the maximum voltage (V_{stop}), with increasing V_{stop} (sequence I), as shown in Fig. 4. The amount of slow trap density responding to this scan (ΔN_{st}) can be estimated from the amount of hysteresis (ΔV_{hys}) in the C-V measurement with forward and backward scans as a function of the maximum effective electric field across gate insulators (E_{ox}). Here, E_{ox} and ΔN_{st} can be given by $E_{ox} = |V_{stop} - V_{FB}|/CET$ and $q \Delta N_{st} = C_{ox} \Delta V_{hys}$ on the assumption that all traps locate very close to the MOS interfaces. Fig. 5 shows the experimental results. Here, values of V_{FB} in the forward and back scan, extracted from Fig. 5, are plotted as a function of E_{ox} in Fig. 6. It is confirmed that V_{FB} in the backward scan keeps increasing, while V_{FB} in the forward scan almost no change under the present low E_{ox}, meaning that only electron trapping and no hole trapping occur. It is verified, as a result, that the amount of electrons trapped in slow states increases with an increase in E_{ox}, because the difference of V_{FB} in the forward and backward scan corresponds to ΔV_{hys} and resulting ΔN_{st}. Next, the repeated scan with same V_{start} and V_{stop} (sequence II), shown in Fig. 7, is performed to confirm the quantitativeness of the measured ΔN_{st}. Fig. 8 and 9 show the C-V curves under this sequence II and the extracted V_{FB} values as a function of scan cycle number. No change in the C-V and V_{FB} means that ΔN_{st} are stable under a given condition and no generation of slow traps occurs during the present V_g scan with low E_{ox}.

Next, the influence of the C-V scan time is examined. Here, the hold time at the V_{min} and V_{max} points during C-V measurements is varied under constant V_{min} and V_{max} values. Fig. 10 show the C-V curves with changing the V_{start} and V_{stop} hold times. The C-V curves have no change with changing the V_{start} hold time, meaning that the occupancy of slow traps at V_{FB} in the forward scan is under the equilibrium condition. On the contrary, when the V_{stop} hold time increases, ΔV_{hys} becomes larger. Fig. 11 and 12 show the hold time dependence of V_{FB} in the forward and backward scan, and the estimated ΔN_{st} as a function of the V_{stop} hold time, respectively. Since V_{FB} only in the backward scan increases, the total amount of trapped electrons increases with the time. There is no saturation in ΔN_{st}, which can be represented by $\Delta N_{st} \propto t^{0.21}$. These results indicate that the time constant of electron trapping into slow traps is widely distributed and that traps with very long time constants exist. These characteristics of electron trapping can be qualitatively understood by trap distributions spread widely along both the energy and the depth directions, as shown in Fig.13. Here, only slow traps with the energy levels below E_F at V_{stop} and with the position having the time constant shorter than the C-V scan time can be filled with electrons during the forward and backward scan. Also, no saturation in ΔN_{st} means that we cannot detect total amounts of slow traps and that only traps locating in an energy range and a depth range contribute to ΔV_{hys}. As a result, the measured ΔN_{st} amounts to a part of total N_{st} as the effective one. On the other hand, as far as the measurement condition is fixed, the relative comparison in ΔN_{st} can still be meaningful.

Under the understanding of the physical meaning of the present evaluation method, the slow trap properties in the three types of the fabricated Ge MOS capacitors are compared. Fig. 14(a) shows the measured ΔN_{st}-E_{ox} relationship in the three types of the n-Ge MOS capacitors. It is confirmed for n-Ge MOS interfaces that insertion of Y_2O_3 can slightly decrease ΔN_{st} and that the pre-PO process leads to much lower ΔN_{st} than the post-PO process. Also, the comparison between p-Ge and n-Ge is shown in Fig. 14 (b). ΔN_{st} in p-Ge with both post-PO and pre-PO is much lower than that in n-Ge, meaning that the gate stack instability due to slow trap is much more serious in n-Ge. This is the reason why we focus on the slow traps in n-Ge MOS capacitors. In order to carefully examine the difference in ΔN_{st} of n-Ge between the pre- and post-PO process, ΔN_{st} is evaluated by C-V curves with changing the step time at each V_g step, shown

in Fig. 15. It is confirmed that ΔN_{st} is higher in the post-PO capacitors, irrespective of the step time, indicating that the difference in ΔN_{st} between the pre- and post-PO process is attributed to the difference in the total slow trap density, not to the modulation of the time constant. Fig. 16 shows a schematic model to explain the increase in slow traps by the post-PO process. We can interpret that additional slow traps can be generated by the post-PO process, independent of the defects inherent to GeO_x, probably through any reaction and/or inter-diffusion between Al_2O_3 and GeO_x.

IV. Slow trap properties under high V_g (E_{ox}) conditions

As described, the hysteresis observed in the C-V scan with low V_{stop} (E_{ox}) is attributed to electron trapping into existing slow trap sites, which is the common interpretation of the hysteresis in Ge MOS interfaces. However, we have found that, when higher V_{stop} (E_{ox}) is applied, both hole trapping and generation of new electron slow traps happen. It should be noted here that the discrimination of existing and generated traps is important for identifying the physical origin of the slow traps. Fig. 17 shows the C-V curves under repeated scan (sequence I), where E_{ox} is increased up to values higher than a critical one ($E_{critical}$). It is observed that V_{FB} starts to shift toward negative V_g, which is totally different from the C-V curves under small E_{ox}. As seen in Fig. 18, when E_{ox} becomes sufficiently large (typically larger than 10 MV/cm), V_{FB} in the forward scan starts to decrease rapidly, while V_{FB} in the back scan increases gradually. Next, the repeated scan with constant V_{stop} and V_{start} (sequence II) is applied to capacitors under E_{ox} higher than $E_{critical}$ in Fig. 19. Fig. 20 summarizes the voltage shift of the C-V scan under low and high E_{ox} as a function of the scan cycle number. The negative shift of the forward scan increases with an increase in the cycle number, suggesting the increase in the amount of trapped holes, which has been reported in Ge p-MOSFETs after NBTI stress [10, 11].

The gate current (J_g) before and after the J_g measurement is shown in Fig. 21. J_g for the post-PO capacitors is higher than the pre-PO ones, suggesting the higher density of defects in the post-PO capacitors. Fig.22 shows J_g before and after the C-V scan. Although a small amount of stress-induced leakage current is observed, the significant degradation is not observed after applying E_{ox} higher than $E_{critical}$. In order to examine the de-trapping of holes, C-V curves after the C-V scan up to high E_{ox} are measured with changing the negative V_{start} values (Fig. 23). No change in the C-V curves means that trapped holes works as fixed charges and do not contribute to ΔV_{hys}. The present results can be explained by a model of Fig. 24. Under low E_{ox}, only electrons in Ge are trapped into slow traps during C-V measurements. Under high E_{ox}, on the other hand, hot holes created probably in the gate metal are injected into dielectrics and trapped into hole traps. These trapped holes do not come out and cause the negative V_{FB} shift as fixed positive charges. In order to determine $E_{critical}$ for hole trapping, the C-V scan using the sequence II with high E_{ox} is applied to the three types of capacitors. Fig. 25 shows the hole trap density after 1 and 2 cycles as a parameter of E_{ox}. The linear relationship between the hole trap density and the cycle number is clearly observed. Fig. 26 shows this slope as a function of E_{ox}. As a result, $E_{critical}$ is estimated to be 11.5 and 14.8 MV/cm for w/ and w/o Y_2O_3 n-Ge MOS interfaces, respectively. It is found that inserting the Y_2O_3 interfacial layer makes the interface more robust against hole trapping.

In addition to hole trapping, we have found that generation of slow electron traps occurs at E_{ox} higher than $E_{critical}$. In order to discriminate generated and existing electron slow traps, we propose a new measurement using sequence III, shown in Fig. 27. Here, after applying high V_{stop} once, ΔV_{hys} under the initial C-V scan condition with sufficiently low V_{stop} is re-measured. Since ΔV_{hys} does not change for the repeated measurements with low V_{stop} (Fig. 8), the increment ΔV_{hys} corresponds to ΔN_{st} for generated slow traps. Fig. 28 shows the change in V_{FB} by using sequence III. We can discriminate and determine $\Delta N_{st\text{-}total}$, $\Delta N_{st\text{-}generated}$, $\Delta N_{st\text{-}existing}$ (total, generated, existing electron slow traps density), and ΔN_h (hole traps density) under the proposed measurement as follows;

$$\Delta N_{st-total} = \Delta V_{hys2} \times C_{ox}/q, \quad \Delta N_{st-generated} = (\Delta V_{hys1} - \Delta V_{hys0}) \times C_{ox}/q,$$
$$\Delta N_h = \Delta V_{forward} \times C_{ox}/q, \quad \Delta N_{st-existing} = \Delta N_{st-total} - \Delta N_{st-generated}$$

Fig. 29 shows the V_{FB} values measured by sequence III. After the V_g scan up to high V_{stop}, V_{FB} in the forward scan decreases and V_{FB} in the backward scan slightly increases, resulting in the increase of ΔV_{hys} in comparison with the initial scan. This result means that trapped holes appear and electron slow traps are generated by applying higher V_{stop} (E_{ox}). By using this new measurement method, we compare the contributions of generated and existing electron slow traps and hole traps to total ΔN_{st} among the three types of n-Ge MOS capacitors. Fig. 30 shows $\Delta N_{st\text{-}total}$, $\Delta N_{st\text{-}existing}$, $\Delta N_{st\text{-}generated}$ and ΔN_h in the Al_2O_3/GeO_x/Ge MOS interfaces with post-PO. It is found that $\Delta N_{st\text{-}existing}$ dominates $\Delta N_{st\text{-}total}$ in lower E_{ox}, while $\Delta N_{st\text{-}generated}$ is comparable to or higher than $\Delta N_{st\text{-}existing}$ in higher E_{ox}. Also, ΔN_h is comparable to $\Delta N_{st\text{-}existing}$ and $\Delta N_{st\text{-}generated}$ in high E_{ox}. These results indicate that the influence of slow trap generation and hole trapping must be taken into account in high E_{ox} as the physical origin of slow electron trapping in Ge MOS reliability. Fig. 31 shows the comparison of $\Delta N_{st\text{-}total}$, $\Delta N_{st\text{-}existing}$, $\Delta N_{st\text{-}generated}$ and ΔN_h among the post- and pre-PO Al_2O_3/GeO_x/n-Ge, and post-PO $Al_2O_3/Y_2O_3/GeO_x$/n-Ge gate stacks. It is found that $\Delta N_{st\text{-}existing}$ in high E_{ox} is almost the same, while pre-PO exhibits the lowest value in low E_{ox}, as shown in Fig. 4(a). Also, $\Delta N_{st\text{-}generated}$ is almost the same between pre- and post-PO Al_2O_3/GeO_x/Ge. These facts suggest that the slow electron trapping and generation in high E_{ox} are determined by a common nature of pure GeO_x. It is found, on the other hand, that $Al_2O_3/Y_2O_3/GeO_x$/Ge shows much lower ΔN_h and $\Delta N_{st\text{-}generated}$, meaning that insertion of Y_2O_3 and doping of Y into GeO_x can be an effective way to improve the gate stack reliability in high E_{ox}. This result is consistent with the report on stabilization of GeO_2 network by Y incorporation [12]. As a result, we can interpret that lower $\Delta N_{st\text{-}total}$ of pre-PO in low E_{ox} and $Al_2O_3/Y_2O_3/GeO_x$/Ge in high E_{ox} are attributed to the suppression of existing trap generation due to pre-PO and the increased robustness against electron slow trap generation and the hole traps, respectively. The present analyses also suggest that existing and generated electron slow trap and hole traps have the different physical origins.

V. Characteristics of slow traps in Ge n-MOSFETs

As described above, the slow traps measured by C-V hysteresis can be a part of existing slow traps. In order to estimate all of slow traps affecting device performance, the evaluation of time dependence of MOSFET currents is effective. Thus, the characteristics of channel currents of Ge n-MOSFETs with Al_2O_3/GeO_x/Ge gate stacks are studied. Fig. 32 and 33 show I_s as a function of V_g and the time dependence, respectively. The decrease in I_s corresponds to the trapped electrons. The long-term I_s-t characteristics in Fig. 34 indicate that show trapping has no saturation and is described by the log t dependence. We have also found that the trapping characteristics have the temperature dependence, as seen in Fig. 35. The activation energy of the slope in log t plot is estimated to be ~ 20 meV (Fig. 36). Thus, any temperature-dependent process could be incorporated into the slow trapping mechanism of channel electrons, as Fig. 37.

VI. Conclusion

The properties of slow traps in Ge MOS interfaces in small and large E_{ox} were systematically examined. It was found that only existing slow traps are responsible in low E_{ox}, while generation of slow traps and hole trapping additionally occur in high E_{ox}. Also, we proposed a new measurement scheme to discriminate existing and generated electron slow traps. The pre-PO and Y_2O_3 insertion have been found to reduce existing and generated slow electron traps, respectively, contributing to the reduction in total slow trap density.

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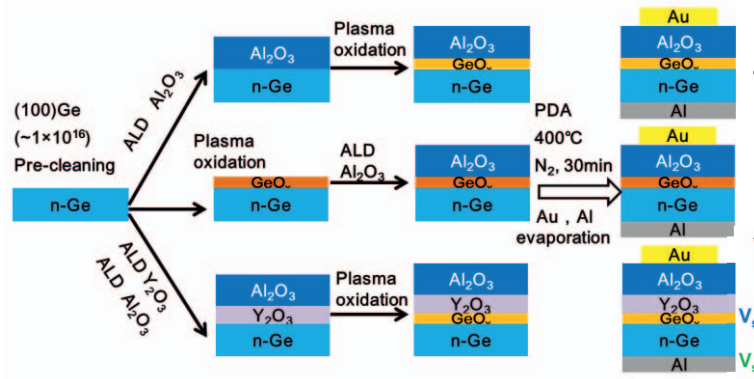

Fig. 1 Process flow and structures for and Al_2O_3/GeO_x/Ge with post-PO, Al_2O_3/GeO_x/Ge with pre-PO and $Al_2O_3/Y_2O_3/GeO_x$/Ge with post-PO MOS interfaces

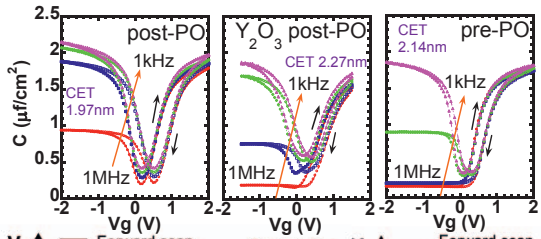

Fig. 2 C-V curves for the MOS interfaces in Fig. 1

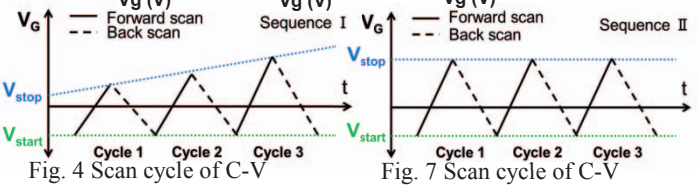

Fig. 4 Scan cycle of C-V measurements with same V_{start} and changing V_{stop} (Sequence I)

Fig. 7 Scan cycle of C-V measurements with same V_{stop} and V_{start} (Sequence II)

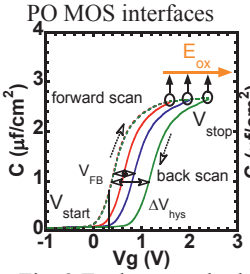

Fig. 3 Evaluate method for slow trap density by using C-V measurement

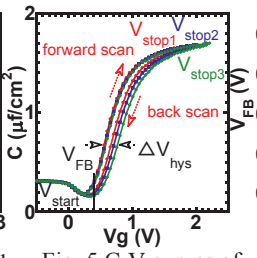

Fig. 5 C-V curves of Al_2O_3/GeO_x/Ge MOS interfaces with changing V_{stop}

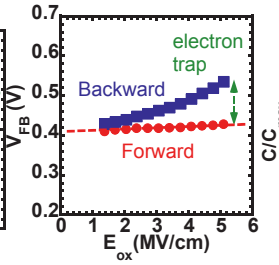

Fig. 6 V_{FB} values for forward and backward C-V scans

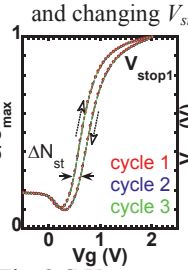

Fig. 8 C-V curves under cycle scans with same V_{stop} and V_{start}

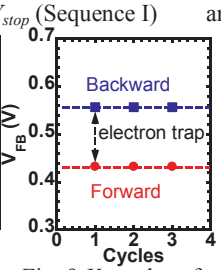

Fig. 9 V_{FB} values for forward and backward C-V scans with same V_{stop} and V_{start}

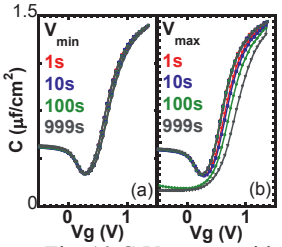

Fig. 10 C-V curves with different (a) V_{min} and (b) V_{max} hold time

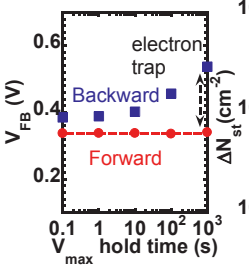

Fig. 11 V_{FB} values as a function of V_{max} hold time for forward and backward C-V scans with same V_{stop} and V_{start}

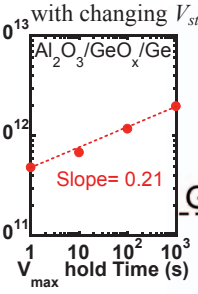

Fig. 12 Slow trap density as a function of V_{max} hold time with same V_{stop} and V_{start}

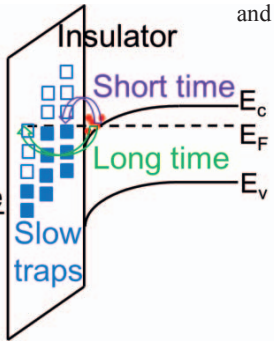

Fig. 13 Schematic diagram for slow trap response in Ge n-MOS interfaces

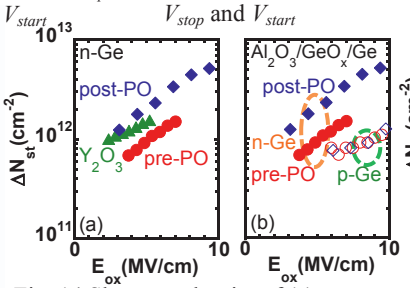

Fig. 14 Slow trap density of (a) Al_2O_3/GeO_x/n-Ge with post-PO and pre-PO, and $Al_2O_3/Y_2O_3/GeO_x$/n-Ge MOS interfaces with post-PO (b) Al_2O_3/GeO_x/n-Ge and /p-Ge with post-PO and pre-PO

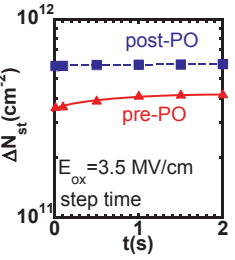

Fig. 15 Slow trap density as a function of step time in Al_2O_3/GeO_x/n-Ge MOS interfaces with post-PO and pre-PO

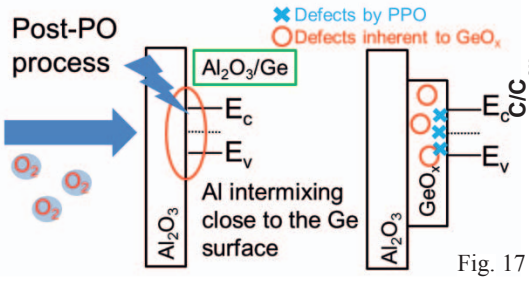

Fig. 16 Schematic diagram for slow trap generation by the post-PO process in Al_2O_3/GeO_x/n-Ge MOS interfaces

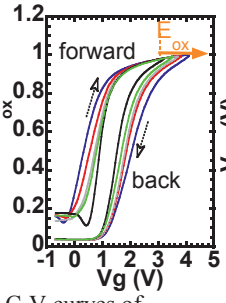

Fig. 17 C-V curves of Al_2O_3/GeO_x/n-Ge with pre-PO capacitor under high E_{ox}

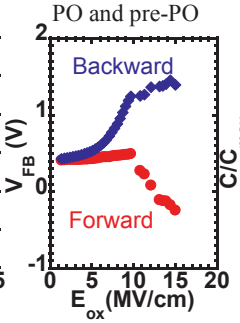

Fig. 18 V_{FB} in forward scan and backward scan in C-V measurements up to high E_{ox}

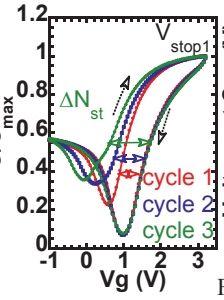

Fig. 19 C-V curves under cycle scans with same V_{stop} and V_{start}

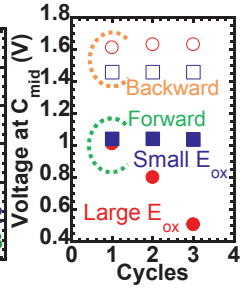

Fig. 20 Voltage at C_{mid} for forward and backward C-V scans under low and high E_{ox} conditions

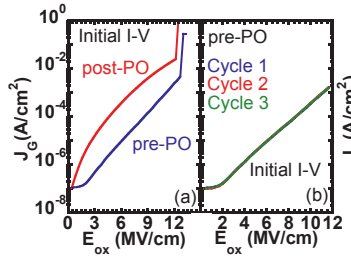

Fig. 21 Relation of J_G and E_{ox} in (a) Al_2O_3/GeO_x/n-Ge MOS capacitors with post-PO and pre-PO and (b) cyclic measurements of J_G

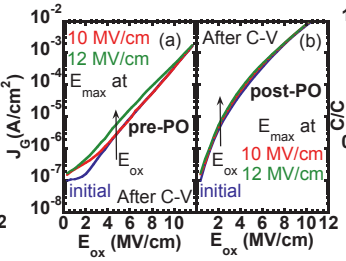

Fig. 22 Relation of J_G and E_{ox} in Al_2O_3/GeO_x/n-Ge MOS capacitors with (a) pre-PO and (b) post-PO after C-V scan with different E_{ox}

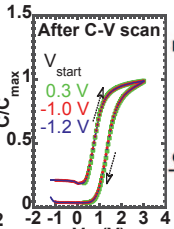

Fig. 23 C-V curves with different V_{start} after C-V scan at E_{ox} max value is 13.8MV/cm

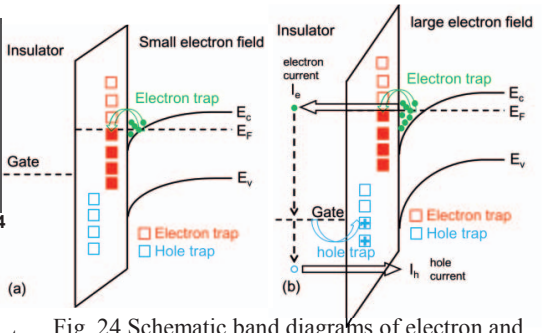

Fig. 24 Schematic band diagrams of electron and hole trapping behaviors under (a) low E_{ox} and (b) high E_{ox} in n-MOS gate stacks

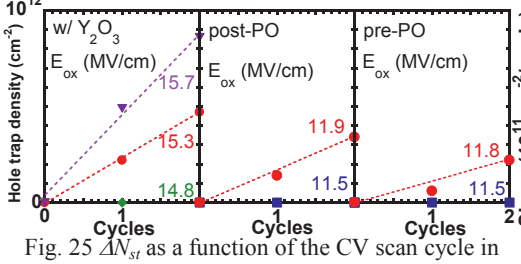

Fig. 25 ΔN_{st} as a function of the CV scan cycle in Al_2O_3/GeO_x/Ge, $Al_2O_3/Y_2O_3/GeO_x$/Ge gate stacks with post-PO and Al_2O_3/GeO_x/Ge gate stack with pre-PO. A parameter is E_{ox}.

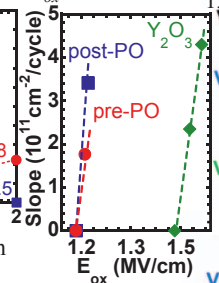

Fig. 26 Slope of ΔN_{st}-CV cycle as a function of E_{ox} for the three gate stacks.

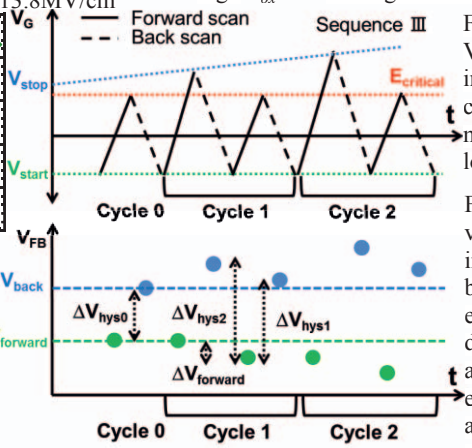

Fig. 27 Scan cycle of C-V measurement with increasing V_g and constant V_{gc} for monitoring hysteresis at low E_{ox} (Sequence III)

Fig. 28 Schematic view of V_{FB} change in forward and backward scan for evaluating the density of existing and generated slow electron trap density and hole trap density as a function of E

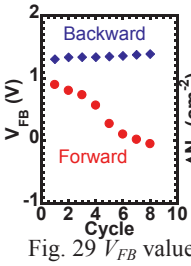

Fig. 29 V_{FB} values in forward and backward C-V scans of Al_2O_3/GeO_x/Ge MOS interfaces by cycle measurement at $E_{critical}$ of 11.5MV/cm and max E_{ox} values from 12 to 15MV/cm

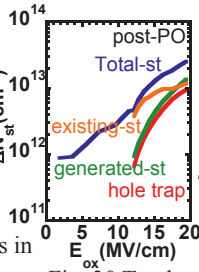

Fig. 30 Total, generated and existing electron slow trap density, and hole trap density of Al_2O_3/GeO_x/Ge MOS interface with post-PO

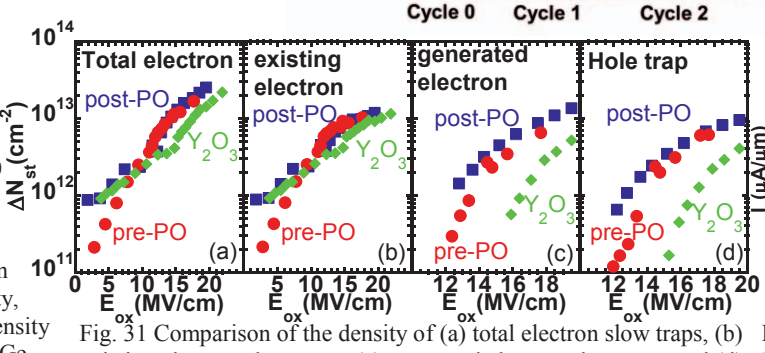

Fig. 31 Comparison of the density of (a) total electron slow traps, (b) existing electron slow traps, (c) generated electron slow traps and (d) hole traps in Al_2O_3/GeO_x/Ge, $Al_2O_3/Y_2O_3/GeO_x$/Ge gate stacks with post-PO and Al_2O_3/GeO_x/Ge gate stacks with pre-PO

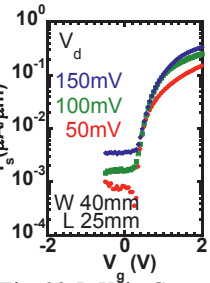

Fig. 32 I_s-V_g in Ge n-MOSFETs with the Al_2O_3/GeO_x/Ge gate stack using different V_d

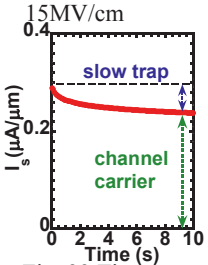

Fig. 33 Time dependence of I_s in Ge n-MOSFETs with the Al_2O_3/GeO_x/Ge gate stack

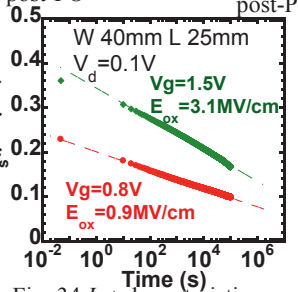

Fig. 34 I_s-t characteristics in Ge n-MOSFETs with the Al_2O_3/ GeO_x/Ge gate stack as a parameter of V_g

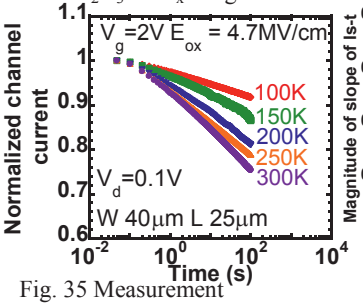

Fig. 35 Measurement temperature dependence of normalized I_s-log t characteristics in Ge n-MOSFETs

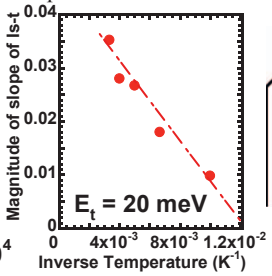

Fig. 36 Activation energy plot of the slope in the I_s-log t characteristics

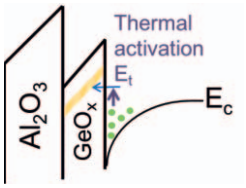

Fig. 37 Schematic diagram of possible thermal activation process in slow electron trapping in Ge MOS interfaces