4.2 A Broadband Switched-Transformer Digital Power Amplifier for Deep Back-Off Efficiency Enhancement

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Sophisticated OFDM modulation schemes with high spectrum efficiency and data throughput in modern wireless communication systems often result in a large peak-to-average power ratio (PAPR). Besides, wireless standards like LTE, WLAN, NB-IoT, etc., require wide transmission power range to accommodate various communication environments, and devices often function at low average output power. For better battery lifetime, it is critical to improve the power amplifier (PA) efficiency at deep power back-off (PBO) levels (e.g., 12/18dB or higher). Recently, several digital-style techniques have been employed to enhance PA PBO efficiency, such as dynamic power control [1], Class-G, and Doherty [2-4], as well as multi-level outphasing [5]. Class-G or Doherty techniques usually provide an efficiency peaking at 6dB PBO, and when combined together [2,3] or cascaded [6] they can further enhance the efficiency beyond 6dB PBO by introducing two efficiency peaks at 6/12dB PBOs. However, most of the Class-G Doherty PAs suffer from large area overhead with two power supply paths and glitches due to mode transitions. The dynamic power control or multi-level outphasing PA requires multiple phase modulators and amplitude-level transitions, which cause inherent discontinuities and degrade the linearity. In this work, a switched-transformer digital-PA technique is proposed for wide-range PBO efficiency enhancement. This topology does not require multiple power supplies and does not introduce AM/PM discontinuities. The PA achieves multiple efficiency peaks at 0/6/12/18dB PBOs and wide frequency coverage with a single-transformer footprint and only one supply voltage.

Figure 4.2.1 illustrates the operating principles of proposed switched-transformer PA. PA1/PA2/PA3/PA4 are four differential sub-PA pairs that are digitally controlled independently, and the transformer can be reconstructed to perform the function of power combining at different PBO levels. At 0dB PBO, all sub-PAs are fully switched on and the 5-coil transformer combiner performs an 8-way parallel power combining, where the four primary coils are driven by four differential sub-PA pairs to collect their output currents and provide the optimum single-ended load impedance Ropt. Besides, the transformer combiner is configured as shown in Fig. 4.2.1 to maintain all sub-PA pairs quasi-differential so as to reduce differential mismatches. With output power decreased, the unit cells of PA3 and PA4 are gradually switched off. At 6dB PBO, PA3/PA4 are fully turned off and the transformer combiner is reconfigured as a 4-way power combiner with SW3/SW4 switched on, where the single-ended impedance seen by PA1/PA2 reaches 2×Ropt and an efficiency peaking is achieved due to load modulation. With output power reduced continuously, PA2 is then switched off and the single-ended impedance seen by PA1 continues to increase until it reaches 4×Ropt, thus leading to another efficiency peaking at 12dB PBO. Furthermore, when PA1 goes from differential to single-ended, the single-ended impedance seen by PA1+ increases to 8×Ropt and an efficiency peaking appears at 18dB PBO. Therefore, deep back-off efficiency enhancement at 6/12/18dB PBOs are achieved with the proposed switched-transformer power-combing technique.

Figure 4.2.2 shows the detailed schematic of proposed switched-transformer digital PA, where the switched-capacitor PA topology is adopted for fine amplitude control due to its good linearity and efficiency [3]. In the design, the total resolution of 9b is employed and the 2 MSBs control four 7b sub-PAs. In each sub-PA, the hybrid unary-and-binary array is utilized to achieve a better resolution and reduce layout mismatch. Each sub-PA is divided into 4 groups controlled by AM1/2/3/4<6:5> and each group consists of 7 thermometer-coded cells and 2b LSB binary-coded cells. Here, PA2/PA3/PA4 are three identical sub-PAs while PA1 is slightly different from the others since it has the single-ended operation mode. A simple inverter-based Class-D topology is employed in the differential unit PA cell, which has two operation states in all the sub-PAs. During 0-to-12dB PBO, the unit cells of PA3/PA4 and PA2 are gradually transformed from the on-state to the high-impedance state in sequence, and the transformer combiner is reconstructed through the switches that are formed by three NMOS transistors between the differential outputs. Within 12-to-18dB PBO, the differential branches of PA1 are controlled independently. At 18dB PBO, the positive half of PA1 is fully at the on-state while the negative half is completely at the off-state with inverter outputs grounded, thus enhancing the deep back-off efficiency by reconstructing the transformer combiner and performing the load modulation.

Figure 4.2.3 presents the implementation of proposed switched-transformer-based matching network. The 8-way transformer combiner is realized within a compact single-transformer footprint. The 4 sub-PAs are located at the four corners of the transformer to achieve good differential matching and diagonal symmetry. The output currents from the 4 sub-PAs flow in parallel direction in the four primary coils, which achieves magnetic enhancement and increases the effective primary inductance, thus contributing to size reduction and lower loss. The passive matching network consists of sub-PA device parasitic capacitors, switched capacitors, a digitally reconstructive transformer, and 2 capacitors C_1, which transform the optimum load impedance for the 4 sub-PAs. It achieves broadband frequency coverage over 1.3 to 3.5GHz with less than 1dB output power variation. The total passive loss from the 4 sub-PAs to 50Ω load is less than 1.5dB in a wide frequency range. The balun function is also implemented on-chip with a single-ended output pad. In the design, a total of 300pF de-Q'ed decoupling capacitors are integrated to attenuate supply and ground fluctuations while further improving the linearity performance.

The proposed deep back-off efficiency-enhanced DPA has been fabricated in a 40nm CMOS process (Fig. 4.2.7), and occupies an area of 1.15×0.7mm^2 including all decoupling capacitors and I/O pads. The chip is powered by a single 1.1V supply, and the power consumption of all IO buffers, logic blocks, and PAs is included in the PAE calculation. Figure 4.2.4 shows the measured continuous-wave (CW) results, where the DPA achieves 21.4dBm output power with 31.3% peak PAE at 1.5GHz and 20.4dBm output power with 24.5% peak PAE at 3.5GHz. The 1dB bandwidth is over 90% spanning from 1.3 to 3.5GHz while maintaining good PAE performance. Thanks to the switched-transformer power-combining and load-modulation techniques, the expected back-off efficiency enhancement is realized, where the DPA achieves the PAE of 31.3%, 27.7%, 16.6%, and 7.7% for 0dB, 6dB, 12dB, and 18dB PBOs at 1.5GHz, respectively. Besides, our proposed DPA demonstrates the significant PAE improvements of 1.77×, 2.12×, and 1.97× at 6dB, 12dB, and 18dB PBOs, respectively, compared to the traditional Class-B PA.

In modulation tests, 1-D AM-AM and AM-PM memoryless look-up tables (LUTs) are used to linearize the DPA. For the 20MHz 64-QAM LTE signal with 6.2dB PAPR, the measured spectrum and constellation are shown in Fig. 4.2.5. With -32.5dB EVM, the DPA achieves the P_{avg} of 15.2dBm with average PAE of 25.3%, and the measured upper/lower ACLRs are -30.4dBc and -33.0dBc, respectively. Figure 4.2.6 summarizes the performance and makes a comparison with prior deep back-off efficiency-enhanced DPAs. By utilizing the switched-transformer power-combining technique, the proposed DPA achieves the effective deep back-off efficiency enhancement and broadband frequency coverage with the smallest die size, thus suitable for multiple communication standards especially with a wide dynamic power range.

Acknowledgements:
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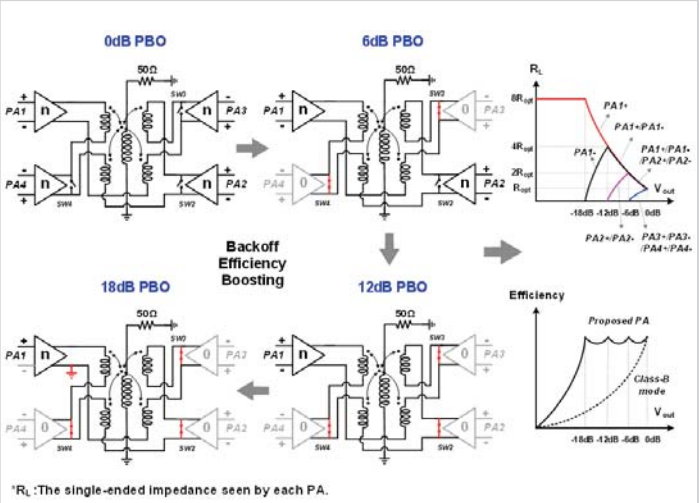

Figure 4.2.1: Operating principles of the proposed switched-transformer digital PA.

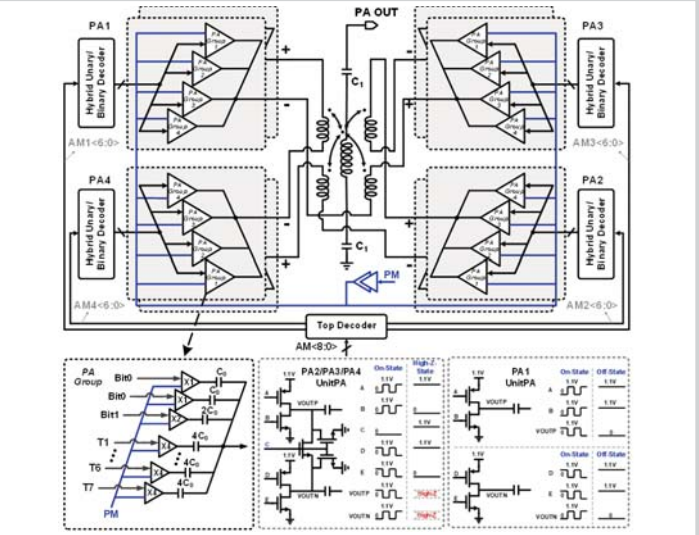

Figure 4.2.2: Detailed schematic of the proposed switched-transformer digital PA.

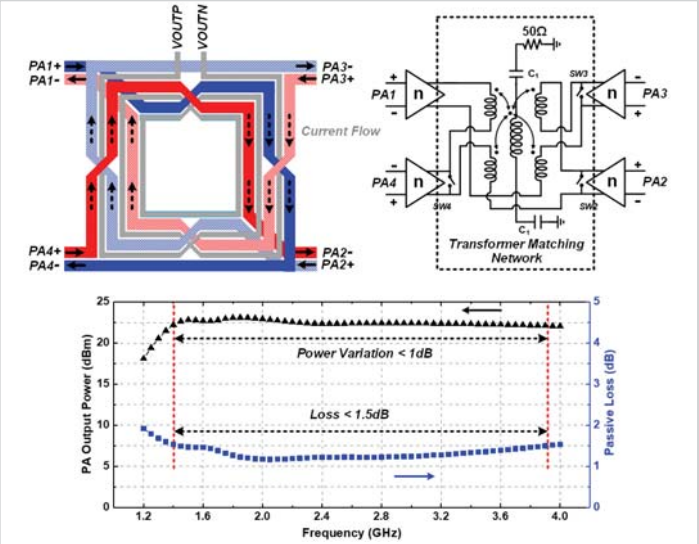

Figure 4.2.3: Implementation of the proposed switched-transformer-based matching network and its simulation results.

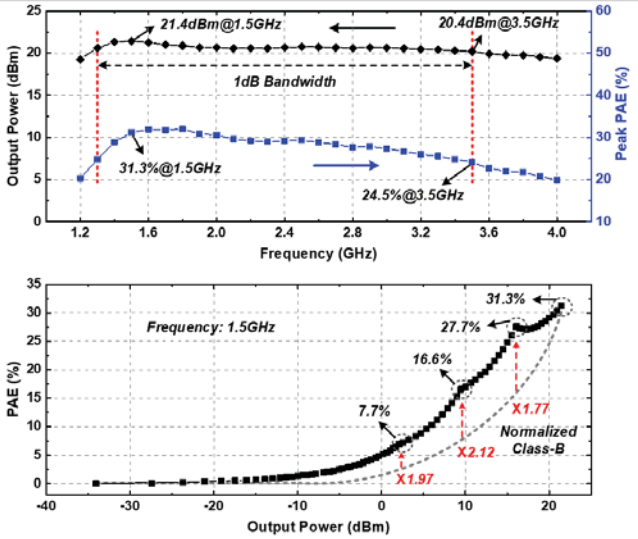

Figure 4.2.4: Measured CW results of output power, PAE (PAE=Pout/Pdc_total), and the frequency response.

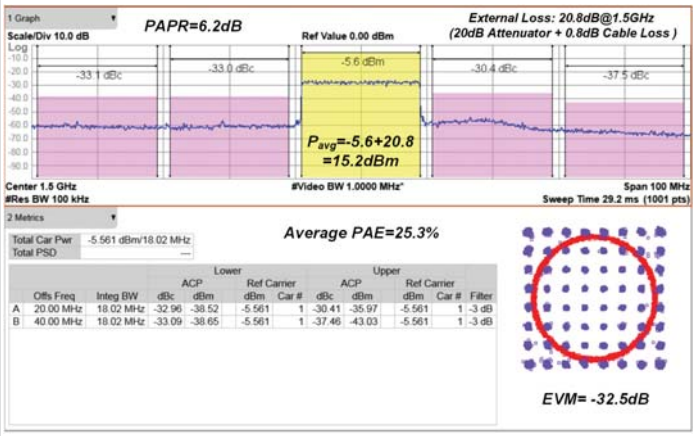

Figure 4.2.5: Measured DPA spectrum and constellation of 20MHz 64-QAM LTE signal.

	This work	ISSCC 2015 [2]*	ISSCC 2017 [3]*	RFIC 2018 [5]
Architecture	Switched transformer-based polar	Class-G+Doherty polar	Class-G+Doherty polar	Multi-level outphasing
Matching Newtork	On-chip (1 transformer)	On-chip (2 transformers)	On-chip (2 transformers)	Off-chip
PAE Improvement @Deep PBOs	6/12/18dB	6/12dB	6/12dB	2.5/6/12dB
Frequency (GHz)	1.5	3.71	3.5	1.7
1dB RF Bandwidth (GHz) (Frequency Coverage)	1.3-3.5 (91.7%)	3.1-4.7 (41.0%)	2.9-4.3 (38.9%)	NA
Peak Pout (dBm)	21.4	26.7	25.3	29.7
Peak PAE (%)	31.3	40.2 (DE)	30.4	34.7
PAE @6/12/18dB PBO (%)	27.7/16.6/7.7	37.0/26.2/NA (DE)	25.3/17.4/8*	20.5/11.5/3.5**
Modulation Signal	20MHz 64QAM LTE	1MS/s 16QAM	32 Carriers, 10MHz 256QAM	20MHz LTE
Average Pout (dBm)	15.2	20.8	19.0	23.1
Average PAE (%)	25.3	28.8 (DE)	24.0	15.3
EVM (dB)	-32.5	-24	-35.0	-21.9
Supply (V)	1.1	1.4/2.8	1.2/2.4	1.8/3.6
Chip Size (mm²)	0.8	3.2	1.2	1.31
Technology	40nm CMOS	65nm CMOS	45nm CMOS SOI	28nm CMOS

*Results measured with GSG probe. *Estimated from Fig. 6 in [3]. **Estimated from Fig. 6 in [5].

Figure 4.2.6: Performance summary and comparison with prior works.

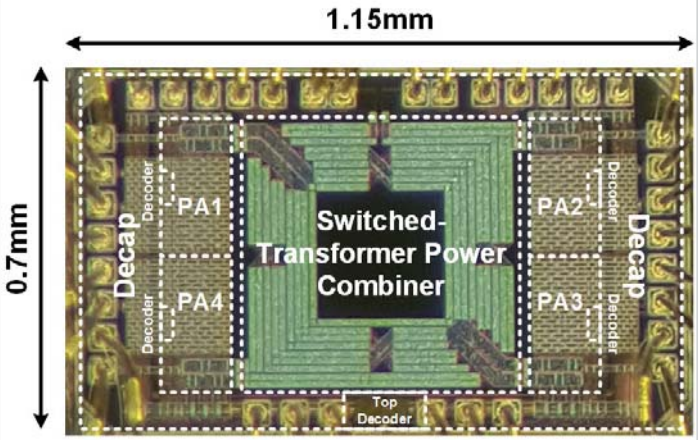

Figure 4.2.7: Die micrograph.

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