15.3 All-Digital Phase-Domain TX Frequency Synthesizer for Bluetooth Radios in 0.13μm CMOS

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Traditional designs of commercial frequency synthesizers for multi-GHz mobile RF wireless applications are based on a charge-pump PLL. Unfortunately, the required design flow and circuits techniques are quite analog intensive and utilize process technologies that are incompatible with a digital baseband, now built in a low-voltage deep-submicron CMOS process with no analog extensions.

Block diagram of the proposed frequency synthesizer that uses digital design and circuit techniques from the ground up is presented in Fig. 15.3.1. At the heart, there is a digitally-controlled oscillator (DCO) that deliberately avoids any analog tuning voltage controls [1]. Fine frequency resolution is achieved through high-speed ΣΔ dithering. This allows for its loop control circuitry to be implemented in a fully digital manner as suggested in [2]. The all-digital PLL (ADPLL) operates in a digitally-synchronous fixed-point phase domain. The variable phase $R_V[i]$ is determined by counting the number of rising clock transitions of the DCO oscillator clock. The reference phase $R_R[k]$ is obtained by accumulating the frequency command word (FCW) – a.k.a fractional frequency division ratio N – with every rising edge of the retimed frequency reference (FREF) clock. The sampled variable phase $R_V[k]$ is subtracted from the reference phase in a synchronous arithmetic phase detector. The digital phase error is filtered by a digital loop filter and then normalized by the DCO gain. It must be recognized that the two clock domains, FREF and DCO, are entirely asynchronous and it is difficult to physically compare the two digital phase values without having to face metastability problems. Consequently, the digital-word phase comparison is performed in the same clock domain. The synchronous operation is achieved by over-sampling the FREF clock by the high-rate DCO clock. The resulting retimed CKR clock is used throughout the system.

The main advantage of keeping the phase information in fixed-point digital numbers is that after the conversion, it cannot be further corrupted by noise. Consequently, the phase detector could be simply realized as an arithmetic subtractor that performs an exact digital operation. Therefore, the number of conversion places is kept at minimum: a single point where the continuously-valued clock edge delay is compared in a time-to-digital converter (TDC). It should be emphasized that it is very advantageous to operate in the phase domain for several reasons. First, the phase detector used is not a conventional correlative multiplier generating reference spurs [3]. Here, an arithmetic subtractor is used and it does not introduce any spurs into the loop. Second, the dynamic range of the phase error could be made arbitrarily large simply by increasing word-length of the phase accumulators. Conventional three-state phase/frequency detectors are typically limited to only ±2π of the compare rate. Third, the phase domain operation is amenable to digital implementations, which is quite opposite to the conventional approach.

Due to the DCO edge counting nature, the phase quantization resolution as described above cannot be better than ±1/2 of the DCO clock cycle. For wireless applications, a finer resolution is required. This is accomplished without foresaking a digitally-intensive approach. The whole-clock-domain quantization error ε is corrected by means of a fractional error correction circuit based on a TDC. The TDC (Fig. 15.3.2) measures the fractional delay difference between the reference clock and the next rising edge of the DCO clock. It has a resolution of a single inverter delay, which in this deep-submicron CMOS process is considered the most stable logic-level regenerative delay and is better than 40ps. This results in a GSM-quality phase detection mechanism, as evidenced by the excellent close-in and rms phase-noise measurement results. The TDC operates by passing the DCO clock through a chain of inverters. The delayed-clock replica vector is then sampled by the FREF clock using an array of registers whose outputs form a pseudo-thermometer code. Figure 15.3.3 shows the TDC timing and the decoded outputs. The raw binary TDC output is normalized by the DCO clock period before feeding it to the loop. The combination of the arithmetic phase detector and the TDC is considered to be a replacement of a conventional phase/frequency detector.

The oscillating frequency is dynamically controlled by directly modulating the DCO frequency in a feed-forward manner with PLL loop compensation such that it effectively removes the loop dynamics from the modulating transmit path. The rest of the loop, including all error sources, operates under the normal closed-loop regime. This method is similar to the two-point direct modulation scheme [4], but because of its digital nature, it is exact and does not require any analog component matching, except for the DCO gain $K_{DCO}=\Delta f/\Delta OTW$ calibration, which is achieved in digital domain just-in-time with every packet [5]. OTW is the oscillator tuning word and is analogous to the voltage tuning for a VCO.

Figure 15.3.4 is a simplified diagram of a near-class-E RF power amplifier whose amplitude (power) is controlled digitally with 3.5-bit precision by means of binary-weighted transistor switches followed by a matching network.

The close-in synthesizer phase noise is measured at -86.2dBc/Hz (Fig. 15.3.5). Eye-diagram and TX spectrum in Fig. 15.3.6 indicate great margin over the Bluetooth specifications. The integrated rms phase noise is 0.9^o (GSM spec: $\leq 5^o$). The close-in spurious tones are below -62dBc and the far-out spurious tones are below -80dBc. Settling time is ≤50μs. The chip has passed the official Bluetooth qualification and is in production.

Figure 15.3.7 shows a micrograph of the complete single-chip Bluetooth radio. It is fabricated in a 0.13μm digital CMOS process with copper interconnects, 1.5V transistors, 0.35μm minimum metal pitch, 2.9nm gate oxide thickness and with no extra masks. The TX part consists of the DCO, PA, ADPLL and the TX modulator. Total continuous power consumption during TX is 25mA at 1.5V supply and 2.5dBm RF output power, plus 3mA consumed by the digital baseband.

References:

[1] R. B. Staszewski et al., "A First Digitally-Controlled Oscillator in a Deep-Submicron CMOS Process for Multi-GHz Wireless Applications," *Dig. RFIC Symp.,* pp. 81–84, June 2003.

[2] R. B. Staszewski et al., "Digitally-Controlled Oscillator (DCO)-Based Architecture for RF Frequency Synthesis in a Deep-Submicron CMOS Pprocess," *Trans. on Circuits and Systems II,* vol. 50, no. 11, pp. 815-828, Nov. 2003.

[3] A. Kajiwara, M. Nakagawa, "A new PLL Frequency Synthesizer with High Switching Speed," *Trans. on Vehicular Technology*, vol. 41, no. 4, pp. 407–413, Nov 1992.

[4] M. Bopp et al., "A DECT Transceiver Chip Set Using SiGe Technology," *ISSCC Dig. Tech. Papers*, pp. 68–69, Feb. 1999.

[5] R. B. Staszewski et al., "Just-in-Time Gain Estimation of an RF Digitally-Controlled Oscillator," *Dig. CICC Conf.*, pp. 571–574, Sept. 2003.

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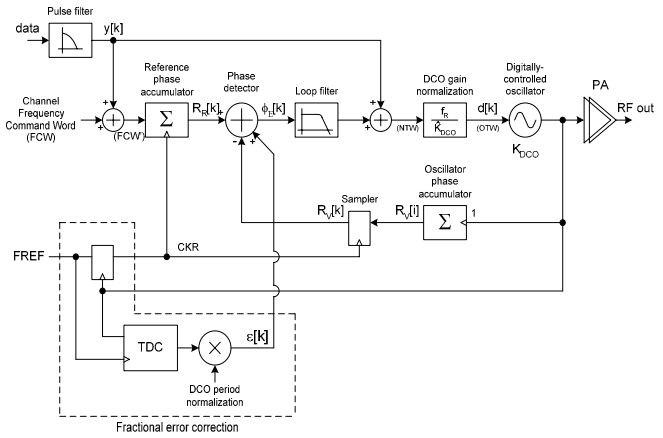

Figure 15.3.1: Synchronous phase-domain all-digital PLL-based transmitter.

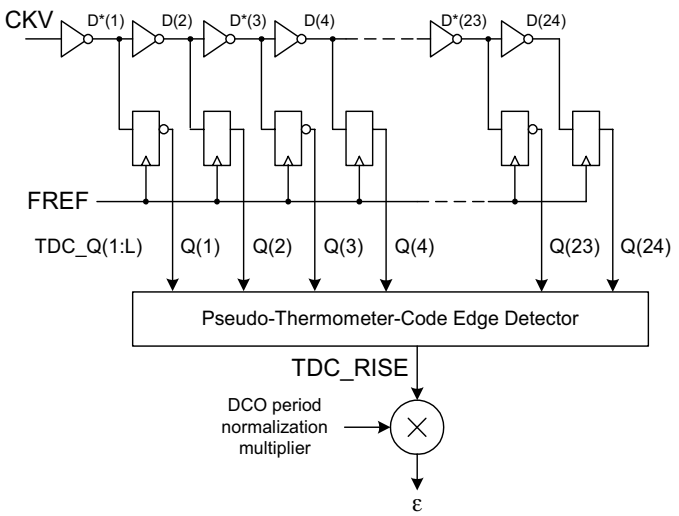

Figure 15.3.2: Fractional error correction based on a time-to-digital converter (TDC).

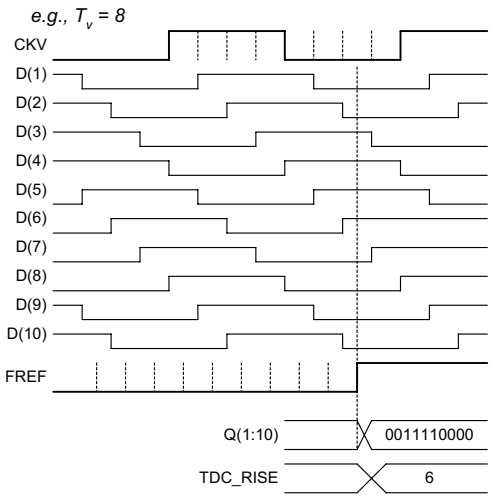

Figure 15.3.3: Timing of TDC signals.

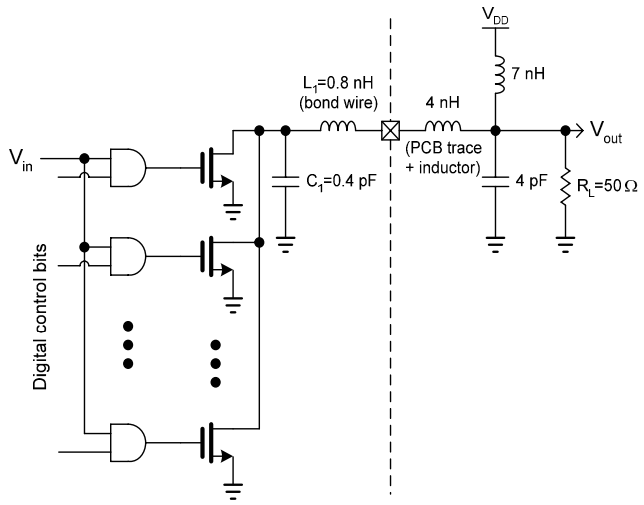

Figure 15.3.4: Near-class-E RF power amplifier with digitally-controlled amplitude regulation (half-circuit).

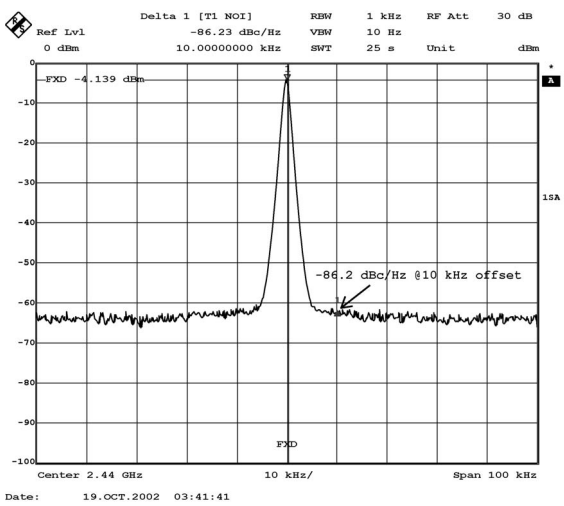

Figure 15.3.5: Close-in spectrum of an unmodulated RF carrier at 2440MHz.

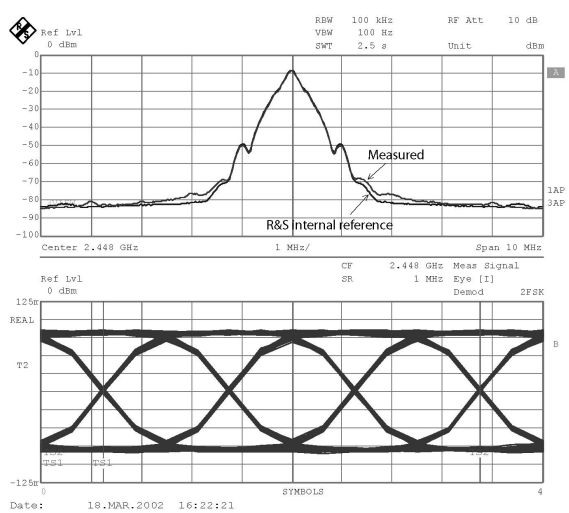

Figure 15.3.6: Measured Bluetooth TX spectrum and eye-diagram using Rohde&Schwarz (R&S) FSIQ-7 signal analyzer.

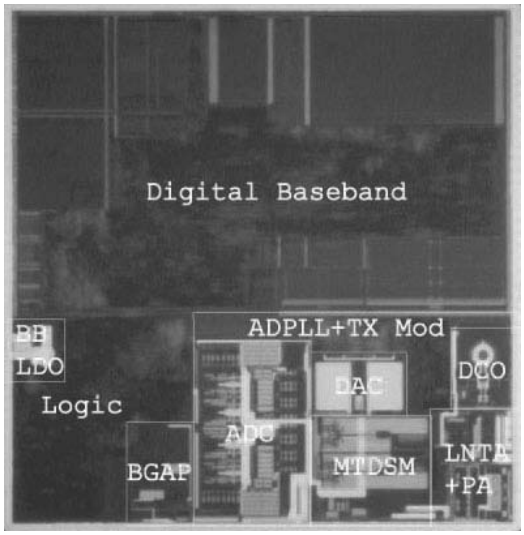

Figure 15.3.7: Die micrograph of the single-chip Bluetooth radio.

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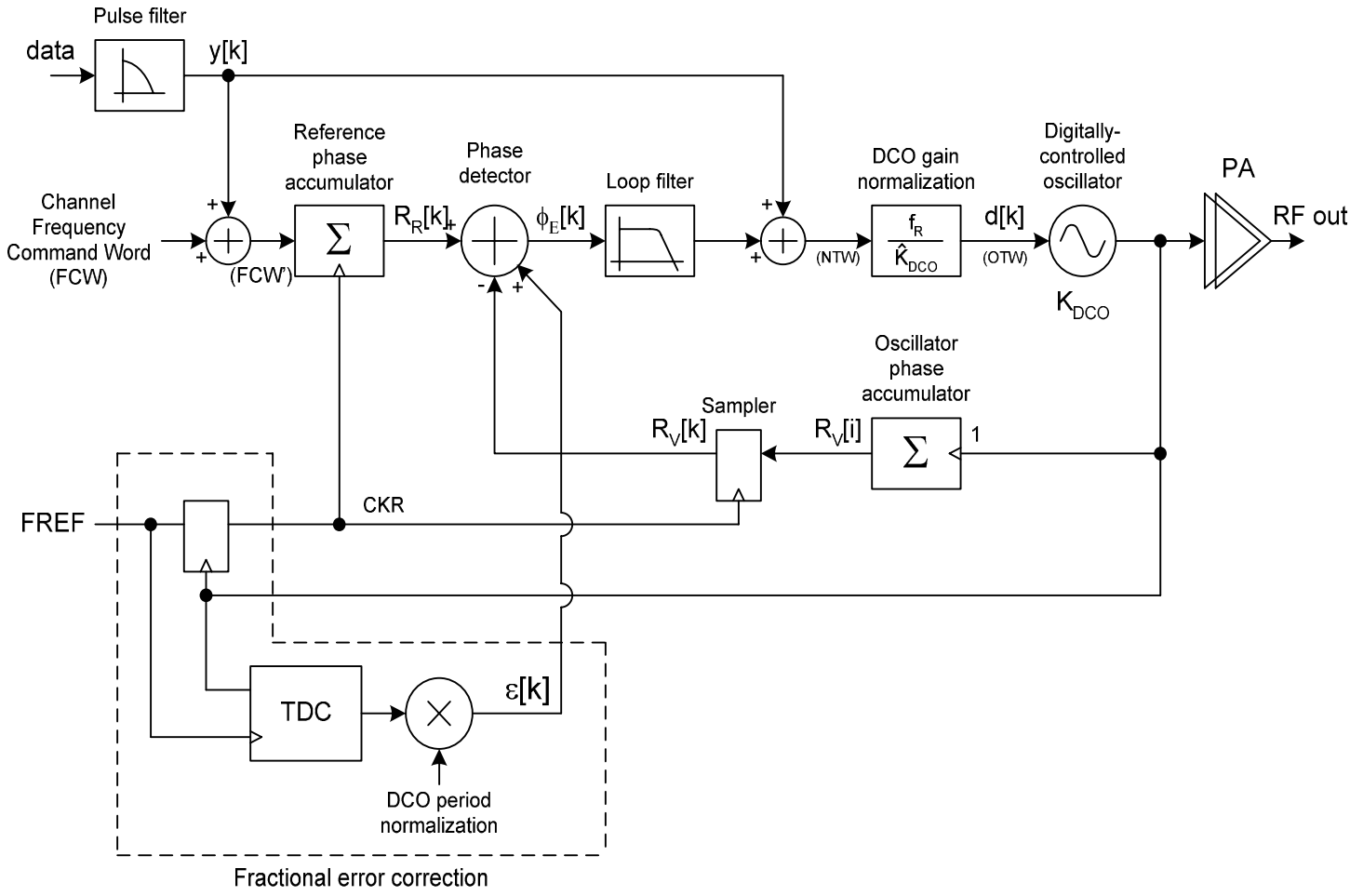

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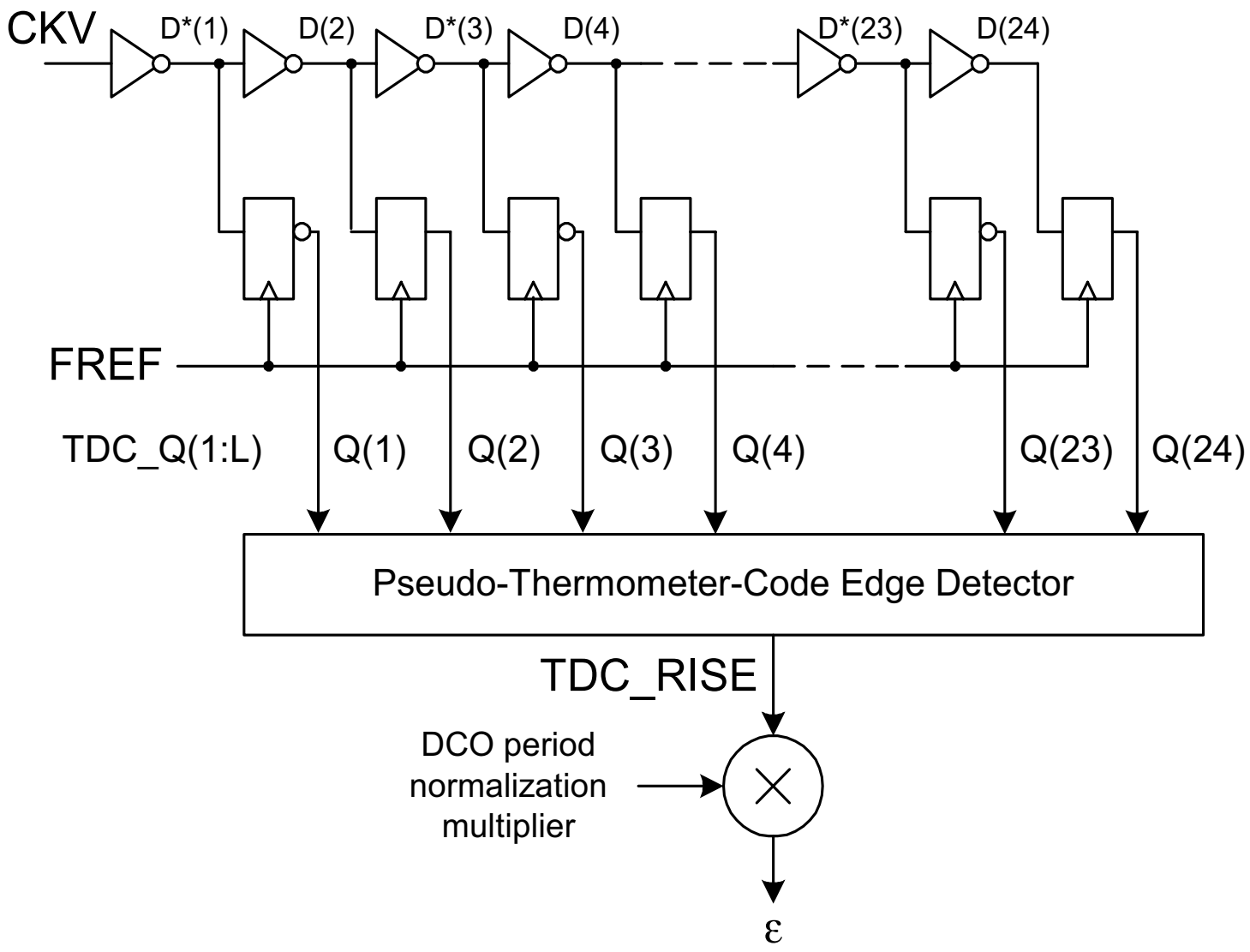

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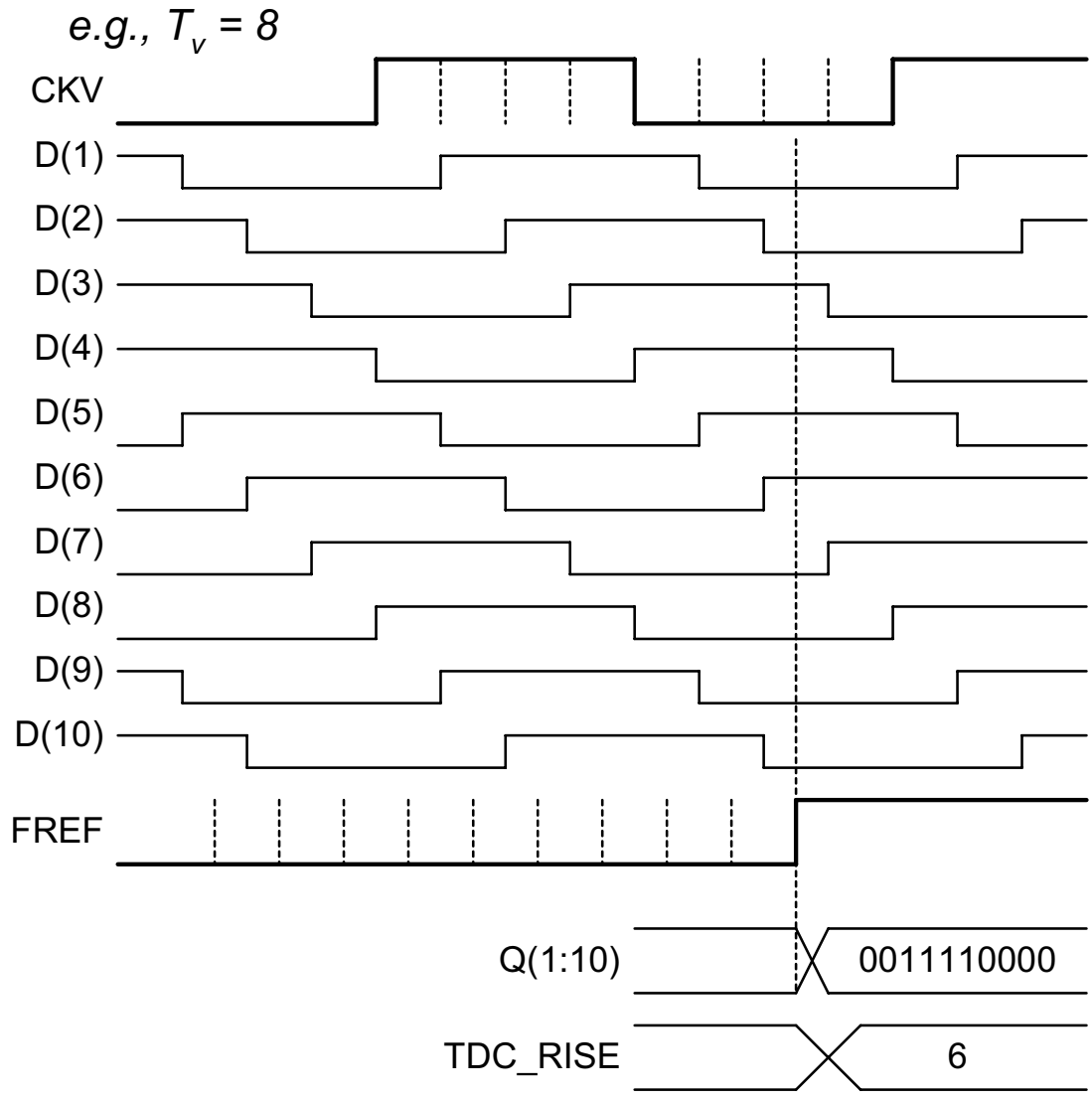

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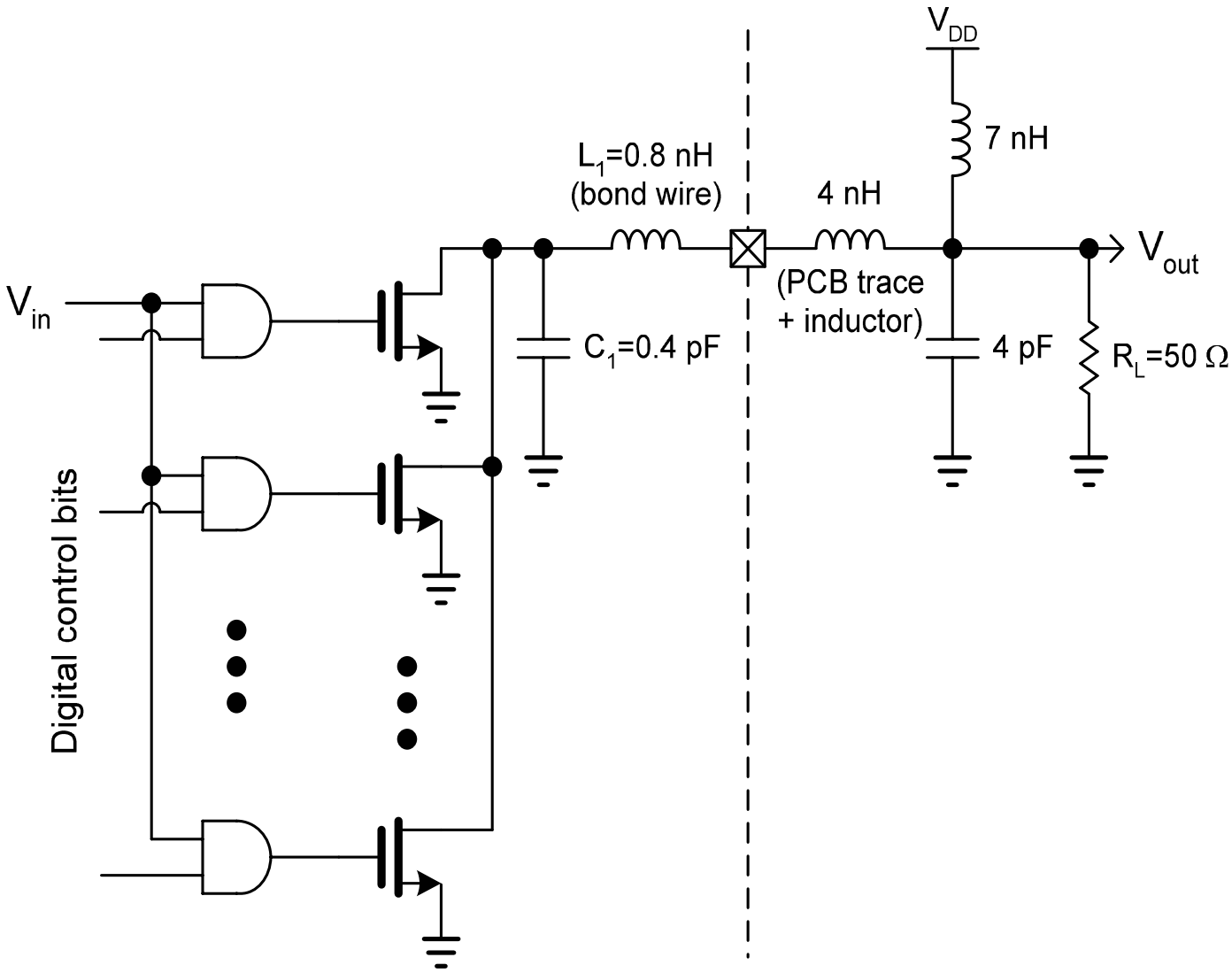

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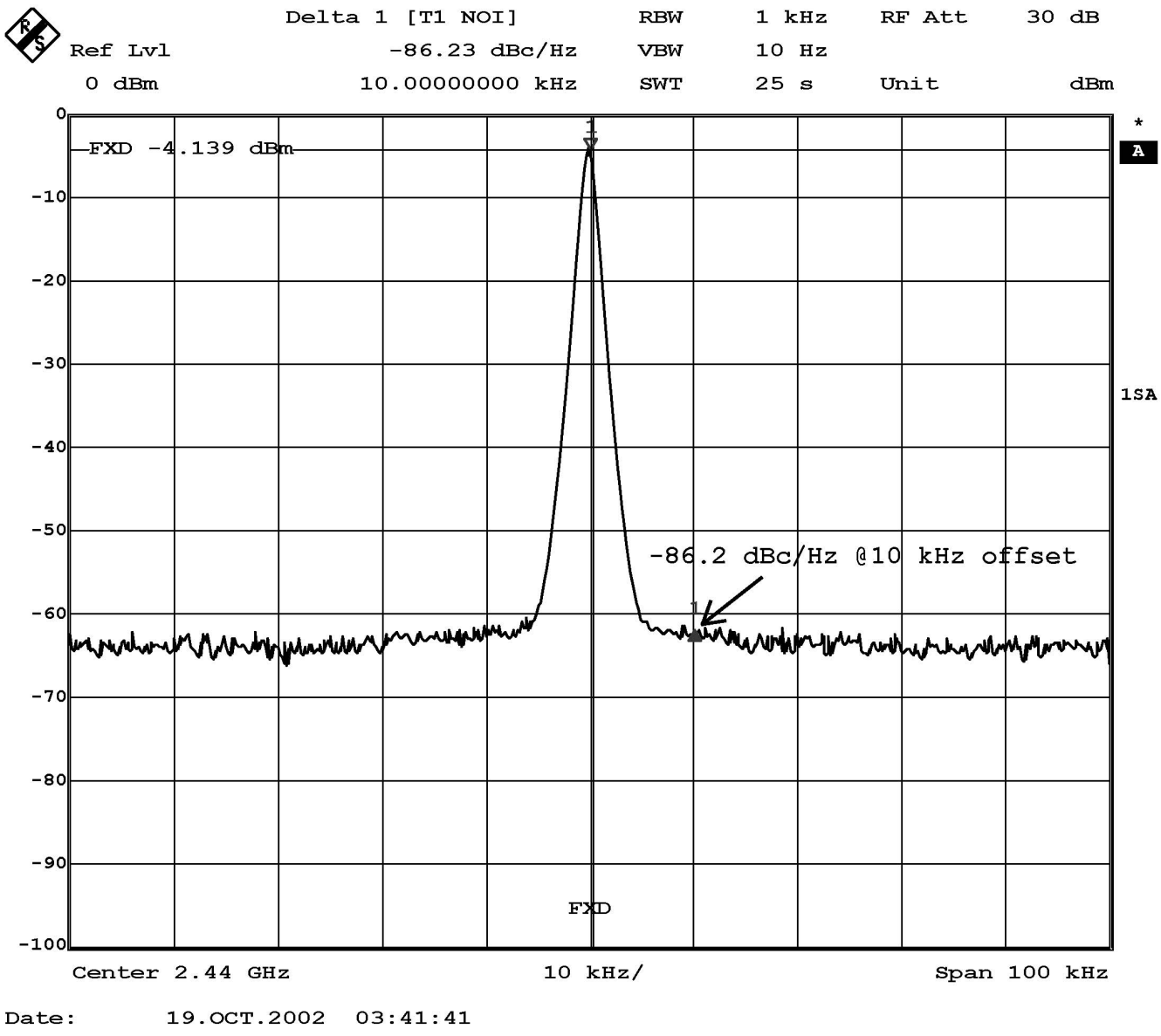

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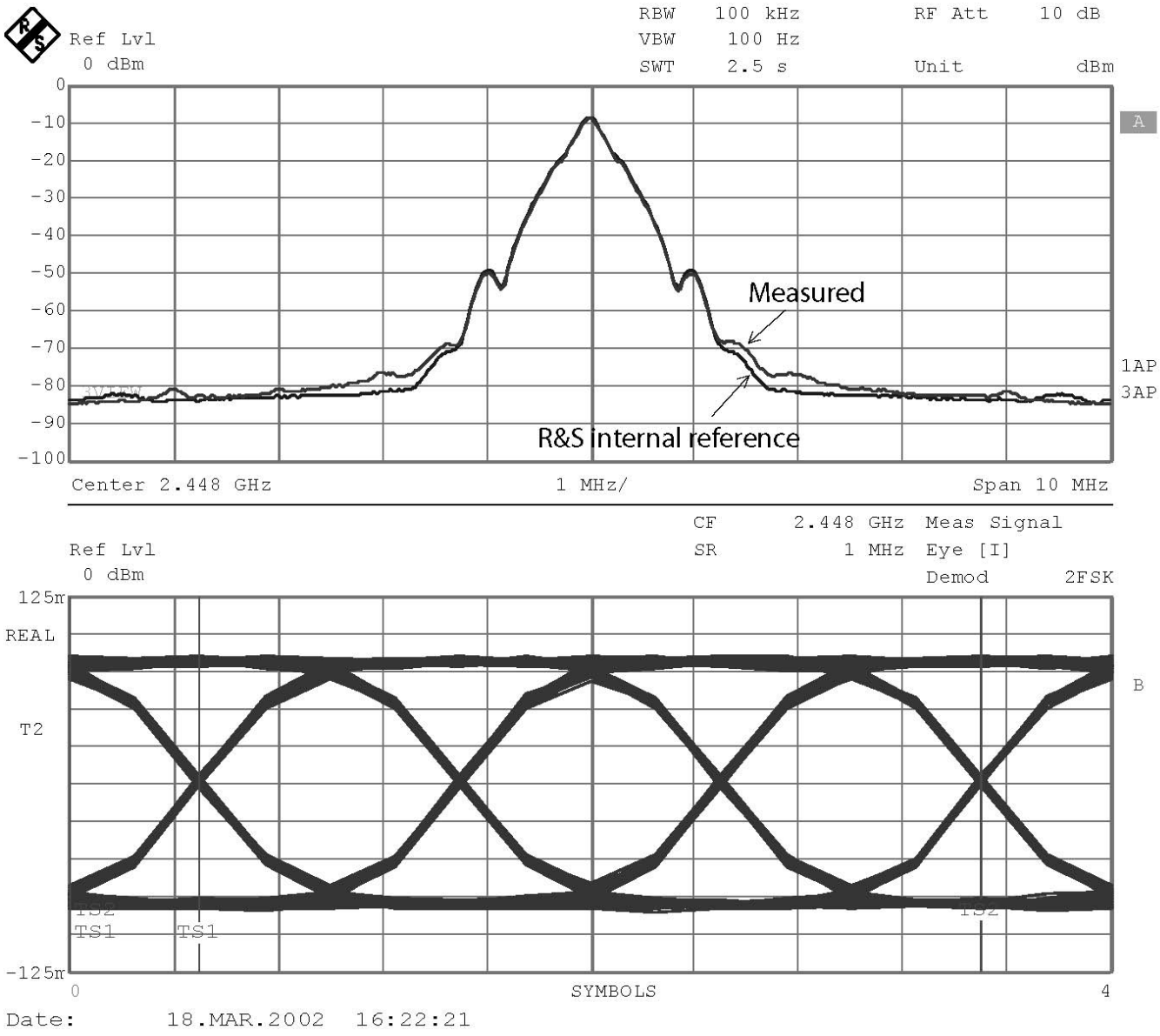

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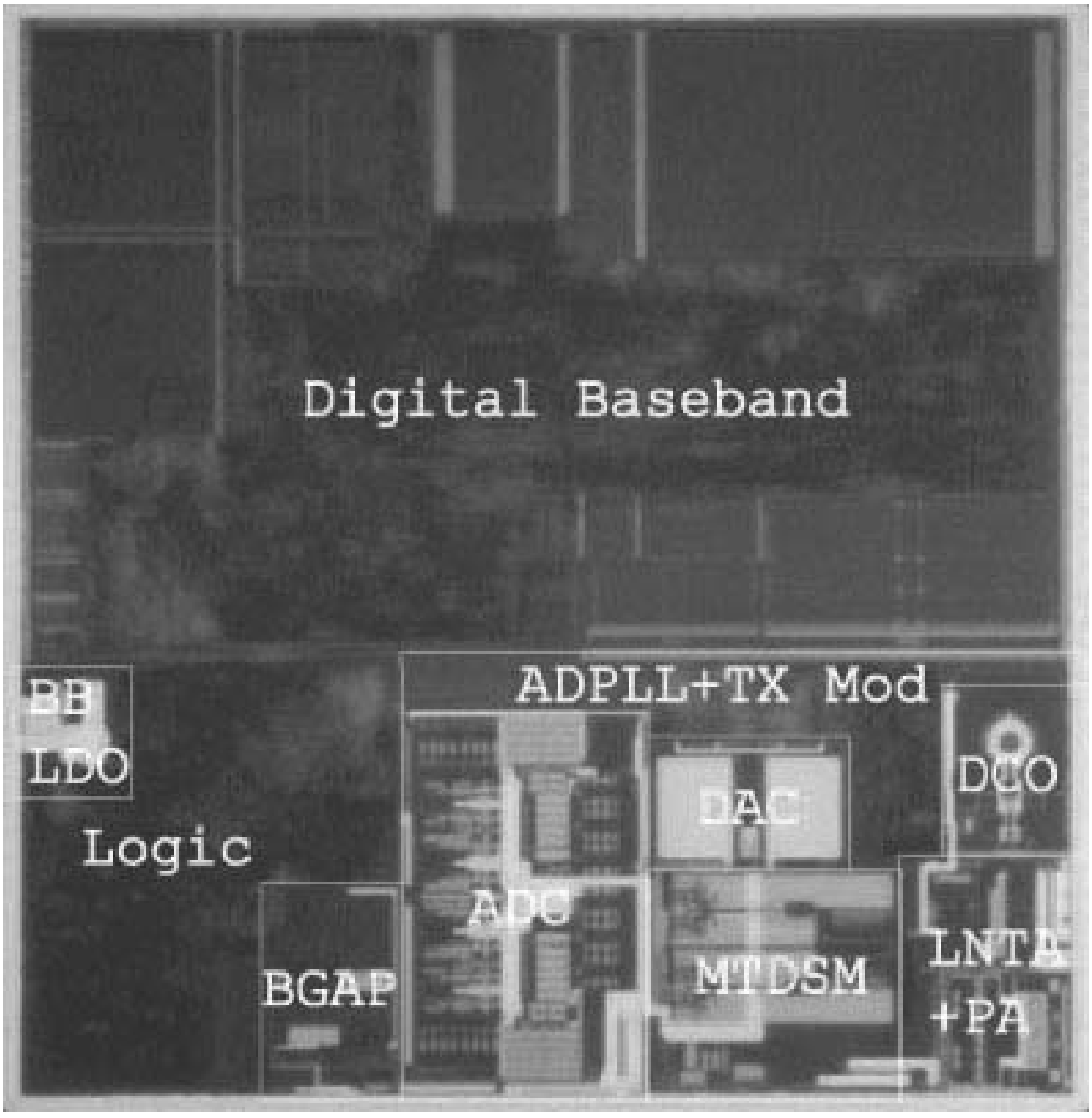

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