A 21 to 30-GHz Merged Digital-Controlled High Resolution Phase Shifter-Programmable Gain Amplifier with Orthogonal Phase and Gain Control for 5-G Phase Array Application

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Abstract—**This paper presents a 21 to 30-GHz merged passive vector sum phase shifter (PS) and programmable gain amplifier (PGA) with sub-degree phase resolution for 5-G phased array application. In PS, a transformer-based full-differential high-order resonant coupler functions as a quadrature generator (QG) with a novel layout strategy to achieve broad bandwidth, low loss, and accurate quadrature phase within only one inductor-footprint. Compared to the conventional transformer-based fourth order resonant coupler, the proposed resonant coupler with higher order features much wider quadrature bandwidth. Two phase invariant 6-bit binary-weighted arrays of vector modulators scale the quadrature signals to achieve the desired high resolution vector phase interpolation. In PGA, a phase invariant and dB-linear gain is achieved by adopting a "fractional-bit-based" PGA design. The chip prototype is fabricated in a 65-nm CMOS process, this implementation achieves 43% fractional $\text{BW}_{-3\text{dB}}$ (20 to 31-GHz). The phase control operates with 0.8° steps while maintaining a minimum RMS phase error of 0.42°, demonstrating the best phase accuracy when compared to state-of-the-art mm-wave PSs.**

Keywords— **Phase shifter, programmable gain amplifier, ultra-compact, high-order, quadrature generator, phased array.**

I. INTRODUCTION

Emerging 5-G mm-wave networks require large array-size beamforming systems to improve the link budget and system capacity. Fig. 1 illustrates an example of All-RF phased array transceiver front-end module (FEM). The phase shifter (PS) is one of the most critical blocks in phased array systems, since its phase resolution and phase shifting range dominate the beam-forming. The phase resolution directly translates to beam steering resolution (Fig. 1), thus a high resolution PS is highly recommended. Phase-invariant programmable gain amplifier (PGA) with accurate dB-linear gain control and high resolution is another critical block required at each element to compensate for gain/loss variations between radiating elements and reduce side lobes through amplitude tapering [1]. From a system perspective, orthogonal beam steering, sidelobe suppression functions and accurate dB-linear gain control are essential to ease the calibration of phase array. To achieve orthogonal beam steering control and sidelobe suppression, the phase and amplitude control in each element should be independent [1].

Conventional passive PSs like reflection-type PSs (RTPS) [2] or switch-type PSs (STPS) [3] naturally feature high linearity but also rely on higher loss and larger die area for higher resolution. Active vector modulator-based PSs [4] typically suffer from low linearity and narrow bandwidth. To addresses all the aforementioned issues, a transformer-based full-differential ultra-compact high-order resonant coupler is proposed in this work to function as a quadrature generator (QG) to achieve broad bandwidth, low loss, and accurate quadrature phase within only one inductor-footprint. Two phase invariant 6-bit binary-weighted arrays of vector modulators (VMs) scale the quadrature signals to achieve the desired high resolution vector phase interpolation, independent phase control and high linearity (Fig. 2).

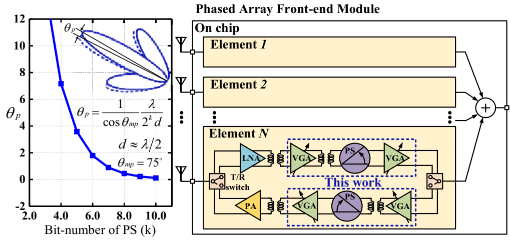

Fig. 1. Typical block diagram of an N-element All-RF phased array transceiver (right) and the effect of PS bit-number (i.e. resolution) on beam steering step-size (left), where d represents the element spacing, θ_{mp} represents the phase gradient, and θ_p represents the beam steering resolution.

To achieve independent and accurate dB-linear gain control, The PGA utilizes a novel robust "fractional-bit-based" method and achieves mathematically zero phase variant and accurate dB-linear gain across a wide tuning range with low power consumption and wide bandwidth (Fig. 2).

II. VECTOR MODULATOR-BASED PASSIVE PS

A. A Fold Transformer-Based Full Differential Ultra-Compact High-order QG

The QG is a critical block in a VM-based PS, as its performance largely governs the phase interpolation quality. Compared to RC-CR poly-phase filter and Lange Coupler, the transformer-based QG (Fig. 3(a)) is preferred in mm-wave applications due to the low insertion loss and compact layout. The bandwidth of the conventional transformer-based QG is mainly limited by the I/Q magnitude and phase mismatches. In [2], multiple transformer-based QG are cascaded to form a high-order poly-phase network to substantially extend the quadrature signal generation bandwidth with the cost of larger die area and greater passive loss, which is unacceptable for

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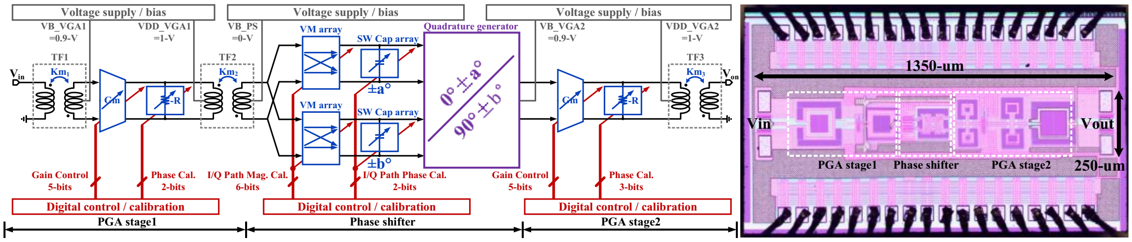

Fig. 2. Block diagram and die photo of the proposed merged PS-PGA, core area: 0.34-mm^2.

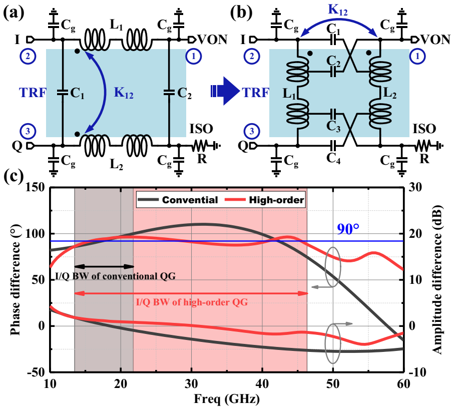

Fig. 3. (a) The circuit schematic of the conventional transformer-based QG, where C_g represents the grounded capacitor. (b) The single-ended equivalent form of the proposed transformer-based high-order resonant coupler. (c) Comparison of the I/Q bandwidth of conventional and proposed high-order QG.

large array-size beamforming systems. To address the challenge, we propose a folded transformer-based high-order poly-phase resonant coupler to suppress I/Q magnitude and phase mismatches and achieve ultra-broadband operation, the simplified single-ended equivalent form is shown in Fig. 3(b). Two additional capacitors are introduced and all the capacitors (C_{1to4}) are placed between a primary/secondary port and part of the secondary/primary inductor to increase the order of the resonant coupler. With higher order, more pairs of pole-zero poles are introduced, making the 3-dB quadrature relationship ($S_{21}/S_{31}=j$) of the resonant coupler been interpolated into more roots, so that the phase and magnitude errors are substantially suppressed and the quadrature fractional bandwidth (phase error < 2°, magnitude error < 0.5-dB) is greatly expanded from 49.3% (13 to 21.5-GHz) to 112.6% (13 to 46.5-GHz) (Fig. 3(c)). In addition, with the re-arrangement of the port order, the resonant coupler can also function as an impedance converter for the front and rear stages with easier dc feed, and the added capacitors decrease the required inductance and leads to further size reduction.

The single-ended transformer based quadrature generation scheme can be extended to a fully differential scheme with constructive magnetic coupling for further substantially size reduction. Two identical singled-ended high-order resonant coupler-based QG can be placed side-by-side for full differential operation (Fig. 4(a)). With a differential mode operation, the current directions in the two transformers are contrary, making it feasible to fold the two transformers into one structure within a single inductor footprint (Fig. 4(b)). The folding operation introduces additional magnetic coupling (K_{13} and K_{24}) and ensures magnetic coupling enhancement of the two single-ended resonant couplers, the additional magnetic coupling leads to further reduction of required inductance and die area. The shunt capacitors at I and Q ports C_{dv} are implemented with switched capacitor arrays for quadrature calibration. The physical layout implementation of the proposed fold transformer-based full differential high-order QG is shown in Figure 4 (c). The coils of TRF1 (L1 and L2) occupy the second and fourth windings, while the coils of TRF2 (L3 and L4) occupy the first, third and part of the fifth windings. The coil lengths of TRF1 and TRF2 are kept the same to ensure the same inductance. It is worth noting that the core area of the proposed QG is only 90-μm by 70-μm, achieving size reduction of over 100 times compared to a 28-GHz λ/4 Lange Coupler. The simulated behavior of the proposed QG is shown in Fig.3, demonstrating ultra-wide quadrature bandwidth with 0.9-dB passive loss at 28-GHz.

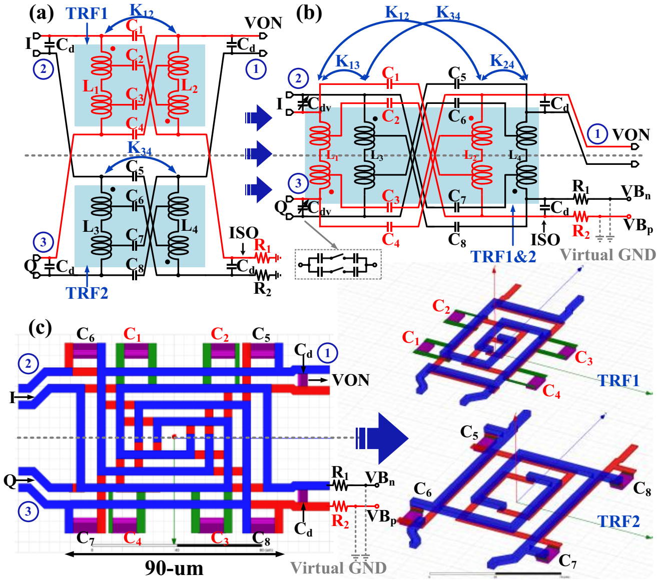

Fig. 4. (a) The circuit schematic of the transformer-based full differential high-order QG, where C_d = C_g/2. (b) The circuit schematic of the fold transformer-based full differential high-order QG. (c) The physical layout implement of the fold transformer-based full differential high-order QG.

B. *Passive Vector Modulator-Based PS Design*

The architecture of the proposed PS is shown in Fig. 2. Two phase invariant VM arrays scale the quadrature signals to achieve the desired high resolution vector phase interpolation. Each VM array is implemented as phase variant 6-bit binary-

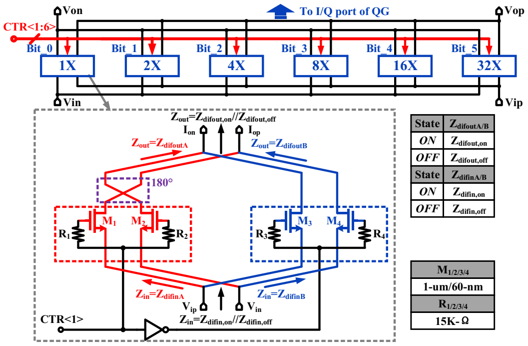

Fig. 5. The circuit schematic of the 6-bit binary weighted VM array. The Bit_N VM cell is used to generate normalized “2^N” or “-2^N” weighting.

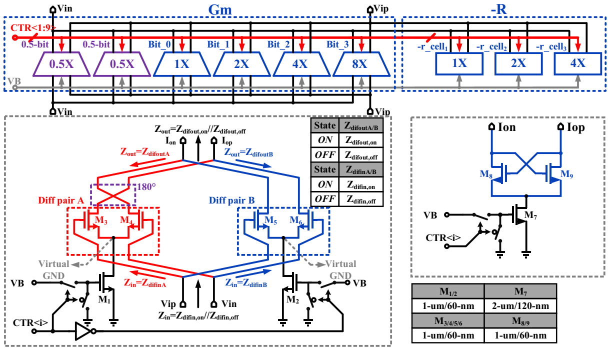

Fig. 6. The circuit schematic of the 6-bit binary weighted gm-cell array and negative resistance array (Gm and –R in Fig. 2).

weighted VM cells connected in parallel (Fig. 5). The VM cells are implemented as polarity selectors with unchanged input and output impedance to ensure phase invariance and thus achieve high phase resolution for PS. The VM array can achieve normalized AC current for all the odd integers within range of -63 to +63 ($\pm2^0\pm2^1\pm2^2\pm2^3\pm2^4\pm2^5$) with the resolution of 2. Summation of the weighted currents from I/Q paths is achieved by connecting two VM arrays to the proposed QG. The VM array naturally shows superior linearity performance than active amplifiers and the low input impedance of VM array further reduces the passive loss of QG compared to active common-source amplifying stages.

III. “Fractional-Bit-Based” Phase-Invariant PGA

The architecture of the “fractional-bit-based” PGA is shown in Fig. 2. The binary weighted cells in the PGA are implemented as polarity selectors with digital controlled differential common-source amplifiers (Fig.6). The complementary control signal determines the polarity of the output currents with unchanged input and output impedance. Constant input and output impedance guarantees unchanged parasitic capacitive loadings for a bit-setting-independent and phase invariant frequency response. As the integer-bit (0/1/2/3-bit) cell is used to generate normalized “2^N” or “-2^N” weighting, the PGA can achieve normalized AC output currents for all the odd integers within range of -15 to +15 ($\pm2^0\pm2^1\pm2^2\pm2^3$) with the resolution of 2. To improve the gain resolution and obtain accurate dB-linear gain, two fractional-bits (0.5-bit) are introduced to ensure the normalized gain of the PGA can be set between –16 to +16 ($\pm(0.5\pm0.5)\pm2^0\pm2^1\pm2^2\pm2^3$) to achieve dB-linear gain with the resolution of 1. It is noteworthy that this scaling method is independent of transistor modeling, and thus robust to modeling inaccuracy and PVT variations.

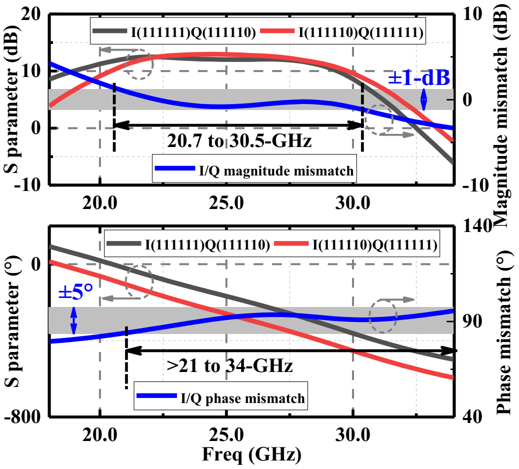

Fig. 7. The I/Q magnitude (up) and phase (bottom) difference of the merged PS-PGA.

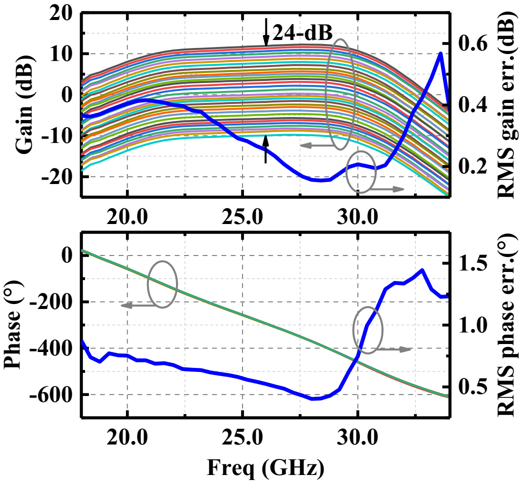

Fig. 8. Measured gain response and RMS gain error (up). Measured phase response and RMS phase error (bottom).

IV. Measurement Result

The chip is fabricated in a 65-nm CMOS process while occupies 1350-μm by 250-μm die area (Fig. 2) and consumes 12-mA from 1-V supply voltage. We perform all characterizations using an N5247A network analyser. The I/Q gain and phase difference of the proposed high-order QG was indirectly measured by turning on only the I-path and Q-path VM arrays of PS (*ON* word = ‘111111/000000’, *OFF* word = ‘111110/000001’) as shown in Fig. 7, The measured quadrature frequency of the merged PS-PGA is wider than 37% (21 to 30.5-GHz), demonstrating the quadrature bandwidth of the proposed high-order QG is much wider than 37%. The higher-order effect is also evident in Fig. 7. Fig. 8 shows the measured gain response of the merged PS-PGA, which achieves 43% fractional BW_{-3dB} (20 to 31-GHz) with 12.2-dB

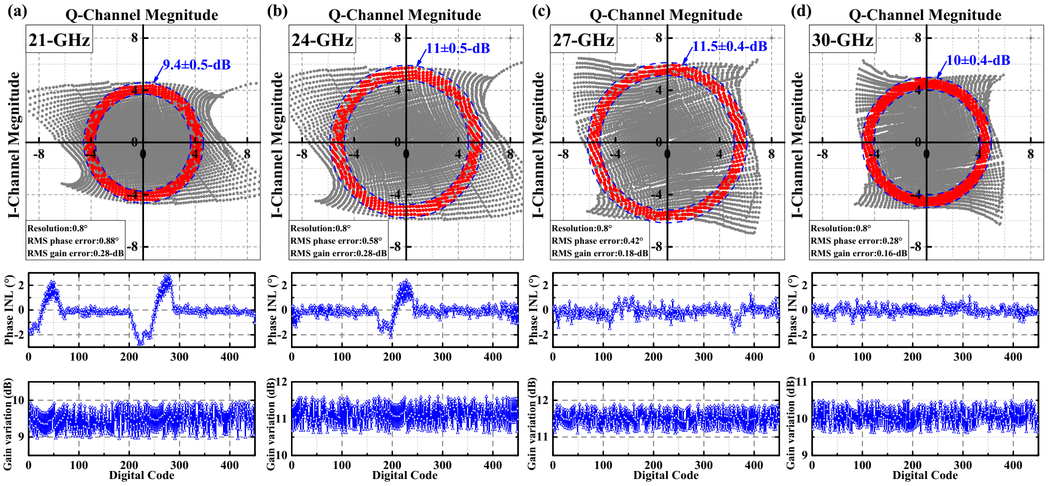

Fig. 9. Measured constellation points on the I/Q channel coordinates showing four phase interpolation examples with 0.8° step and 0.4/0.5-dB magnitude variations at (a) 21-GHz, (b) 24-GHz, (c) 27-GHz and (d) 30-GHz. The RMS phase errors are 0.88°, 0.58°, 0.42°and 28°, respectively. The RMS gain errors are 0.28, 0.28, 0.18 and 0.16-dB, respectively (up). Measured phase Integral nonlinearity (INL) error and gain variation vs. digital code (middle and bottom)

Table 1. Performance comparison of state-of-the art

	[1]	[3]	[4]	[5]	**This Work**
Type	Passive		Active		Passive +PGA
Tech.	130-nm SiGe	40-nm CMOS	SiGe	65-nm CMOS	65-nm CMOS
Freq (GHz)	28	22-36	20.5-26.5	27-29	21-30
Range (deg)	190	360	360	360	360
Phase res.(º)	91	45	5	5.625	0.8
RMS phase err. (deg)	0.6	<12.8	0.55-21	0.54	0.28-0.88
Gain var.(dB)	0.25	0.5	0.75	0.47	0.4-0.5
RMS gain err. (dB)	N/A	<0.6	>0.5	0.13	0.16
Gain (dB)	-9.3	-5.6	0.51	-3.1	12.2
Area (mm2)	0.18	0.132	0.12	0.32	0.052
Power (mW)	0	0	10	25.2	12

[1] Estimate from figures [2] Only core area of PS

maximum gain and 24-dB gain range with 0.75-dB gain step. The RMS gain error is less than 0.4-dB from 18 to 32-GHz with the minimum value of 0.18-dB at 28-GHz, demonstrating high accuracy of dB-linear gain. The RMS phase error is plotted in Fig. 8 (bottom), and the value is less than 1° from 18 to 30-GHz, demonstrating that the "fractional-bit-based" PGA features independent, accurate gain control.

Fig. 9 shows the measured constellation points on the I/Q channel coordinates with 0.8° phase step within 0.4/0.5-dB amplitude variation at 21/24/27/30-GHz. The results demonstrate that thanks to the proposed high-order QG the merged PS-PGA achieve phase and magnitude bandwidth of wider than 37%. Table I compares this work with state-of-the-art, this work demonstrates the best phase accuracy with highest resolution and wide bandwidth.

V. CONCLUSION

This paper demonstrates a novel passive VM-based PS merged with two "fractional-bit-based" PGA stages. The PS employs a folded transformer-based high-order full-differential QG to substantially extend the quadrature bandwidth and reduce the die area. The PGA utilizes a novel robust "fractional-bit-based" method and achieves mathematically zero phase variant and accurate dB-linear gain across a wide tuning range. The phase control operates with 0.8° steps while maintaining a minimum RMS phase error of 0.42°, and the gain control operates with 0.75-dB steps while maintaining a minimum RMS gain error of 0.18-dB.

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