

A 1.7-2.1GHz +23dBm TX Power Compatible Blocker Tolerant FDD Receiver with Integrated Duplexer in 28nm CMOS

Matteo Ramella⁽¹⁾, Ivan Fabiano⁽²⁾, Danilo Manstretta⁽¹⁾, and Rinaldo Castello⁽¹⁾

⁽¹⁾ University of Pavia, Pavia 27100, Italy ⁽²⁾ Marvell, Pavia 27100, Italy

Abstract — The first integrated duplexer compatible with a -15dBm RX blocker for up to 23dBm TX power is reported. A three winding transformer is driven at the primary by a single ended PA and drives a differential push-pull common-gate LNA. Only 45 dB isolation is required thanks to the 23 dBm RX IIP3 drastically simplifying hybrid balancing and adaptation loop. Cascaded noise figure of duplexer, LNA and base-band stays below 6.7dB and the TX insertion loss below 4 dB from 1.6 to 2.2 GHz. The chip is implemented in 28nm CMOS has an active area of 0.7mm² and uses only 26mW.

Index Terms — cellular communications, duplexers, FDD balancing network, isolation, duplexers, tunable circuits.

I. INTRODUCTION

In today's transceivers a different radio for each band with external SAW filters is used. As MIMO and Carrier Aggregation are extended, both passives and pin count increase. Single-ended blocker-tolerant SAW-less TDD receivers have been reported [5]. In FDD systems, due to the finite TX-RX isolation, the TX signal leakage may intermodulate with blockers, leading to challenging IIP3 requirements. The two reference scenarios (Half Duplex and Full Duplex) are sketched in Fig. 1. The required antenna referred IIP3 are $IIP3_{HD} = (P_{TX} + 2P_B + 99\text{dBm})/2$ and $IIP3_{FD} = (2P_{TX} + P_B + 99\text{dBm})/2$ respectively, where P_{TX} and P_B are TX and blocker power in dBm. As an example with 23 dBm P_{TX} and -15 dBm P_B , $IIP3_{HD} = 46$ dBm and $IIP3_{FD} = 65$ dBm. A typical duplexer reduces P_{TX} and P_B by 50 to 55 dB drastically relaxing receiver $IIP3_{RX}$. This makes it hard to keep TX noise and IM3 products below the RX noise floor (-99dBm) without duplexer. In duplexer-less transceivers (DLT) TX-RX isolation is based on an impedance-balanced hybrid transformer [1-4]. Even though TX-to-RX isolations of up to 70dB were reported (over a very narrow band), nonetheless the IIP3 requirements in half-duplex and full-duplex scenarios were not met. Moreover, when a realistic PIFA antenna model is considered, the minimum achievable TX-to-RX isolation across a bandwidth of just a few MHz is below 50 dB [2]. With the blocker passing un-filtered, this translates into a required receiver $IIP3_{RX}$ above 20 dBm ($IIP3_{RX} > IIP3_{FD} - ISO_{TX-RX}$ and $IIP3_{RX} > IIP3_{HD} - ISO_{TX-RX}/2$), making the blocker immunity of reported DLT inadequate in real life. Regarding TX noise leakage to RX, the duplexer relaxes it by at least 45 dB. Although 45 dB cancellation through impedance balancing is feasible, the problem is maintaining it across the frequency span that separate TX from RX. A more complex double-notch canceller addresses this problem [2]. In this work the strategy is to rely on high receiver linearity to bring the required balancing accuracy in both TX and RX band around 45 dB. This has the potential to drastically simplify DLT, making them feasible in real life.

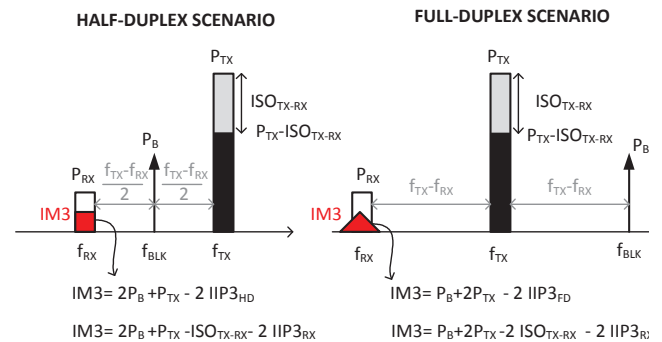


Fig. 1: Blocker and TX-leakage intermodulation scenarios.

II. SYSTEM DESIGN CONSIDERATIONS

The idea behind a DLT is the use of a balanced hybrid to decouple TX from RX. As shown in Fig. 2, the PA drives the center tap of either an auto-transformer or the primary of a transformer. The first choice minimizes transformer losses but cannot meet distortion targets since the full TX appears at the LNA input as common mode (CM). The second choice has higher losses but decouples the TX signal from the LNA. In actuality, capacitive coupling between windings limits CM rejection to about -40dB [2] preventing sufficient blocker immunity with common source LNAs. A possible way to address this problem is to put the balance impedance between antenna and RX (with a single-ended LNA) [3] or to drive the antenna differentially [2]. For the latter case the external balun adds 1dB loss and increases cost. All reported DLT use LNAs with IIP3 below 6 dBm, so even with 70 dB isolation their IIP3 is too low. This paper addresses these problems in several ways. First, a large common mode can be managed by the LNA avoiding the need for a differential PA (with external balun). Second, a noise matched push-pull common base LNA gives almost 25 dB more IIP3 (for the same NF and current) than a common source and a lower trans-conductance (improving baseband linearity). Third, the complete RX analog front-end is integrated with the hybrid. Fourth, a linear balancing circuit is integrated in a 28nm CMOS technology with enough tuning range to track the antenna impedance with antenna tuning.

III. RECEIVER CHAIN

The LNA core consists of a push-pull common-gate amplifier with cross-coupled feed-forward capacitors. This configuration, used in the SAW-less receiver in [5], in this design is driven by the two secondary of the hybrid transformer, as shown in Fig. 3. The key features of the

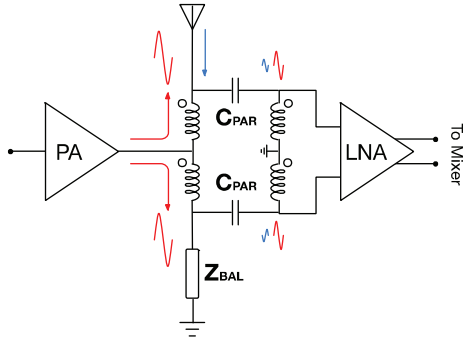


Fig. 2: Transceiver front-end with hybrid transformer-based duplexer

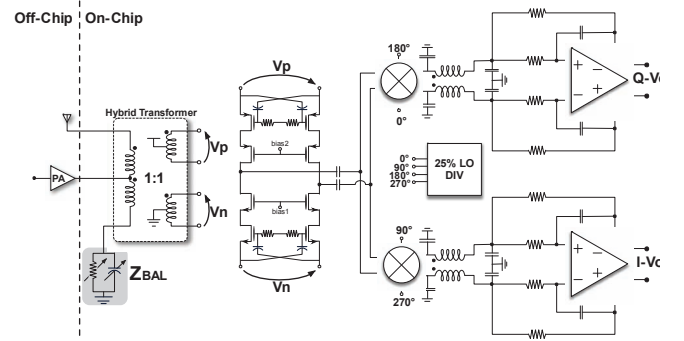


Fig. 3: Receiver front-end schematic with integrated hybrid transformer

proposed solution are excellent IIP3 at low bias current and high common mode immunity. Contrary to the design in [5] the common-gate amplifier is not power matched to its source. By making the common-gate amplifier input impedance much smaller than its driving impedance, as in a cascode, transistors noise is reduced and IIP3 is increased. Large impedance mismatch with small bias current comes from the cross-coupling of the complementary (p-n) topology and the doubling of the source impedance due to the hybrid termination ($Z_{BAL} \approx Z_{ANT}$). Notice that antenna S_{11} is kept low by Z_{BAL} and is acceptable since there is no SAW and antenna tuning is used. Moreover, cross-coupling strongly enhances common mode rejection, reducing intermodulation between TX CM leakage and RX blockers. This is because the feed-forward capacitors double the gate-source voltage of the input devices for differential signals while it nulls it for common-mode signals. Simulation shows that IM3 is not affected for a CM TX leakage up to 15dB higher than differential TX leakage. Output compression is minimized by using large cascode devices, minimizing the load impedance. The noise factor for a balanced hybrid is

$$F = 2 + \frac{R_{ANT}}{R_P} + \frac{\gamma(2R_{ANT} + R_P)^2}{16k^2 n^2 g_m R_{ANT} R_P^2} \quad (1)$$

with R_{ANT} antenna impedance, R_P , k and n transformer parallel loss resistance, coupling factor and turn ratio. The transistor noise reduction by 16 is due to impedance mismatch as explained above. For $Q = 10$ at the primary and 12 at the secondary, $\gamma = 0.7$ and $g_m = 35\text{mS}$ (6mA total current), simulated LNA NF (including hybrid loss and balancing impedance noise) is 4.7 dB and IIP3 = 26 dBm.

B. Mixer and Baseband

The LNA drives two (I/Q) 25% duty cycle passive mixers followed by two second order filters as shown in Fig. 3. The mixer is AC coupled to the LNA with 2 pF series capacitors. A parallel LC resonating at the LO fourth harmonic is placed in series with the mixer on the base band side [5]. This creates a high impedance at the 3rd and 5th harmonic of the LO on the RF side, avoiding noise folding. Care is taken to minimize parasitic capacitance at the LNA output to maximize the base band driving resistance that, together with the shunt capacitance, has a dominant effect on noise. The Rauch filter attenuates the -15dBm blockers, using low power thanks to the

use of a single opamp. The 3 MHz filter bandwidth is a reasonable compromise between selectivity and in band noise. To minimize noise and maximize linearity for a given current bias, the opamp uses a complementary p-n differential pair at the input and a push-pull stage (based on floating batteries) at the output.

C. Hybrid Transformer

The transformer turn ratio can be used to change input impedance trading off NF, power consumption and linearity. Stacked transformers have high k but low Q if only one thick metal is available. Coplanar topologies reduce common-mode coupling and maximize the Q of both primary and secondary windings but degrade NF due to a poor k . Shorting different metal layers increases both Q and capacitive coupling. Considering the above trade-offs, a coplanar three coils transformer with a turn ratio of 1 was implemented (Fig. 4). The secondary windings (outer and inner coils) use shorted AP and thick metal, while the primary (placed between the two secondary) uses only the thick metal layer.

C. Balancing Network

RX to TX isolation relies on balancing the bridge composed

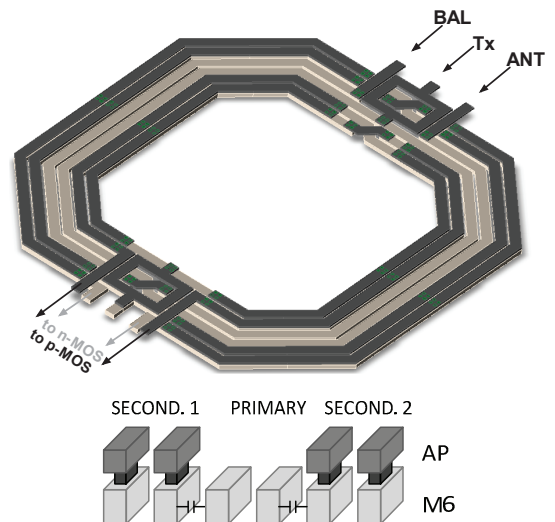


Fig. 4: Layout and cross-section of the hybrid transformer.

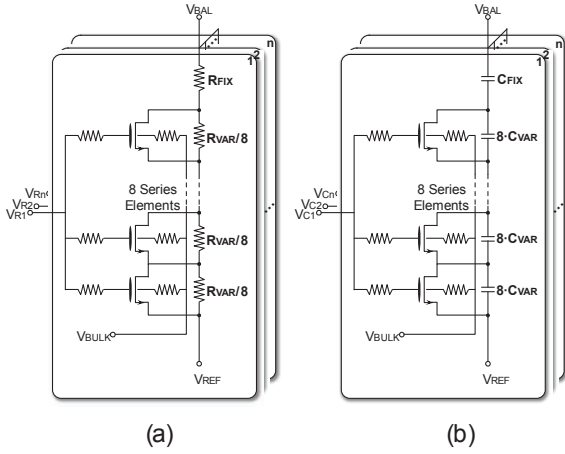


Fig. 5: Balancing Network (a) Resistor stack (b) Capacitor stack

by antenna (ANT) and balance impedance (BAL) [4]. Moreover, BAL has to be highly linear since it is directly connected to the PA [6]. A parallel array of switched resistors for BAL and two switched capacitors at the ANT and BAL ports are used (Fig. 5). To reduce device voltage swing and improve linearity, a stack of 8 series switches is used. Parasitic source/drain-bulk capacitors generate uneven voltage distribution across the stack, making the technique less effective. Therefore 28nm thin oxide NMOS transistors with switched bias and floating bulk and deep N-wells are used to minimize parasitic. Moreover, fixed resistors/capacitors in parallel with the switches ensure that each switch has a gate-source/drain voltage of 1/16 the stack input voltage. A fixed resistance/ capacitance in series with the stack provides a further 2x attenuation at the price of a reduced tuning range. The BAL resistance varies between 35Ω and 70Ω and the capacitances between 200fF and 400fF.

IV. EXPERIMENTAL RESULTS

The duplexer less transceiver was implemented in TSMC 28nm LP CMOS process with an active area of 0.72mm^2 , as shown in Fig.6. Measured and simulated gain and NF of the receiver are plotted in Fig. 7. NF goes from 6.5 dB to 6.8 dB from 1.7 to 2.3GHz, i.e. $\bullet 0.8\text{dB}$ above simulation. This is consistent with the extra noise folding due to an error in the tuning circuit of the LC tank at the mixer output, as confirmed by harmonic rejection measurements. The gain is about 36 dB and varies by less than 1 dB. TX-to-Antenna insertion loss is 4–4.3 dB. IIP3_{RX} vs two-tones frequency spacing is plotted in Fig. 8. It starts at -10 dBm with tones in band and increases as they move out of band. At 10 MHz IIP3 is 13.5 dBm and exceeds 20 dBm beyond 30 MHz with a peak of 25 dBm beyond 50 MHz, limited by the LNA. Measurements are in good agreement with simulations and are almost 20 dB better than any previously reported DLT. The measured IIP3_{RX} full-fills both HD and FD blocking requirements with TX to RX isolation of only 45 dB as opposed to more than 70 dB for all prior DLT. The balancing network can be programmed to

TABLE I
PERFORMANCE COMPARISON TABLE

	[2]	[3]	This work
Technology	65nm CMOS	0.18 μm CMOS	28nm CMOS
Area [mm^2]	2.2	0.35	0.72
Power diss. [mW]	51.1	10.5	26
Freq [GHz]	1.7-2.2	1.6-2.2	1.7-2.1
RX Gain [dB]	45	N/A	35
RX NF [dB]	6.7 ¹	6.5	6.7
RX IIP3 [dBm]	-4.6	N/A	>20dBm
$\text{IL}_{\text{TX-ANT}}$ [dB]	4.5 ¹	3.2	4
$\text{ISO}_{\text{TX-RX}}$ [dB]	>50	>60	>40
IIP3_{HD} [dBm]	22 ²	N/A	>46.5

¹ Includes 0.8dB ext. balun loss; ² extrapolated from triple-beat test and RX IIP3; [3] includes Duplexer + LNA only

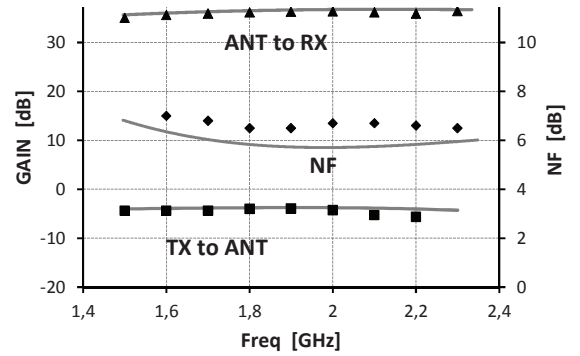


Fig. 7: Measured (dots) and simulated (lines) receiver RX gain, TX insertion loss ($\text{IL}_{\text{TX-ANT}}$) and RX noise figure.

balance the hybrid across the whole band. TX to RX isolation vs. TX frequency is shown in Fig. 9 for a fixed configuration. Up to 70 dB is achieved and 40 dB are maintained across 160 MHz. IIP3_{HD} was measured with 100 MHz TX-RX separation. The expected IM3 vs. signal power slope i.e. 2dB/dB for TX and 1dB/dB for RX is experimentally verified. For an IIP3_{RX} of 23 dBm the relationship $\text{IIP3}_{\text{HD}} = \text{IIP3}_{\text{RX}} + \text{ATT}/2$ is verified to within 1 dB up to $\text{IIP3}_{\text{HD}} = 43\text{ dBm}$ ($\text{ATT} = 40\text{ dB}$). Beyond this IIP3_{HD} saturates (at $\bullet 50\text{ dBm}$) due to other non-idealities. In any case compatibility with -15 dBm blocker up to 23 dBm TX is proven for the first time. Finally power consumption excluding LO is only 18.2 mW and total power (including LO) is 26mW. Table I summarizes the results, demonstrating a significant performance improvement over prior DLT solutions. Similar NF compared with prior implementations is achieved over a broad frequency range with equal or better power consumption (notice that [3] includes only the LNA). TX-to-antenna loss is also comparable with [2] (when balun loss is considered) and is $\bullet 1\text{dB}$ higher than in [3], where duplexer loss is tilted in favor of the TX-antenna path. Receiver IIP3 over 20dB higher than in prior DLT implementations is demonstrated. IIP3_{HD} in [2] (estimated

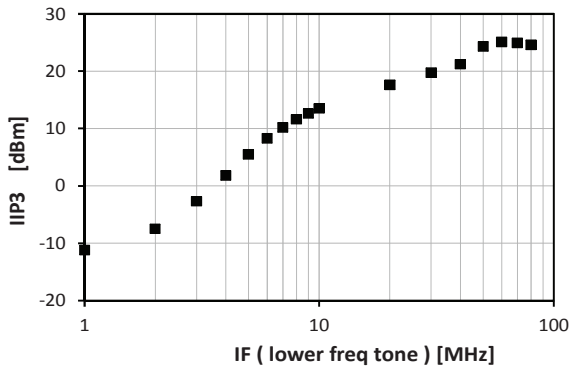


Fig. 8. Receiver IIP3 vs. blocker frequency spacing ($f_{IM3}=100\text{kHz}$).

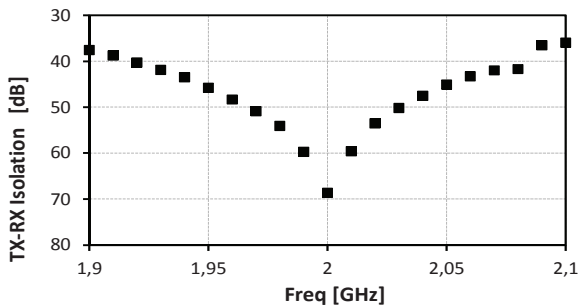


Fig. 9: TX to RX isolation (ISO_{TX-RX}) vs. frequency for a fixed balancing

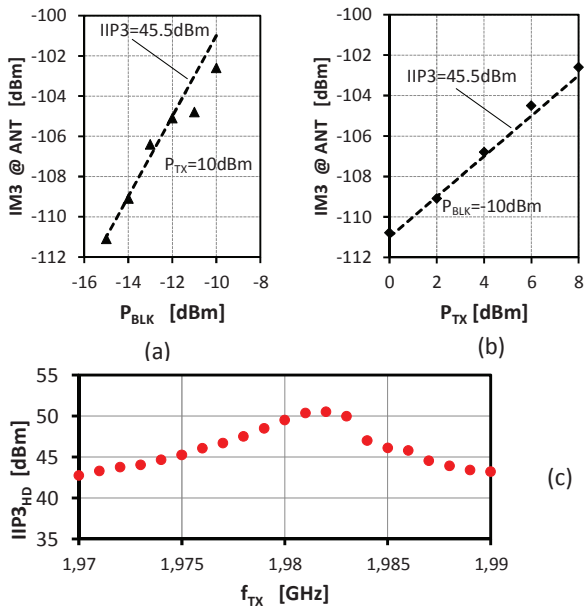


Fig. 10: HD intermodulation between TX and RX blocker. (a-b) measured IM3 referred at the antenna input; (c) $IIP3_{HD}$ vs frequency ($f_{TX}-f_{BLK}=50\text{MHz}$)

based on RX IIP3 and effective isolation measured in triple-beat test) is improved by over 24 dB.

VII. CONCLUSION

Fully integrated duplexers still need improvements especially in linearity to compete with passives ones. 25 dBm RX IIP3 brings the balancing accuracy required for blocker compatibility to around 45 dB. This drastically simplifies hybrid balancing and adaptation loop accuracy potentially paving the way to DLT into real cell phones.

ACKNOWLEDGEMENT

The authors acknowledge Marvell Technology Group for support in chip fabrication and useful discussion.

REFERENCES

- [1] M. Mikhemar, H. Darabi, and A. Abidi, "A Multiband RF Antenna Duplexer on CMOS: Design and Performance," *IEEE J. of Solid-State Circuits*, vol. 48, no. 9, pp. 2067- 2077, Sept. 2013
- [2] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, "Tunable CMOS Integrated Duplexer with Antenna Impedance Tracking and High Isolation in the Transmit and Receive Bands," in *IEEE Trans. on MTT*, pp. 2092–2104, Sep 2014.
- [3] Elkholy, M.; Mikhemar, M.; Darabi, H.; Entesari, K., "A 1.6–2.2GHz 23dBm low loss integrated CMOS duplexer", *Proc. of the 2014 IEEE CICC*, pp.1,4 15-17 Sept. 2014
- [4] H. Darabi, A. Mirzaei, and M. Mikhemar, "Highly Integrated and Tunable RF Front Ends for Reconfigurable Multiband Transceivers: A Tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.58, no.9, pp.2038,2050, Sept. 2011.
- [5] Fabiano, I.; Sosio, M.; Liscidini, A.; Castello, R., "SAW-Less Analog Front-End Receivers for TDD and FDD," *Solid-State Circuits, IEEE Journal of*, vol.48, no.12, pp.3067,3079, Dec. 2013
- [6] B. van Liempd, et al., "A 70dBm IIP3 Single-Ended Electrical-Balance Duplexer in 0.18 μm SOI CMOS", *Proc. of IEEE ISSCC 2015*, pp 32-33, Feb 2015