Novel shallow trench isolation process
using flowable oxide CVD for sub-100nm DRAM

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ABSTRACT

We have investigated the characteristics of cell leakage and data retention time when using flowable oxide chemical vapor deposition (CVD) as a shallow trench isolation (STI) process of 1-Gbit DRAM. The trench gap filling capability was increased dramatically by combining high-density plasma (HDP) CVD with flowable oxide CVD. The reduced local stress by flowable oxide in narrow trenches leaded to decrease in junction leakage and gate induced drain leakage (GIDL) current and increase in data retention time of DRAM compared to HDP STI. Therefore, it is concluded that the combination of flowable oxide and HDP oxide is the most promising technology for STI gap filling process of sub-100nm DRAM technology.

INTRODUCTION

Rapid miniaturization of dynamic random access memory (DRAM) raises problems of shallow trench isolation (STI) gap filling process. Since the device performance is very sensitive to STI, the noble method for gap-fill needs to be developed for sub-100nm DRAM. High-density plasma (HDP) chemical vapor deposition (CVD) process has been mostly used as the STI gap filling process. Its gap filling capability is strongly dependent on trench depth, trench angle, and aspect ratio due

the redeposition behavior caused by sputtering. Figure 1 shows the range of isolation space currently available for gap filling by HDP CVD. This result indicates that the introduction of new gap filling method is required for the sub-100nm DRAM. As a solution, we propose the new process of combining thin flowable oxide CVD process with conventional STI process as shown in Fig. 2. Since the flowable oxide has the fluid characteristics similar to a spin-on-glass film at the moment of deposition, it shows excellent gap filling capability. However, the nano-pores generated in narrow trenches during densification annealing make flowable oxide to be susceptible to a severe cleaning condition. The dense HDP oxide over the flowable oxide can prevent the exposure of nano-pores to cleaning chemicals.

It has been known that junction leakage has a strong relationship with stress at the interface of Si and field oxide [1-3]. T. Kuroi et al. reported that crystal defects were generated by local stress and the stress increased with the reduction in the isolation pitch [4]. Therefore, the minimization of the local stress is one of the key solutions to suppress junction leakage at the sub-100nm technology. Fortunately, the flowable oxide exhibits less thermal mismatch with Si compared to HDP oxide. Therefore, it is expected that the local stress around field oxide can be released. In this paper, the effect of the addition of flowable oxide on the junction leakage and the data retention time was investigated.
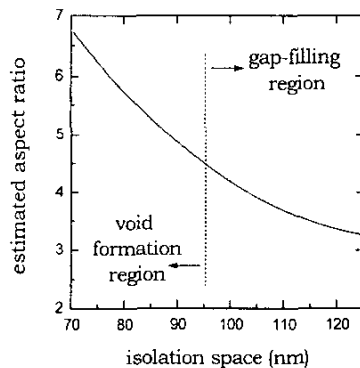

Fig. 1. The estimated aspect ratio with isolation space. The limitation of HDP CVD gap filling was regarded as aspect ratio of about 4.5 and isolation space of 95nm.
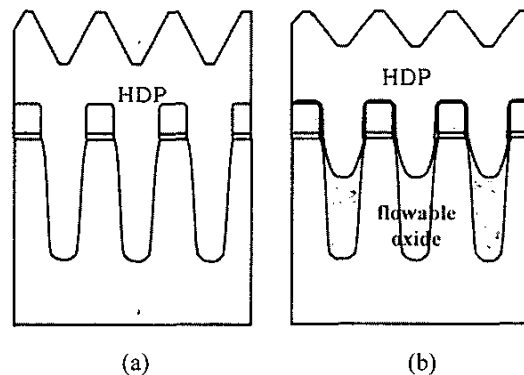
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Fig. 2. The schematic diagrams of (a) the conventional STI using HDP CVD and (b) the proposed STI using flowable oxide. In the case of the proposed STI process, the only flowable oxide process was added.

9.4.1

EXPERIMENTAL

The flowable oxide CVD process is the method depositing liquid $Si(OH)_4$ film like gel by supplying silane and hydrogen peroxide gases at the temperature of about $0\,^{\circ}C$. And the subsequent high temperature densification step is followed. Since deposited film has the behavior like liquid, the surface should be modified into the hydrophilic surface before deposition. The thermal expansion coefficient and the intrinsic stress of flowable oxide were obtained by measuring the stress hysteresis and the local stress near a trench was estimated through simulation using TSUPREM-4. DRAM cell array with 100nm-design rule was used for the evaluation of isolation characteristics with a flowable oxide layer and a thin nitride film. The 256-Mbits SDRAM with 130nm-design rule was also used to investigate the device performance such as hot carrier immunity, gate induced drain leakage and data retention time when flowable oxide CVD was applied.

RESULTS AND DISCUSSION

The deposition profile of flowable oxide depends on sizes and densities of patterns due to the surface tension of $Si(OH)_4$. Figure 3 shows the deposition profiles of flowable oxide through SEM photographs. Since the $Si(OH)_4$ has high surface energy, flowable oxide becomes thicker at the bottom of trench as the trench space decreases for the reduction of surface area. The surface tension attracted flowable oxide from the trench sidewall to the trench bottom. Therefore, flowable oxide layer remained very thin over the active area and at the sidewall of trench as shown in Fig. 3.

Moat depth was measured by SEM and TEM to judge whether the existence of very thin flowable oxide at the sidewall of trench made the moat deeper after chemical cleaning. Any chemical attack on flowable oxide layer at the trench sidewall could not be observed as shown in Fig. 4. Some voids were observed at the bottom of trenches in the flowable oxide STI. However, they were confirmed to be nano-pores exaggerated during preparation of TEM sample. Figure 5 shows the gate oxide integrity. There was no significant difference between flowable oxide STI and HDP STI.

Figure 6 shows the local stress related to flowable oxide thickness in narrow trenches. Stress simulation provided the estimated values of local stresses at the top and the bottom corners of trench. The local stress decreased with flowable oxide thickness. Even though they were calculated by using the thermal expansion coefficient obtained from the flat film, the flowable oxide layer was effective to reduce the local stress. Considering that the flowable oxide inside narrow gap is more porous, it was expected that the local stress could be more effectively suppressed in narrow trenches.

Figure 7 shows the p-n junction leakage measured with 256-kbit cell arrays of 100nm-scaled DRAM. The flowable oxide STI provided the improved junction leakage

(a)   Flowable   (b)
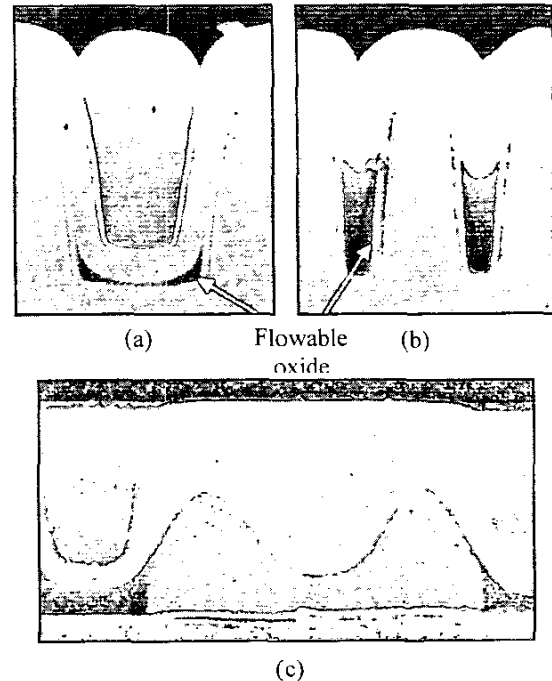   oxide

(c)

Fig. 3. SEM photographs of the deposition profiles of flowable oxide. Poly-crystal Si film was deposited over the flowable oxide. (a) narrow space with parallel to word line, (b) wide space with parallel to word line, (c) parallel to bit line.

characteristics compared to the conventional HDP STI. Considering that HDP STI with thin liner nitride was comparable with flowable oxide STI without thin liner nitride, the effect of stress relaxation originated from the use of the flowable oxide was similar to the application of liner nitride into HDP STI. By the insertion of thin nitride film into the flowable oxide STI, the additional reduction in junction leakage was obtained. Figure 8 shows the isolation punch-
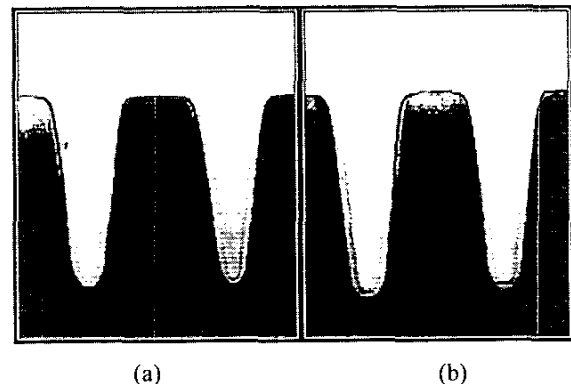

(a)   (b)

Fig. 4. TEM photographs of STI filled by (a) only HDP oxide and (b) the flowable oxide covered by HDP oxide. The samples were prepared after gate electrode deposition. The moat depths of two processes were similar.
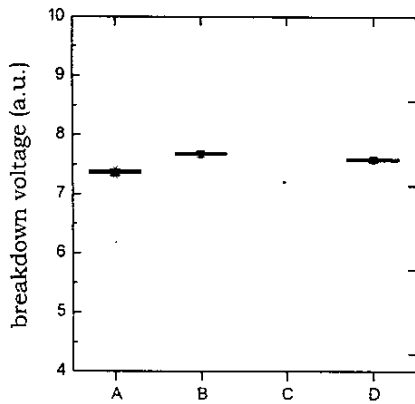
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Fig.5. Gate oxide breakdown voltage measured in the 256-kcell arrays. A and B: HDP, C, D and E: HDP/flowable oxide, A and C: without liner nitride, B and D: with liner nitride.
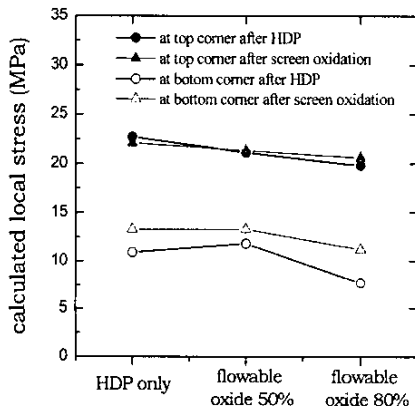

Fig. 6. The simulated local stress related to flowable oxide thickness in narrow trenches at the top and bottom trench corners.
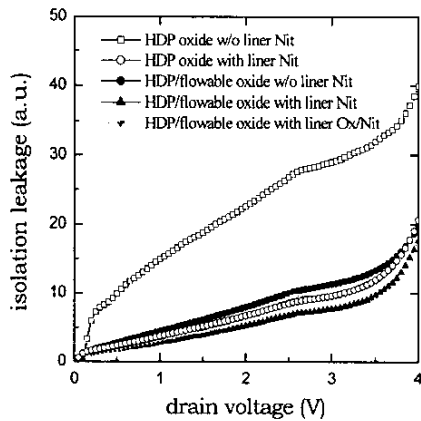

Fig. 7. The p-n junction leakage measured with 100nm-scaled 256-kbit cell arrays. The junction leakage through the flowable oxide STI was improved compared with the HDP STI.
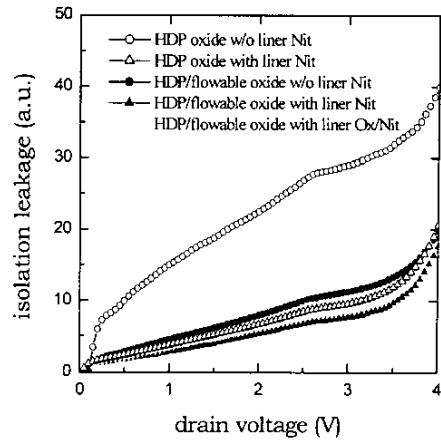

Fig. 8. The isolation punch-through leakage current measured with 100nm-scaled 256-kbit cell arrays. The junction leakage through the flowable oxide STI was improved compared with the HDP STI.

through leakage at 256-kbit cell arrays. The trend was similar to that of cell junction leakage. The junction leakage current of HDP STI could be reduced as much as 3 times by the introduction of flowable oxide layer or liner nitride. Therefore, it was evident that the generation of interface states near the trench could be suppressed by the buffer layer such as flowable oxide and thin nitride films.

The reliability of 130nm-scaled 256Mbit DRAM using flowable oxide STI was examined. In this study, thin nitride liner was used in both of HDP STI and flowable oxide STI. Figure 9 shows the cell junction leakage at 80-kbit cell arrays. The leakage current in flowable oxide STI was less than that of HDP STI. A little reduction in junction leakage current was obtained. This result was coincident with the result shown in Fig. 7. Figure 10 shows the gate induced drain leakage (GIDL) current, which is generally known as the major source of degradation of refresh characteristics of DRAM. Like the junction leakage data, the reduced GIDL current was obtained by using the flowable oxide. It is clear that the introduction of
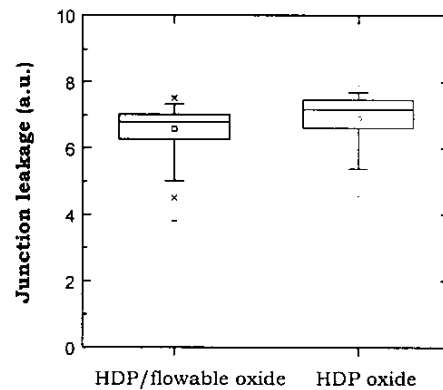

Fig. 9. The cell junction leakage current at 80-kbit cell arrays of 130nm-scaled DRAM. Vds was 2V and the gate was floated.
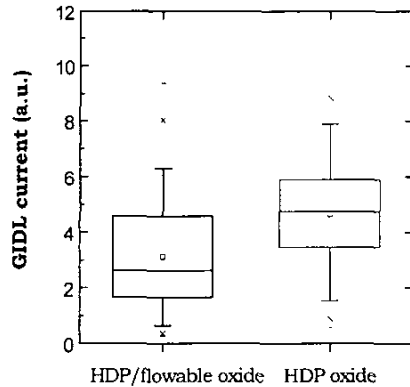
9.4.3

Fig.10. The cell GIDL current at 80-kbit cell arrays with 130nm-scaled DRAM. Vds is 6V. The gate voltage is 0V.
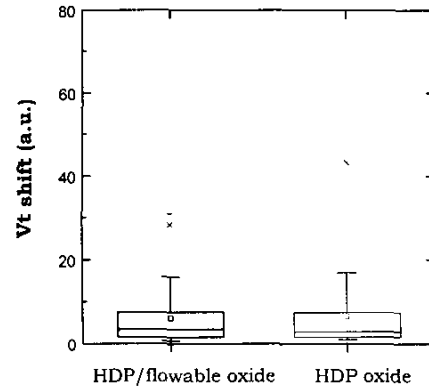

Fig. 12. The hot carrier immunity of cell transistors expressed by the change of threshold voltage after high voltage stress.

flowable oxide CVD into STI process contributes to the reduction of junction leakage of cell transistor. And the improvement of leakage performance would be resulted from buffering of local stress.

Figure 11 shows the refresh characteristics of 256-Mbits DRAM. The data retention time is exhibited at $10^{-4}\%$ cumulative failure. The data retention time of DRAM cells using flowable oxide as gap-fill materials was improved by about 10% compared with conventional HDP while there were no differences in cell capacitance and threshold voltage of cell transistor. Based on these results, we concluded that there is considerable stress relaxation effect of flowable oxide process on the reduction in the cell junction leakage and GIDL current. And it leaded to the improvement of refresh performance.

Figure 12 shows the hot carrier immunity of cell transistors expressed by the change of threshold voltage after high voltage stress, which is a reliability item. Any detrimental effect on the hot carrier immunity was not induced by the addition of

flowable oxide into conventional STI process.

CONCLUSIONS

The new STI process using the combination of flowable oxide CVD and HDP CVD was successfully developed for sub-100nm DRAM technology. The gap filling capability was startlingly improved and it could be very easily obtained even though the only flowable oxide CVD was added into conventional process with HDP CVD. Moreover, its low thermal mismatch from Si resulted in the improvement of the device performance such as junction leakage and data retention time. Therefore, this process was believed to be the most promising candidate for the isolation process of sub-100nm technology.

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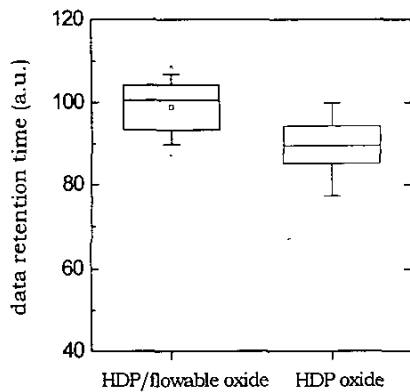
Fig. 11. The retention time of 256-Mbits DRAM at $10^{-4}\%$ cumulative failure.