# A 550-1050MHz +30dBm Class-E Power Amplifier in 65nm CMOS

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***Abstract*— A 65nm CMOS broadband two-stage class-E power amplifier (PA) using high voltage extended-drain devices is presented. To reduce the peak drain-source voltage and improve reliable operation, sub-optimum class-E operation is applied. The PA is followed by a broadband output matching network implemented as an off-chip two-stage LC ladder. The measurements with a 5.0V supply voltage for the power stage and 2.4V for the driver stage show a drain efficiency $> 67\%$ and a power-added efficiency (PAE) $> 52\%$ with a $P_{out} > 30$dBm within 550MHz-1050MHz. The output power variation is within 1.0dB and efficiency variation is less than 13%. The highest efficiency is observed at 700MHz with peak drain efficiency of 77% and peak PAE of 65% at a $P_{out}$ of 31dBm and 17dB power gain. By using dynamic supply modulation, the PA achieves a PAE of 40% and a drain efficiency of 60% at 10dB power back-off from 30dBm.**

***Index Terms*— Broadband, class-E, CMOS power amplifier**

## I. Introduction

The coexistence of various wireless communication standards requires that the user terminals can cover multi-standard operations. It is desirable for a single module to operate at multi-band frequencies, e.g., from 860MHz to 960MHz for GSM/CDMA850, GSM900, and UMTS900. This new feature puts major challenges on the RF power amplifier (PA) design. A PA operating over a broad frequency range with high efficiency, high linearity, and a flat output power is an ideal candidate for these systems. In advanced linear transmitters using nonlinear PAs, the switch-mode class-E PAs are often used as main amplification device due to their good efficiency performance and well-developed design methodology [1]-[2]. In addition, a watt-level PA in deep submicron CMOS is the most preferable candidate for low cost mobile terminals. However, the implementation of CMOS RF PAs in a standard CMOS technology is a challenging task due to the associated low breakdown voltage. In recent years, devices with high breakdown voltage such as extended-drain MOS and thick-oxide MOS have gained interest [3]. Such devices can withstand a higher drain-source voltage, hence delivering more output power in a reliable manner.

In the last few years, various broadband class-E PAs have been designed. Some PAs are designed to cover a wide frequency range (of more than 40%) [4]-[5], however, their related efficiency and output power are not flat over the frequency band of interest. Other PAs demonstrated a relatively flat efficiency and output power, but only for bandwidths below 20% [6]. Therefore, the design of a PA with high efficiency and flat output power across a broad frequency range is still a challenging task.

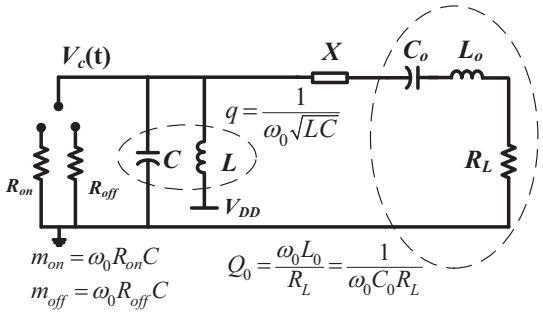


Fig. 1. Analytical model of class-E PA.

In this paper, a possible PA solution is proposed using a broadband class-E topology. Section II introduces a theoretical analysis of sub-optimum class-E operation. Section III gives the design of the high voltage CMOS die and an identification of its optimum class-E load impedances. In section IV, a broadband output matching network is developed. Section V shows the overall circuit implementation and measurement results. Section VI concludes the design.

## II. Analysis of Class-$E_{VV}$ Power Amplifier

Since Sokal [1] published a high-efficiency class-E switch-mode tuned PA, many analytical studies of this circuit have appeared. Recently an analytical modeling method for class-E PAs has been presented [2]. This method provides a set of design equations that make it possible to design a class-E PA by only specifying the supply voltage $V_{DD}$, frequency $\omega_0$, the device parameters $m_{on}$ and $m_{off}$[1] and the output power of the PA. Fig. 1 shows the analytical circuit model, in which the active device is replaced by a switch. The switch resistances $R_{on}$ and $R_{off}$, dc-feed inductance $L$, loaded quality factor $Q_0$, and operation mode are all taken into account as part of the class-E PA design procedure.

In the proposed design, the sub-optimum class-E operation, i.e., non-zero switching voltage and zero switching slope (known as Variable Voltage Class-E, class-$E_{VV}$ [2]) is chosen

[1] $m_{on} = \omega R_{on} C$, $m_{off} = \omega R_{off} C$

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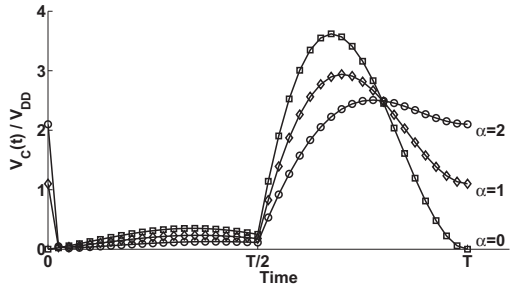



Fig. 2. Normalized switch voltage for different values of $\alpha$ representing class-E$_{VV}$ operation.

to reduce the peak switch voltage as to protect the active device. For class-E$_{VV}$ operation, the switch voltage $V_C(t)$ must satisfy the following two conditions:

$$V_C(t)|_{t=T} = \alpha V_{DD} \quad (1)$$

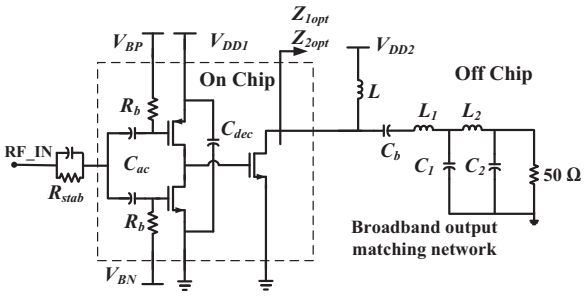
$$\left.\frac{dV_C(t)}{dt}\right|_{t=T} = 0 \quad (2)$$

where $\alpha V_{DD}$ is the voltage of $V_C(t)$ at the moment switch is closed ($t = T = 1/f_0$). The peak switch voltage $V_C$(t) can decrease from 3.6V$_{DD}$ to 2.5V$_{DD}$ when $\alpha$ increases from 0 (ideal class-E operation) to 2 for a certain non-ideal switch ON-resistance (see Fig. 2). This indicates that class-E$_{VV}$ operation can have lower peak switch voltage which allows the PAs to use a higher supply voltage to deliver more output power at the cost of a slight decrease in efficiency.

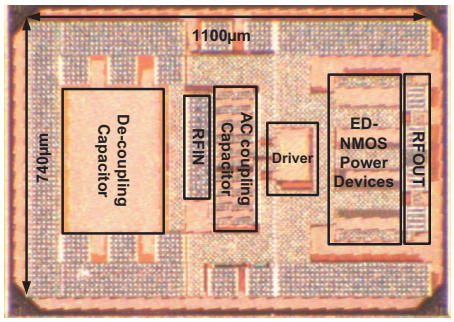
## III. ED-NMOS Device and Optimum Loads Design

Fig. 3 shows the overall schematic of the broadband class-E PA design and the realized high voltage CMOS PA die. The power output stage is formed by a dedicated high voltage, extended-drain, thick-oxide device (ED-NMOS) implemented in a standard 65nm CMOS technology without extra masks or processing steps [3]. The ED-NMOS transistor has an OFF-state breakdown voltage (BV$_{DS}$) of 15V. The measured $f_A$ exceeds 13GHz. The high breakdown voltage of the device enables the use of a higher supply voltage in class-E, which for a given output power yields higher load impedance. This relaxes the requirements on the impedance transformation and broadband output matching network. The total gate width of the used ED-NMOS transistor is 3.84mm and the channel length is 0.28$\mu$m realizing an ON-resistance $R_{on}$ of 0.7$\Omega$, an OFF-resistance of $R_{off}$ of 10$k\Omega$, and a total OFF-state output capacitance $C$ of approximately 4.14pF. To drive the output stage as a switch, a square-wave signal is generated by an inverter-based driver implemented using standard thick-oxide MOS devices with a gate length of 0.28$\mu$m. The inverter can deliver a 2.4 $V_{pp}$ square-wave to the ED-NMOS transistor when $V_{BP} = V_{BN} = 1.1V$ and $V_{DD1} = 2.4V$.

To apply the analytical design approach of [2], technology parameters ($m_{on}$ and $m_{off}$), supply voltage, operation frequency, and desired output power have to be specified first.




(a)



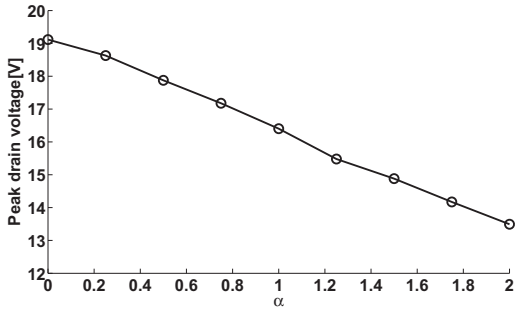

(b)

Fig. 3. Broadband class-E PA: (a) simplified schematic; (b) microphotograph of the realized high voltage CMOS PA die.

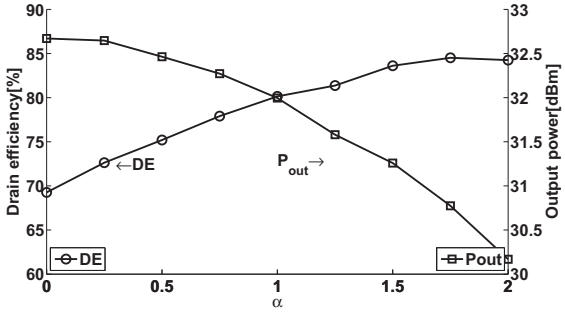
For this design, the target output power of the PA is +30dBm at 1GHz with 5.0V supply voltage. Based on the parameters ($R_{on}$, $R_{off}$ and $C$) of the intended output transistor stage, the technology related parameters can be calculated as $m_{on} = 0.02$ and $m_{off} = 260$. Substituting these parameters together with the other design targets ($m_{on}$, $m_{off}$, $V_{DD}$, $\omega_0$, $P_{out}$) into the analytical design equations of [2], a design set $K$ can be obtained[2], which enables us to calculate the values of the class-E circuit elements. Fig. 4 shows the related peak drain-source voltage $V_{ds}$, the drain efficiency, and output power as a function of parameter $\alpha$. It shows that the peak $V_{ds}$ decreases as $\alpha$ increases. When $\alpha > 1.5$, the peak $V_{ds}$ is less than ED-NMOS BV$_{DS}$. As can be concluded from Fig. 2, the voltage across the switch is the highest for $\alpha = 0$, which would result in higher switch losses and a lower efficiency. As remarkable consequence, the highest drain efficiency is not obtained at $\alpha = 0$ (traditional class-E operation). In fact, the drain efficiency increases as $\alpha$ increases, while the output power decreases with $\alpha$ (Fig. 4(b)). Accounting for an optimal combination of output power, drain efficiency, and peak drain voltage, $\alpha = 1.5$ is chosen for this design. The corresponding optimum PA load impedances[3] at the fundamental ($Z_{1opt}$) and second harmonic frequency ($Z_{2opt}$) are

[2] $K_L = \frac{\omega L}{R}$, $K_C = \omega CR$, $K_P = \frac{P_{out}R}{V_{DD}}$, $K_X = X/R$

[3] The optimum load impedances include the output capacitance of device $C_{ds}$, dc-feed inductance $L$, output matching network, and 50$\Omega$ load.




(a)




(b)

Fig. 4. Effects of variable-voltage parameter $\alpha$ on: (a) peak drain voltage; (b) drain efficiency and output power.

$$Z_{1opt} = 15.3\angle 20.8 \quad (3)$$

$$Z_{2opt} = 24.1\angle -90. \quad (4)$$

TABLE I
LUMPED ELEMENT VALUES FOR OUTPUT LOAD NETWORK

| $L$ | $L_1$ | $C_1$ | $L_2$ | $C_2$ |
|---|---|---|---|---|
| 12nH | 3.3nH | 6.8pF | 7.5nH | 2.2pF |

## IV. Broadband Output Matching Network

An ideal output matching network should provide the optimum load impedances across the frequency band of interest. The schematic of the used output matching network is also shown in Fig. 3(a). The two-stage LC ladder can easily provide a relatively flat broadband fundamental impedance and second harmonic impedance. The components values were optimized using ADS. The optimization strategy was to set a higher weight on the fundamental magnitude to obtain flat output power, rather than on the fundamental phase to get high efficiency. The reason for this is that the efficiency only drops 5% when the fundamental phase varies from 0° to 20°. In addition, the shunt capacitors were tuned deliberately to give the required second harmonic capacitive loading. Table I shows the element values of the synthesized matching network. Fig. 5 presents the synthesized fundamental load impedance.

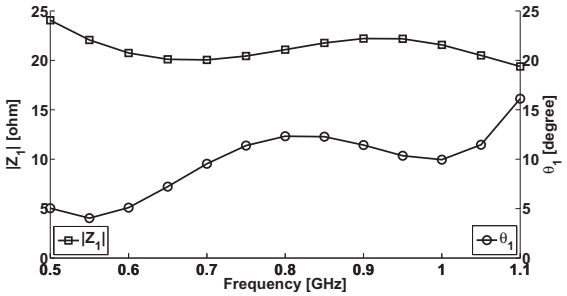



Fig. 5. Synthesized fundamental impedance.

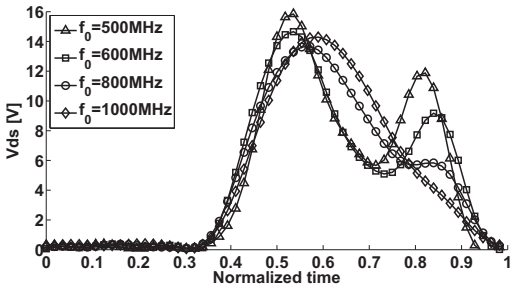



Fig. 6. Simulated drain-source voltage waveforms.

The magnitude $|Z_1|$ is larger than the previously found value of 15.3, which will reduce slightly the output power. The variation in magnitude from 600MHz to 1000MHz is about 10%. The fundamental phase $\theta_1$ is between 5° and 12°. Fig. 6 shows the simulated drain-source voltage $V_{ds}$ waveforms. At 500MHz, $V_{ds}$ significantly deviates from the standard class-E waveform resulting in a relatively lower efficiency. The peak $V_{ds}$ for the frequencies above 500MHz are all below $BV_{DS} = 15V$ so that the device can operate reliably.

## V. Implementation and Experimental Results

Fig. 7 shows the photograph of the implemented broadband PA. The PCB size is 35×25 mm$^2$. The CMOS chip is mounted on a Rogers substrate with $\epsilon_r = 3.5$ and a thickness of 0.203mm. The bond wires were kept as short as possible to limit their influence on the desired load impedances. High quality SMD inductors and capacitors were used to implement the output matching network. The power stage is biased at $V_{DD2} = 5.0V$ and the driver stage is biased at $V_{DD1} = 2.4V$ with $V_{BP} = V_{BN} = 1.1V$. Fig. 8 shows the measured and simulated output power, power gain, drain efficiency, and PAE against frequency from 500MHz to 1100MHz at RF input power of +14dBm. Close agreement is achieved between the simulated and measured results. Measured output power indicates a flat characteristic associated with broadband design from 550MHz to 1050MHz, at a value of 30.5±0.5dBm. A power gain between 16-17dB has been observed over the same frequency band. The drain efficiency and PAE remain above 67% and 52% across the same bandwidth. The peak drain efficiency of 77% and peak PAE of 65% are measured at

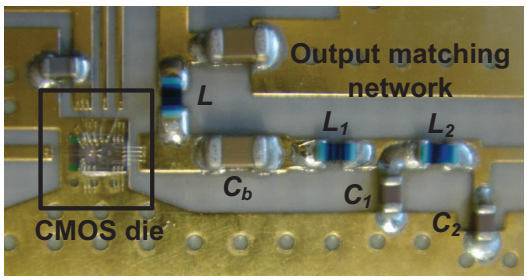



Fig. 7. Photograph of the broadband class-E PA.

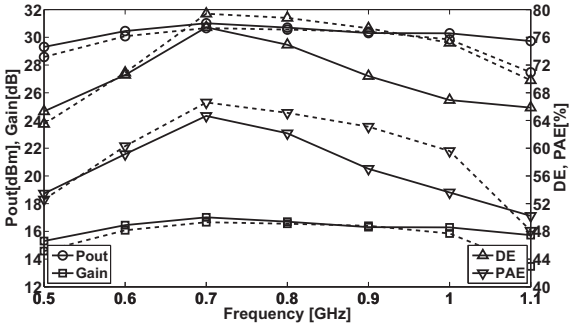



Fig. 8. Measured (solid lines) and simulated (dashed lines) output power, power gain, drain efficiency, PAE versus frequency ($V_{DD2} = 5.0V$, $V_{DD1} = 2.4V$, $V_{BN} = V_{BP} = 1.1V$, and $P_{in} = +14dBm$).

700MHz with 31dBm output power. The variation in drain efficiency and PAE over a bandwidth of 500MHz is less than 13%. Therefore the measured bandwidth[4] for this CMOS class-E PA is about 62.5% with $P_{out} \geq 30dBm$, $\eta \geq 67\%$, and PAE $\geq$ 52%. Table II compares the results of this work with previously published broadband class-E PAs around 1.0GHz. Compared with others' works, this CMOS PA can deliver watt-level output power with relatively flat power and efficiency across a very broad frequency range.

For polar transmitter, the efficiency in power back-off is more important. To enable output power control of the class-E amplifier and to improve its PAE at power back-off, supply modulation is applied. Fig. 9 shows the drain efficiency and PAE as a function of output power for the varying supply voltages of the final and driver stages. It shows that the PA exhibits a 45% PAE and a 68% drain efficiency at 10dB power back-off from 30.2dBm at 900MHz.

## VI. Conclusion

A 65nm CMOS broadband class-E PA is presented. The variable-voltage class-E operation is applied to reduce the device stress and improve reliability. With a straightforward two-stage LC ladder output matching network a good broadband output power performance is achieved in the 550-1050MHz band, with an output power larger than 30dBm and less than

[4]Bandwidth: the frequency range for which the variation in the output power is less than 1.0dB.

TABLE II
Comparison broadband Class-E PAs

| | 2006[4] | 2007[6] | 2009[5] | This work |
|---|---|---|---|---|
| BW [GHz] | 0.5-1.2 | 0.8-0.94 | 0.6-1.0 | 0.55-1.05 |
| $P_O$ [dBm] | $> 17.2$ | $> 31$ | $> 45.2$ | $> 30$ |
| $\Delta P_O$ [dB] | $< 3.0$ | $< 0.5$ | $< 1.7$ | $< 1.0$ |
| Gain [dB] | $> 7.2$ | $> 30$ | $> 10$ | $> 16$ |
| DE [%] | N.A. | N.A. | $> 66$ | $> 67$ |
| PAE [%] | $> 50$ | $> 55$ | $> 62$ | $> 52$ |
| $\text{PAE}_{PK}$ [%] | 70 | 62 | 80.6 | 65 |
| Technology | SiGe | 0.18$\mu$m CMOS | GaN | 65nm CMOS |
| Topology | Single-stage | Two-stage | Single-stage | Two-stage |

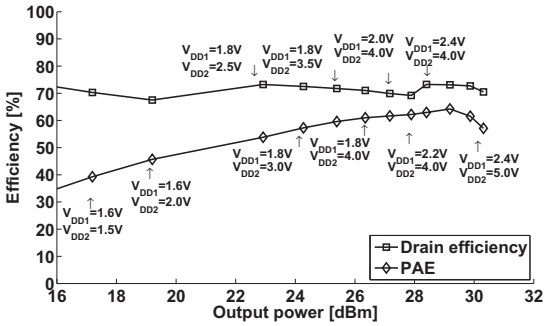



Fig. 9. Measured drain efficiency and PAE with optimum supplies of power stage and driver stage at 900MHz with $P_{in} = +14dBm$.

1dB variation. The drain efficiency is between 67% and 77% and PAE is between 52% and 65% over the same bandwidth. Using dynamic supply, more than 40% PAE and 60% drain efficiency can be achieved at 10dB power back-off.

## Acknowledgement

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## References

[1] N. Sokal and A. Sokal, "Class E - a new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, Jun. 1975.

[2] M. Acar, A. Annema, and B. Nauta, "Variable-Voltage Class-E Power Amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 1095–1098.

[3] J. Sonsky, A. Heringa, J. Perez-Gonzalez, J. Benson, P. Chiang, S. Bardy, and I. Volokhine, "Innovative high voltage transistors for complex HV/RF SoCs in baseline CMOS," in *VLSI Technology, Systems and Applications, 2008. VLSI-TSA 2008. International Symposium on*, 2008, pp. 115 –116.

[4] D. Lie, J. Popp, P. Lee, A. Yang, J. Rowland, F. Wang, and D. Kimball, "Monolithic class E SiGe power amplifier design with wideband high-efficiency and linearity," in *IEEE Int. Symp. VLSI-DAT*, Apr. 2006, pp. 1–4.

[5] A. Al Tanany, A. Sayed, and G. Boeck, "Broadband GaN switch mode class E power amplifier for UHF applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 7-12 2009, pp. 761–764.

[6] J. Jang, C. Park, H. Kim, and S. Hong, "A CMOS RF power amplifier using an off-chip transmision line transformer with 62% PAE," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 5, pp. 385 –387, May 2007.