SP 23.3: An I/Q Active Balanced Harmonic Mixer with IM2 Cancelers and a 45° Phase Shifter

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Two serious issues must be overcome for direct-conversion receivers and/or low-IF receivers to be used to realize a single-chip receiver. One is dc offset created by self-mixing of local oscillator signal (LO signal) for direct conversion, and the other is 2nd order intermodulation (IM2) for both the receivers.

An active balanced harmonic mixer eliminates the dc offset change due to the self-mixing down to its noise level [1]. An even-harmonic type of harmonic mixer produces no 2nd order distortion in principle, as it has odd symmetric non-linearity. In practice, imperfection in circuit symmetry and imbalance in differential signal result in small 2nd order distortion that may be problematic in applications containing amplitude modulation component. These requirements for IM2 are specified by IIP2. For example, IIP2 of 34dBm should be achieved for the personal handy phone system (PHS) if direct downconverters are used.

Figure 1 shows an active harmonic mixer consisting of two emitter-coupled pairs. The RF signal is input to each pair in anti-phase, and output ports are cross-coupled. At the output port, desired downconverted signal is added in-phase. The LO and IM2 signals are canceled by the cross connection. For usual ac signal cancelation, amplitude balance and phase balance should be considered simultaneously. In this case, only amplitude balance control is necessary. This results in an IM2 cancelation available in a wide frequency range, because amplitude gain is designed to be flat in receiving frequency band.

Assuming that input signal is $a(t)\cos(2\pi f_c t+\theta(t))$, produced 2nd-order distortion terms are $a(t)^2(1+\cos(4\pi f_c t+2\theta(t)))/2$. The low frequency output $a(t)^2/2$ is a concern because it falls into desired signal frequency band. The equation shows that the RF phase mismatch does not affect the baseband components including IM2. This means that the phase of envelope signal, i.e, group delay, should be considered instead of phase delay in RF signals. In high-frequency circuit, group delay is small and is negligible at baseband. Phase balance control is not necessary for IM2 cancelation and only amplitude balance control is necessary.

In the active harmonic mixer, the output signal amplitude is proportional to its bias current and IM2 cancelation is easily adjusted by changing the bias current balance of the two emitter coupled pairs.

For I/Q demodulation with harmonic mixers, there are two ways of phase shifting. One is 90° RF signal phase shifting, and the other is 45° LO signal phase shifting, because LO frequency is half the RF-signal frequency. Considering on-chip implementation, a 45° phase shifter is used, because a phase shifter in the RF signal path can degrade SNR.

Figure 2 is the phase shifter circuit. It contains two RC-bridge circuits. It is similar to the well-known 90° phase shifter, but has different features. Unlike the low-pass/high-pass type bridge phase shifter, the I/Q output LO signals are the same magnitude at any frequency as the bridges have an all-pass characteristic. Bridge1 outputs a 90+22.5° shifted signal and bridge2 outputs 90-22.5° shifted signal at 950MHz. Figure 3 shows the principle of this phase shifter. The curves are frequency responses of two bridges, and phase difference between $V_{LO}I$ and $V_{LO}Q$. The curve of phase difference has a flat top at the center frequency. This means that element sensitivity is very low around the peak point. Assuming that resistances on a chip are 10% larger than nominal value, the curves of frequency response move 10% to the left. The curve of phase difference moves 10% to the left, too, but keeps the shape on log scale unchanged, and the phase difference at center frequency decreases only 0.2°. This principle can be applied to arbitrary-angle phase shifters.

Figure 4 shows a block diagram of the direct downconverter. A micrograph of the chip is shown in Figure 5 with two 3b DACs to offset the tail currents of the active balanced harmonic mixer for IM2 cancelation. There is a mistake in RF-amplifier design in the complete downconverter since the RF-amplifier stage is bypassed, and evaluated gain, noise, and distortion use a chip without the RF amplifier stage.

Figure 6 shows IM2 dependence on RF signal amplitude. After adjustment, IM2 curve moves under the dotted line that crosses fundamental signal line at 144dBμ(37dBm), about 10dB lower than before adjustment. The IM2 cancelation has a distinct notch within a 3b control range (8% of the bias current). Figure 7 shows IM2 dependence on RF-signal frequency. RF input signals are f_{RF}+600kHz and f_{RF}+650kHz. LO frequency is half of f_{RF}. IM2 changes slowly because gain and gain balance change slowly. In PHS band (1895-1918MHz), readjustment is not necessary.

The measured baseband output phase error is 3° when 1.9GHz RF signal is input. It corresponds to 1.5° at phase shifter output at 950MHz. The baseband phase error is less than 5° form 1.8GHz to 2.0GHz.

The summary of measured results is shown in Table 1.

An active I/Q harmonic mixer with IM2 cancelers and a 45° phase shifter for direct downconversion has two advantages. One is small self-mixing dc offset because of harmonic mixing, and the other is small and frequency insensitive IM2. The proposed 45° phase shifter has low element sensitivity. The measured 37dBm IIP2 and 3° phase error indicate that the integrated direct downconverter with harmonic mixers is applicable even for QPSK signals that have an amplitude modulation component.

Reference:

[1] Yamaji, T., H. Tanimoto, "A 2GHz Balanced Harmonic Mixer for Direct-Conversion Receivers," Proc. of IEEE Custom IC Conf. pp.9.5.1—9.5.4, May, 1997.

Supply voltage	2.7V
Current consumption	68mA
Conversion	27dB
Noise figure	14dB
IIP3	-4dBm
IIP2	≥37dBm
Phase error	3°
Gain mismatch	0.1dB

Table1: Summary of measured results.

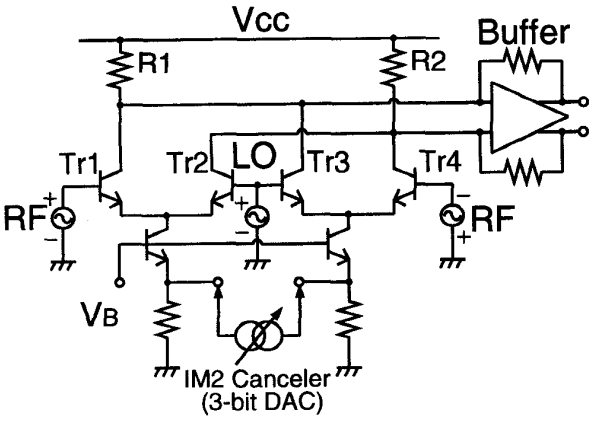

Figure 1: An active harmonic mixer with IM2 canceler.

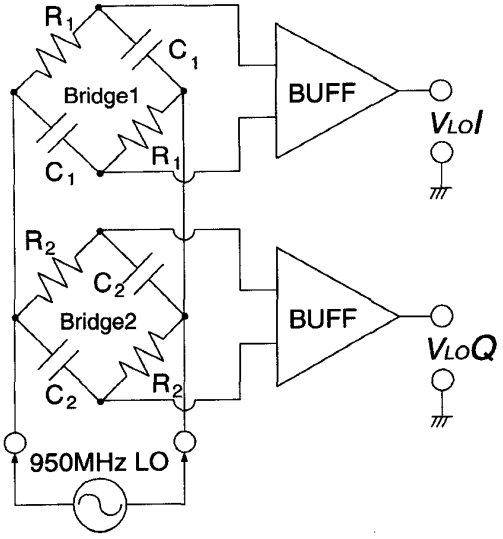

Figure 2: 45° phase shifter.

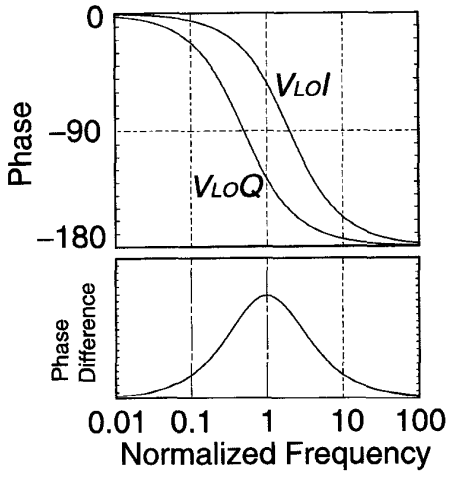

Figure 3: Phase shifter principle.

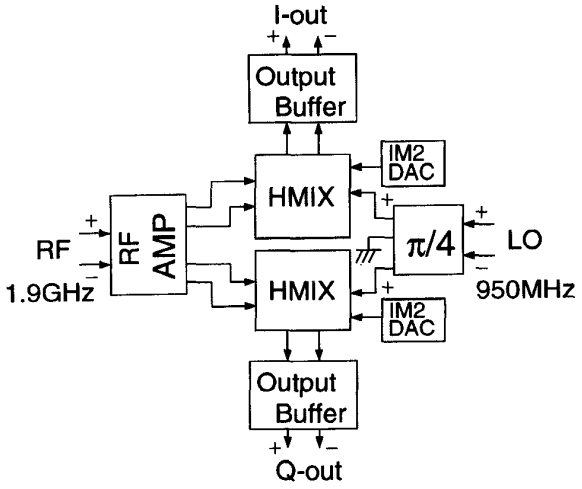

Figure 4: Direct downconverter block diagram.

Figure 5: See page 466.

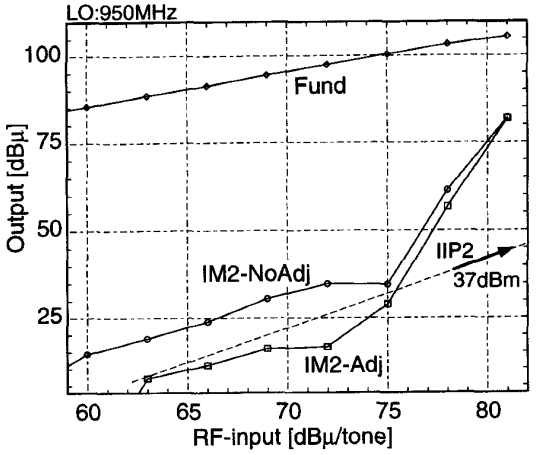

Figure 6: IM2 characteristic.

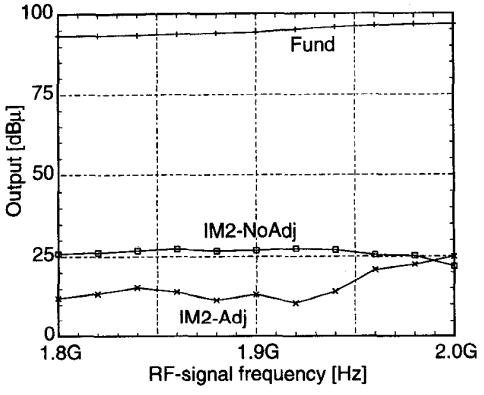

Figure 7: IM2 dependence on RF-signal frequency.

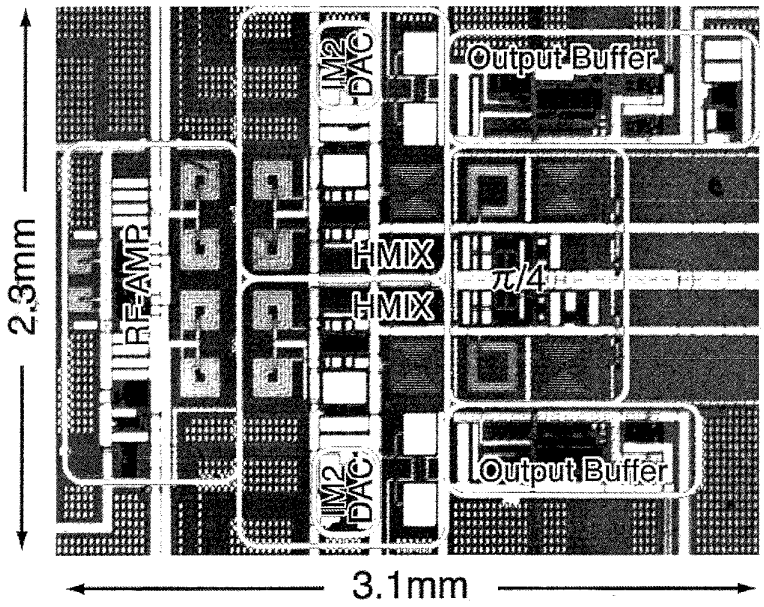

Figure 5: Die micrograph.

SP 23.5:A Fully Integrated CMOS DCS-1800 Frequency Synthesizer

(Continued from page 373)

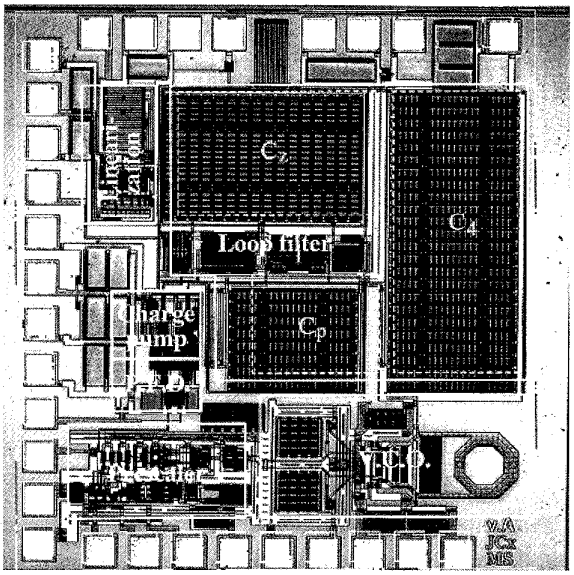

Figure 4: Die photograph with floorplan.

References:

[1] Craninckx, J., M. Steyaert, "A 1.8-GHz Low-Phase Noise CMOS VCO Using Optimized Hollow Inductors," IEEE Journal of Solid-State Circuits, vol. 32, no. 4, pp. 736-744, May, 1997.

[2] Craninckx, J., M. Steyaert, "A Fully Integrated Spiral-LC CMOS VCO Set with Prescaler for GSM and DCS-1800 Systems," Proc. Custom Integrated Circuits Conference, pp. 403-406, May, 1997.

[3] Craninckx, J., M. Steyaert, "A 1.75-GHz/3-V Dual Modulus Divide-by-128/129 Prescaler in 0.7mm CMOS," IEEE Journal of Solid-State Circuits, vol. 31, no. 7, pp. 890-897, July, 1996.

[4] Riley, T., M. Copeland, T. Kwasniewski, "Delta-Sigma Modulation in Fractional-N Frequency Synthesis," IEEE Journal of Solid-State Circuits, vol. 28, no. 5, pp. 553-559, May, 1993.

[5] Ali, A., L. Tham, "A 900-MHz Frequency Synthesizer with Integrated LC Voltage-Controlled Oscillator," ISSCC Digest of Technical Papers, pp. 390-391, Feb., 1996.

[6] Mijuskovic, D., et al., "Cell Based Fully Integrated CMOS Frequency Synthesizers," IEEE Journal of Solid-State Circuits, vol. 29, no. 3, pp. 271-279, March, 1994.