A 68/36ppm/°C TC 32.768kHz-to-1MHz RC-based Oscillator with 72/6pJ Start-up Energy

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***Abstract*—This paper describes a 32.768kHz-to-1MHz RC-based oscillator (RCO) suitable for high- and low-duty-cycle sleep-mode timers in emerging sensor node applications. In contrast to crystal oscillators (XO) based frequency references which employ long and energy intensive restarts, the proposed RCO achieves a 1000X reduction in restarting time. Measurement shows that the implemented RCO achieves a temperature stability of 68.5ppm/°C @32.768kHz and 37.5ppm/°C @1MHz. A proposed autonomous digital scheme uses coarse and fine tuning to compensate for process and temperature variations. Measurements report an energy efficiency of 1.46nW/kHz@1MHz occupying an area of 0.055mm2 in a pure digital 180nm CMOS process node.**

I. Introduction

Emerging IoT sensor nodes demand low-power wake-up timers that perform system duty cycling so that, during long sleeping periods, the system power decreases. Systems usually employ a real-time counter (RTC) XO as an always-on (AON) frequency reference for the wake-up timers. Although off-chip XO offers superior frequency stability, area-constrained and battery-powered sensor nodes restrict the adoption to integrated oscillators. Eeach shutdown of a XO in low-duty-cycle applications is energy intensive, with an approximated consumption of 100mW over a 100ms start-up time [1].

Fig. 1 shows an RCO within the clock distribution of a current system-on-chip (SoC) for IoT sensor nodes. The RCO and an XO provide the low-frequency clocks for the AON domain. Based upon measurement results of start-up times, the proposed RCO architecture may replace the low-frequency XO as a wake-up timer in future applications. Periodic wake-ups enable the processor core to perform computation/communication operations at higher frequencies where even an RCO can be applied as a clock source. This work proposes the use of the same RCO as a clock source to trigger low-duty-cycle periodic events for data rates as low as 1Mb/s.

This low-power wide-band RCO reduces the start-up energy down to three scales lower than the required start-up energy in an XO. The measured RCO can operate at different frequencies ranging from 32.768kHz-to-1MHz, with sub-100ppm temperature coefficients. The proposed circuit has a power control loop with optimized Schmitt trigger inverters to reduce the dominant large DC-current associated with their slow input slope. A wide-band tuning scheme uses two resistor banks for fine and coarse adjustment, plus a capacitor bank to provide a coarser variation. A proposed self-calibration scheme enables the RCO operation over a temperature range from -20°C to 125°C with high temperature and voltage stability.

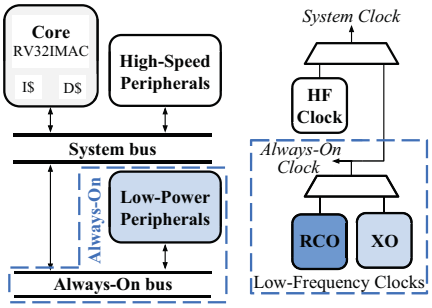

Fig. 1. RC relaxation oscillator as reference clock in an always-on domain.

II. Relaxation Oscillator Architecture and Circuit Implementation

A regular relaxation oscillator uses an error amplifier to generate a pulse that charges and discharges an RC bank [2], [3]. The oscillator frequency depends on the capacitor discharge through the resistance and the comparison time with a voltage reference made by an error amplifier. However, the amplifier is idle during most of the oscillator cycle and comparison operation requires a short time. Thus, the amplifier can be turned-off during most of the idle time and turned-on before the comparison time and, therefore, saving power during almost the whole period [2].

Fig. 2 shows the implemented oscillator with the states diagram of autonomous digital scheme. Most of the reported RCOs are limited to a specific operation frequency, and here we propose a wide-band oscillator operating from 32.768kHz-to-1MHz with reduced start-up time. A power down loop based Schmitt trigger (S_1) controls the on and off error amplifier(OP_1) cycle. In contrast to [2], we propose a fixed Schmitt trigger threshold and a dynamic tuning digital scheme that allows faster calibration time with reduced energy.

A. On the Limits of Power Consumption

There are two main circuits that consume most of the total current. The error amplifier (OP_1) and the Schmitt trigger (S_1) that controls the amplifier power-down signal. Due to the control over amplifier operation, the current consumption in

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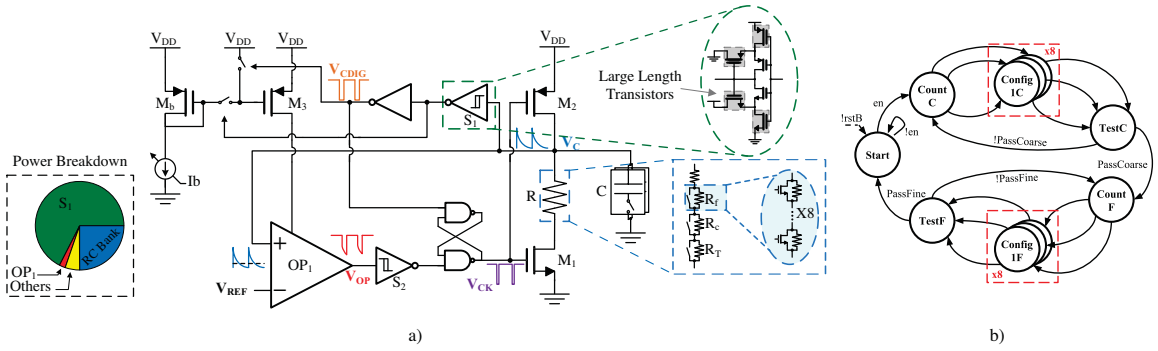

Fig. 2. a) Proposed relaxation oscillator architecture b) States diagram of the digital assisted compensation loop.

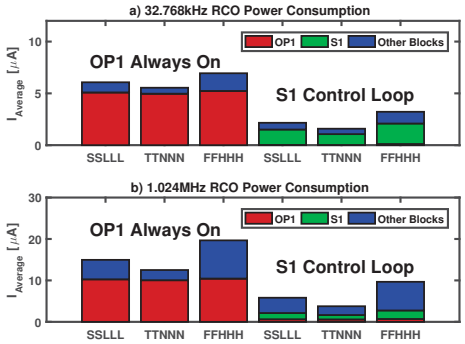

Fig. 3. a) Simulation results of power consumption for different blocks at 32.768kHz. b) Simulation results of power consumption of different blocks at 1MHz.

this circuit is less than 1μA over all process variations. Hence, the major part of the current corresponds to the Schmitt trigger where the slow slope of the RC discharge creates a large DC current.

Savanth et. al. [2] proposes an automatic control for the Schmitt trigger threshold with the aim to optimize the amplifier power consumption. The control requires to estimate the period of OP_1 operation and to adjust a variable Schmitt trigger threshold. They also use the estimations to adjust the frequency with pre-charged values of resistance tuning. In contrast, we optimize the Schmitt trigger performance, sizing it to reduce as much of the associated DC current. In addition, we design a fixed Schmitt trigger threshold for a robust performance over process, temperature and voltage (PVT) variations, ensuring the amplifier is always active for a precise comparison.

Fig. 3 shows a power break-down of the oscillator when OP_1 power control loop operates and when OP_1 is always working. Fig. 3a) and Fig. 3b) show the power break-down at 32.768kHz and 1MHz. For both operation frequencies, OP_1 experiments the higher power consumption when is always on. When the power control loop operates, the OP_1 power consumption is negligible compared to the Schmitt trigger and other blocks. In addition, the behavior is consistent for both operation frequencies and across PVT variations.

For a further power consumption optimization, the implemented amplifier has a bandwidth control feature. As Fig. 2a) shows, the digital word Ib varies the bias current turning-on and off some current mirrors. This digital trimming enables a current consumption of less than 1μA in low-frequency operation (kHz) but it also enables a higher frequency operation with reduced propagation delay when using the extra current bias.

B. RC Bank Tuning and Wide-Band Operation

RCO output frequency relies on the time constant $\tau = RC$. However, resistance and capacitance variations across process and temperature change the RC time constant –and so the output frequency–, also affecting the temperature stability. The proposed RC bank feature three types of tuning, including a temperature coefficient tuning.

Fig. 2a) shows the three resistance banks where R_f, R_c and R_T correspond to fine tuning, coarse tuning and temperature tuning . Two 8 thermometer buses adjust the coarse and fine tuning and an extra resistance control provides the temperature tuning. R_f and R_c banks are poly resistors and R_T are well resistors to help with temperature compensation. Temperature compensation is a major issue considering the resistance bank change over the frequency range. We address this issue by tuning the well resistor bank as well.

Considering that the implementation is performed in a pure digital process flavor, MiM-capacitors are not provided. We implement a C bank with NMOS capacitors occupying a lower area at the expense of increased sensitivity to process variations and leakage. In addition, a capacitance control enables a higher frequency range with only a coarse resistance step. Hence, two control bits provide different operation frequencies with a minimum value of 300fF for the MHz range.

Fig. 2b) shows the states diagram of the proposed FSM to auto-calibrate the RCO using the variable RC bank. Unlike Savanth et al. [2], we propose to calibrate for process and temperature variations counting over the whole cycle of the oscillator. In addition, the FSM uses a starved-inverter based oscillator as a reference to generate the count.

C. Supply Voltage Robustness

The discharge time must be constant to ensure an invariant frequency. If OP_1 compares with a constant reference under supply variations, the discharge time will change due to

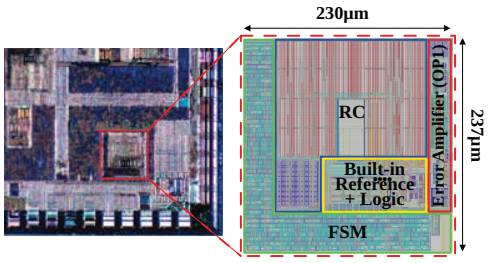

Fig. 4. Die micro-photograph and layout details of the proposed RCO.

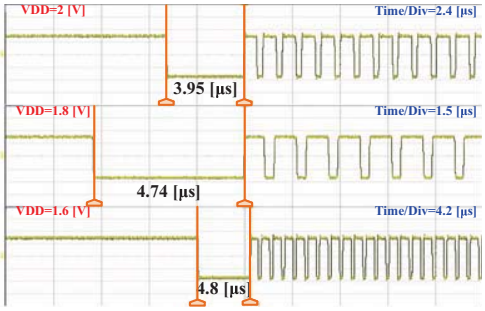

Fig. 5. Start-up time measurement at 1MHz for multiple supply voltages. Nominal start-up time shows a frecuency error of 0.36%.

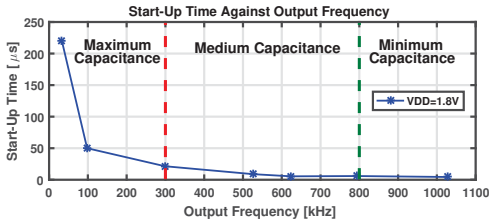

Fig. 6. Start-up time measurement for multiple output frequencies.

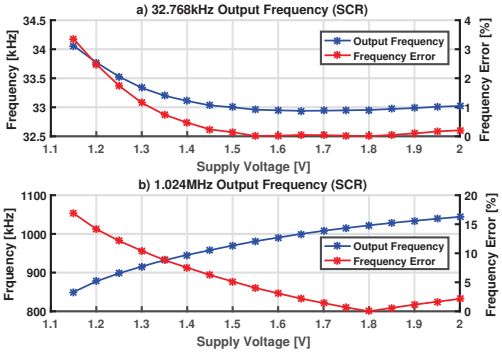

Fig. 7. a) 32.768kHz free-running frequency against supply voltage. b) 1MHz free-running frequency against supply voltage.

the comparison can occur after or before the expected time [2]. Thus, the ideal voltage reference should be invariant to temperature and process but not to supply variations.

We use a switched capacitor based reference (SCR) which emulates a resistor voltage divider [2]. The advantage is that an SCR has a better temperature coefficient, occupies less area and avoids any static current consumption. Moreover, we add a diode reference (DREF) and an external reference (Bandgap) as alternative options for debugging purposes.

III. Measurement Results

The RCO is implemented in a pure logic 180nm CMOS technology node. Fig. 4 shows the die micro-photograph and annotated layout of the proposed oscillator. Fig. 5 shows a characterization of the start-up time when voltage supply changes. Here, we define the start-up time as the required duration for the frequency to settle within $\pm 2\%$ from the target frequency. Although the definition may differ to applications requiring accurate timing, there would be a large number of applications where the settling time could be counted from the first period. The measured start-up times are $3.95\mu s$, $4.74\mu s$ and $4.8\mu s$ for 2V, 1.8V and 1.6V supply voltages respectively. We also measured the start-up time for a frequency of 32.768kHz vs voltage supply, resulting in $244\mu s$@1.6V, $220\mu s$@1.8V and 216μ@2V.

Start-up time measurements reveal a start-up energy of 72pJ@1.8V at 32.768kHz and 6pJ@1.8V at 1MHz. These results show a 1000X reduction in restarting time compared to traditional XO circuit. This feature enables low-power low-duty-cycle mid-frequency operations at data rates as low as 1Mb/s. Fig. 6 shows a characterization of the start-up time under different frequencies in the operating range. Fig. 6 depicts how start-up time depends on the RC time constant where the capacitance introduces a higher change due to its coarser variation. For clock frequencies over 600kHz, the start-up time exhibits a lower dependence.

A. Voltage Stability

Unlike Savanth in [2] that implemented variable threshold Schmitt trigger, we implement robust Schmitt trigger inverters which high-to-low threshold is always greater than reference voltage over PVT variations. Results or show similar voltage stability performance with reduced complexity. Fig. 7 shows the results for 32.768kHz and 1MHz varying the voltage supply from 1.1 to 2V. Fig 7a) shows the stability for 32.768kHz where frequency error is less than $\pm 1\%$ for supply voltages over 1.3V. For supply values less than 1.3V the SCR reference loses the proportionality, hence, increasing the frequency variation. Fig. 7b) shows a similar behavior for 1MHz but with higher variation due to the optimization of the threshold at 32.768kHz.

B. Temperature Stability

As expected, variations over temperature are larger than a mim-cap based RC bank since we based our implementation on a pure standard logic node. We measured oscillator performance from -20 to 125°C for 32.768kHz and 1MHz using SCR and DREF references. Fig. 8a) shows the performance at 32.768kHz at free running and after frequency tuning. The increased sensitivity to temperature mitigates with the tuning feature. Frequency error at high temperatures reduces after tuning, resulting in an average error less than 0.96%. As expected, DREF reference presents a higher sensitivity under temperature variations.

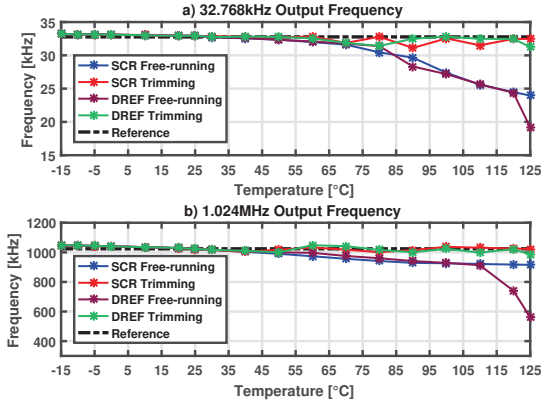

Fig. 8. a) Measured results for 32.768kHz over temperature. b) Measured results for 1MHz over temperature.

Fig.8b) shows the performance at 1MHz for SCR and DREF references. At 1MHz, operation with DREF reference at high temperature presents a stronger sensitivity than at 32.768kHz. Finally, the tuning feature can reduce high-temperature variations to less than 0.5% with SCR reference and 0.9% with DREF reference.

C. Performance Comparison

Table I shows a summary of measurement results and a comparison of the proposed oscillator to some state-of-the-art circuits. This work achieves 68.57ppm/°C in temperature stability with frequency tuning and 0.5% voltage stability without any adjustment at 32.768kHz. The energy efficiency $(Power/Freq)$ at 1MHz is 1.46nW/kHz, which is the second best after the reported by [2]. Energy efficiency is not well scaled with frequency due to the lower slope at the Schmitt trigger input, however, measurement results show an efficiency of 10.07nW/kHz at 32.768kHz.

Few papers in the literature report the start-up time of the RCO. This feature is important since a fast and energy efficient start-up enables low-energy duty-cycle applications by replacing the slower XO circuits. The conventional figure of merit (FOM) is not able to compare performance in terms of the start-up energy and settling time. Therefore, we include the start-up time complementing the original FOM as equation (1) shows. Using this new FOM, we obtain a performance of 2.1pJ/kHz @32.768kHz and 6pJ/kHz @1MHz, being the best-reported result considering the performance comparison of Table I. In addition, Fig. 9 shows a comparison in terms of the proposed FOM. This figure presents the trend for the best FOM that is achieved by the proposed work.

$$FOM = \frac{Power[W] \cdot Startup[s]}{Freq[Hz]} \quad (1)$$

IV. Conclusion

This paper demonstrates a wide-band RCO with a fast and energy efficient start-up. The oscillator includes a Schmitt trigger-based amplifier power control loop and a bandwidth control to optimize power consumption at different operation

TABLE I
Performance Summary and Comparison.

	[2]	[4]	[5]	[6]	[7]	This Work
Tech (nm)	65	180	65	180	180	180
Power(μW)	0.92* 12**	39.6	0.13	110	46.3	0.33$^+$@32.768kHz 1.5@$^+$1MHz
Freq(kHz)	1350	25000	18.5	70.4	82000	**32.768–1024**
Area (mm^2)	0.005	0.14	0.032	0.26	0.028	0.05
Start-up Time (μs)	10	15	216	2500	N.A.	**220@32.768kHz 4@1MHz**
Start-up Energy (pJ)	120**	594	28.1	275	N.A.	**72.64@32.768kHz 6@1MHz**
T. Range (°C)	0 to 150	-40 to 125	-40 to 90	-40 to 80	-20 to 100	-20 to 125
T. Coeff (ppm/°C)	96	1800	5500	34.3	123	68.57@32.768kHz 35.714@1MHz
V. Range	0.9 to 1.9	1.4 to 1.9	0.95 1.05	1.2 to 1.8	0.75 to 0.95	1.1 to 2
V.Stab (%ΔT/V)	0.49	0.2	5	0.75	0.91	0.5@32.768kHz 10.23@1MHz
FOM (nW/kHz)	0.68* 8.89**	1.584	7	7.8	5.6	**10.07$^+$@32.768kHz 1.46$^+$@1MHz**
Start-up FOM (pJ/kHz)	0.09**	0.023	1.512	19.5	N.A.	**2.21$^+$@32.768kHz 0.006$^+$@1MHz**

* Measured at 0.9V ** Measured at 1.4V $^+$ Measured at 1.1V

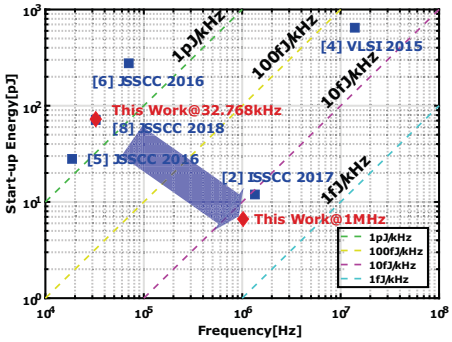

Fig. 9. Comparison chart for start-up energy for different state-of-the-art works [2], [4]–[6], [8].

frequencies. Measurement results show energy efficiencies of 10.07nW/kHz@33kHz and 1.46nW/kHz@1MHz. Results show a restarting time of 220μs@33kHz and 4μs@1MHz, which are 1000X less than the required time of XO circuits, only consuming 72pJ and 6pJ energy at start-up. The circuit was fabricated in a pure digital 180nm technology occupying an area of 0.055mm^2 and achieving a temperature stability of 68.5ppm/°C @32.768kHz and 37.5ppm/°C @1MHz with the autonomous digital scheme enabled. The measured start-up energies are the lowest reported breaking the energy efficiency barrier of 10fJ/kHz.

References

[1] M. Ding *et al.*, "A 0.7-V 0.43-pJ/cycle Wakeup Timer Based on a Bang-Bang Digital-Intensive Frequency-Locked-Loop for IoT Applications," *SSC-L 2018*, vol. 1, no. 2, pp. 30–33, Feb 2018.

[2] A. Savanth *et al.*, "A 0.68nW/kHz Supply-Independent Relaxation Oscillator With 0.49%/V and 96ppm/C Stability," in *ISSCC 2017*, Feb 2017.

[3] Ç. Gürleyük *et al.*, "A CMOS Dual-RC Frequency Reference With 250ppm Inaccuracy From -45C to 85C," in *ISSCC 2018*, Feb 2018.

[4] H. Abbasizadeh, B. S. Rikan, and K. Y. Lee, "A fully on-chip 25MHz PVT-compensation CMOS Relaxation Oscillator," *VLSI 2015*, vol. 2015-Octob, pp. 241–245, 2015.

[5] A. Paidimarri *et al.*, "An RC Oscillator With Comparator Offset Cancellation Arun," *JSSCC 2016*, vol. 51, no. 8, pp. 1866–1877, 2016.

[6] M. Choi *et al.*, "A 110 nW Resistive Frequency Locked On-Chip Oscillator with 34.3 ppm/C Temperature Stability for System-on-Chip Designs," *JSSCC 2016*, vol. 51, no. 9, pp. 2106–2118, 2016.

[7] Lu, Shao-Yung, Liao, Yu-Te, "A 46μW, 8.2MHz Self-threshold-tracking Differential Relaxation Oscillator with 7.66psrms Period Jitter and 1.56ppm Allan Deviation Floor," *CICC 2018*, pp. 3–6, 2018.

[8] J. Jung *et al.*, "A 1.08-nW/kHz 13.2-ppm/C Self-Biased Timer Using Temperature-Insensitive Resistive Current," *JSSCC 2018*, vol. 53, no. 8, pp. 2311–2318, 2018.