A Stacked 6.5-GHz 29.6-dBm Power Amplifier in Standard 65-nm CMOS

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***Abstract* – A stacked amplifier architecture has been used to achieve high RF output power levels in sub-100nm CMOS. The stacking makes it possible to both operate the power amplifier (PA) from a large supply voltage and implement RF power combining. As a proof of concept, a 6.5-GHz PA has been integrated in a 65-nm standard CMOS technology. The amplifier achieves 27.4-dBm output power with an efficiency of 19.2% at 6.5 GHz when driven from a 3.6-V supply voltage and 29.6-dBm output power with an efficiency of 20.3%, when driven from a 4.6-V supply voltage.**

I. Introduction

CMOS technology scaling has enabled the integration of RF transceivers on a single chip for various applications. However, as the feature sizes of the transistors scale, their breakdown voltages are reduced. Lower breakdown voltages lower the maximum voltage swings across the transistors and necessitate operation from a lower supply voltage. These factors, in turn, impose significant limitations on RF power amplifier (PA) design. The low voltage swing limits the maximum power that can be delivered to the load, and DC-DC converters are generally needed to provide a low supply voltage from typical battery voltages.

In order to overcome the limitation on output power imposed by the constrained voltage swings, some form of impedance transformation and/or power combining must be used. In recent years, increasing attention has been given to transformer-based on-chip power combining [1]–[3]. Fig. 1(a) shows the block diagram of n amplifier stages whose output voltages are summed at the secondary sides of the output transformers. For n stages, this architecture gives an impedance transformation ratio of n, and the output power delivered to the load is n times the output power of each amplifier stage.

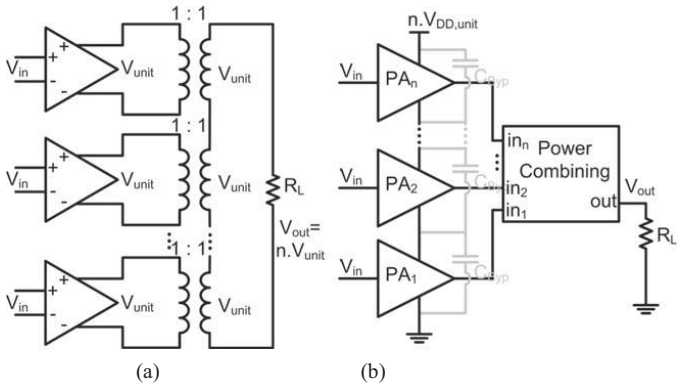

Fig. 1. (a) Transformer-based power combining, (b) DC-stacking of PAs.

When a DC-DC converter is used to provide a low supply voltage for PAs, the loss in the converter can contribute significantly to the overall system power consumption. To drive the PA directly from a large supply voltage and eliminate the need to a DC-DC converter, the PA stages can be stacked in DC [4], as shown in Fig. 1(b). If n stages are stacked in DC, the supply voltage of the amplifier can be n times the supply voltage that one stage can sustain.

This work proposes a stacked power amplifier architecture that can achieve high output power and operate from a large supply voltage without exceeding the transistor breakdown limitations.

II. Architecture

A. Transistor Stacking

This section introduces a PA architecture that combines transformer-based power combining and DC-stacking. For simplicity, the architecture is described in terms of single-ended amplifiers. However, the idea can be applied to differential amplifiers as well, as illustrated by the proof-of-concept design presented in Section III.

Fig. 2(a) shows an amplifier comprising a stack of three single-ended amplifier stages. Since the amplifier stages are stacked in DC, the supply voltage for the overall amplifier can be three times the supply voltage that each individual stage can accommodate. In this configuration, the output voltages of the amplifier stages are added at the secondary windings of the transformers, and their sum appears at the load.

If the arrangement of the transistors and transformers is reconfigured as shown in Fig. 2(b), the current through the transistors and the voltage across the primary coils of the transformers will stay the same, provided the influence of the parasitic capacitances from the drains of the transistors to ground is ignored. The effects of these parasitics are considered in Section II.D. Since both the primary and secondary sides of the transformers in Fig. 2(b) are connected in series, the transformers can be combined into a single transformer. Because the voltage swings are added at the drain of the topmost transistor in the stack, the transformer is not needed to sum the output voltages of the individual stages. Therefore, the transformer can be eliminated, and the load can be connected directly to the drain of the topmost transistor, as illustrated in Fig. 2(c). The architecture of Fig. 2(c) thus does not suffer from transformer loss.

B. Stacked-Transistor Amplifier

In the following analysis a "unit" amplifier is defined as a differential amplifier that consists of a differential pair of transistors with the supply voltage of $V_{DD,unit}$. The differential

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load impedance seen by the pair is defined as $R_{L,unit}$. The output power of a unit amplifier is

$$P_{unit} = k \cdot \frac{V_{DD,unit}^{\ 2}}{2R_{L,unit}}, \tag{1}$$

where k is a constant determined by the class of the amplifier.

A "stacked" amplifier is a differential amplifier that consists of n transistors connected in series on each side of the differential branch. $R_{L,stack}$ is the differential load impedance that the differential stack of n transistors sees. For the same voltage stress on the transistors, the supply voltage of the stacked amplifier, $V_{DD,stack}$ can be

$$V_{DD,stack} = n \cdot V_{DD,unit}. \tag{2}$$

Therefore, the stacked amplifier achieves the following output power:

$$P_{stack} = k \cdot \frac{n^2 \cdot V_{DD,unit}^{\ 2}}{2R_{L,stack}}. \tag{3}$$

If all of the transistors in the stacked amplifier have the same size as the unit amplifier transistors, then the overall on-resistance of the stacked amplifier is

$$r_{on,stack} = n \cdot r_{on,unit}, \tag{4}$$

where $r_{on,unit}$ is the on-resistance of unit amplifier. If the load impedance of the stacked amplifier is chosen to maintain the same ratio of load impedance to amplifier on-resistance as for the unit amplifier, then the stacked amplifier load is

$$R_{L,stack} = n \cdot R_{L,unit}. \tag{5}$$

Substituting (5) into (3) and comparing the result with (1) shows that a stacked amplifier with n transistors in the stack delivers n times the output power of a unit amplifier:

$$P_{stack} = n \cdot P_{unit}. \tag{6}$$

If all the transistors in the stacked amplifier are driven, the power required to drive the stacked amplifier will be n times that used to drive the unit amplifier. However, if only the bottom transistor of the stack is driven, the drive power required for both the stacked amplifier and the unit amplifier are same. In this case, the power gain, overall efficiency, and power-added efficiency (PAE) will be larger for the stacked amplifier than the unit amplifier.

C. Self-Biasing

Previously, some work has been done on self-biasing cascode transistors to avoid hot carrier effects [5] and self-biasing more than two transistors in linear-mode PAs [6]. In this work, we propose to stack three transistors in a differential RF PA that operates in class E/F_{odd} [7] mode.

The voltage waveforms at the terminals of the transistors should satisfy the following conditions:

(1) the maximum allowable swing across the drain-source of the transistors to provide the largest possible output power.

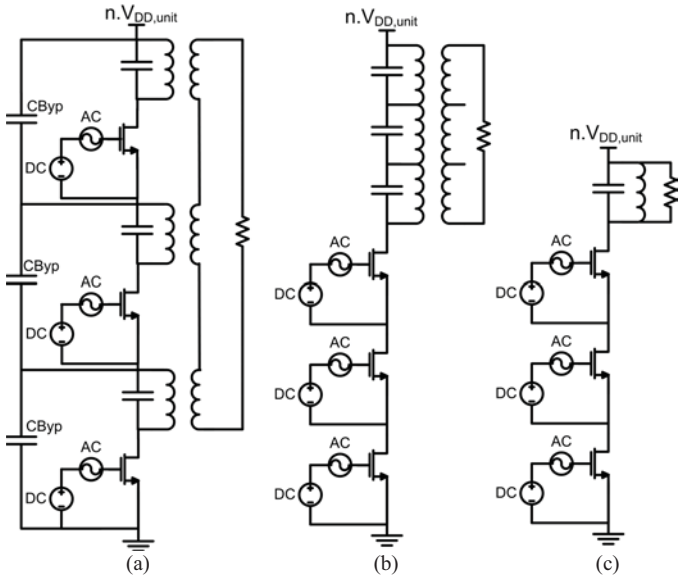

Fig. 2. (a) DC-Stacked PAs, (b) Reordering the transistors and transformers, (c) Stacked-transistor amplifier.

(2) during the ON half-cycle, the gate-source voltage of the transistors should be large enough so that their on-resistance is small.

(3) during the OFF half-cycle, the gate-source voltage of the transistors must be smaller than the threshold voltage.

(4) the gate dielectric voltage and the drain-bulk voltage of all transistors must be smaller than the corresponding breakdown voltages.

The architecture shown in Fig. 3, which shows only one side of the differential amplifier, is proposed to satisfy these conditions. Transistor M_2 is biased with a constant voltage, similar to a conventional cascode structure.

Capacitive coupling through C_{gs3} and C_{gd3} is used to provide the required voltage swing at the gate of transistor M_3. In order to adjust the voltage swing to the desired value, an appropriately sized capacitance C_g is connected from the gate of M_3 to ground. The DC voltage at the gate of M_3 is provided through a peak-detector from the drain of M_3, which consists of D_1, R_1, and C_1 in Fig. 3. Resistor R_2 provides a weak leakage path for the peak-detector.

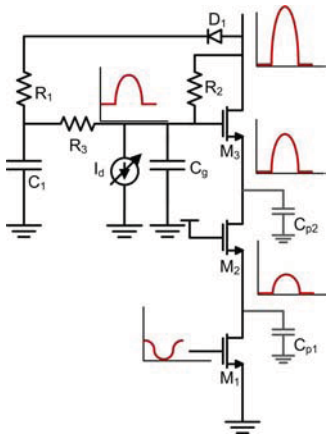

Fig. 3. Self-biasing of the three-transistor stack.

The DC voltage at the gate of M_3 is adjusted through control of the current I_d that passes through R_3. This adjustment makes it possible to satisfy the aforementioned conditions on the voltage waveforms across process and temperature variations.

D. Loss Mechanisms

There are two main loss mechanisms in transistors of a stacked amplifier [8]: (1) loss in the on-resistance of the transistors, and (2) loss in the transistors during charging and discharging of the intermediate drain nodes in the stack.

The capacitance at a drain node is the sum of the parasitic capacitances of the transistors connected to the node and the routing capacitance. Note that these capacitances between the intermediate stacking nodes and ground were ignored in the description of Fig. 2. In order to mitigate the loss mechanism associated with the parasitic capacitances at the intermediate drain nodes, these capacitances can be resonated out using inductors [8]. The next section, which describes the design of an experimental differential PA, discusses which parasitic capacitances should be tuned out using differential inductors.

III. Design

A. Stacked Differential Amplifier Topology

Fig. 4 shows the schematic of a stacked differential RF PA. As indicated in this figure, inverters are used to drive the bottom transistors, M_1, of the stack. On each side of the amplifier, the transistors M_1 are core (65-nm) devices, while the two upper transistors, M_2 and M_3, are thick-oxide I/O (0.25-μm) transistors. I/O devices are used for the two top transistors to increase the supply voltage and output power of the PA.

Since M_2 and M_3 are 0.25-μm devices, while M_1 is a core transistor, the parasitic capacitance at node *b* is larger than the parasitic capacitance at node *a*. Also, the swing at node *b* is larger than that at node *a*. The loss associated with charging and discharging the parasitic capacitance at node *b* is, therefore, significantly larger than the loss associated with charging and discharging the parasitic capacitance at node *a*. The inductor L_{d2} is used to reduce the loss associated with node *b*.

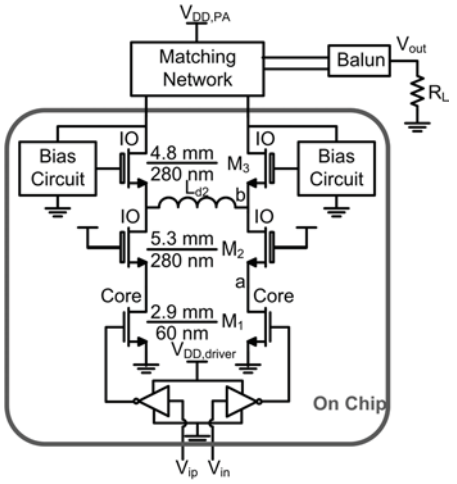

Fig. 4. Stacked differential power amplifier.

The prototype experimental PA has been designed to achieve 30-dBm output power at 6 GHz. In the nominal design, the voltages across the terminals of the core devices and I/O devices are always less than 1.1 V and 2.5 V, respectively. To deliver 30-dBm output power, the load impedance is transformed to a 12.5-Ω differential impedance across the drains of the output transistors using a matching network consisting of bond wires and off-chip capacitors.

B. Layout

Because of the large current needed to drive the 12.5-Ω load, the transistor sizes are very large for M_1, M_2, and M_3, and the metal interconnects are very wide. As a consequence, it is hard to provide a good virtual ground for the differential amplifier, and the parasitic capacitance at node *b* is relatively large. The value of L_{d2} to resonate out the parasitic capacitance at 6 GHz is quite small (0.14 nH), making it difficult to implement. Also the small ratio of L_{d2} to the routing inductance of the drain of M_2 and source of M_3 makes L_{d2} less effective in reducing loss.

To address these issues, the PA is divided into four sub-PAs that are laid out in parallel. Since in each sub-PA the parasitic capacitance is reduced by a factor of four, the required L_{d2} for each sub-PA is four times larger. These inductors are implemented as two-turn spiral inductors. Also, the two sides of the amplifier within each sub-PA are interdigitated to provide a good virtual ground and reduce the routing inductance.

IV. Experimental Results

To demonstrate the concepts embodied in the proposed PA architecture, an experimental prototype has been fabricated in the standard TSMC 65-nm CMOS GP technology. Fig. 5 shows a die photo of the chip. The total chip area is 1.3 mm × 2.2 mm. The chip was attached to a Rogers 4350B printed circuit board using conductive epoxy, and the input and output pads were wire bonded to the top of single-layer capacitors on the board. All other pads were wire bonded directly to the pads on the board. Off-chip baluns were used both at the input and the output of the amplifier. The input and output matching of the amplifier was achieved using narrow-band matching networks tuned to 6.5 GHz.

The output power of the PA was measured using a power meter directly connected to the RF output of the board. On-chip peak detectors were used to monitor the maximum voltages at the drains of all three transistors of the stack (M_1, M_2, and M_3).

Fig. 6 and Fig. 7 show the output power (P_{out}) of the PA, its efficiency and its PAE versus the PA supply voltage $V_{DD,PA}$. As expected, the larger the supply voltage of the amplifier, the larger the output power. The supply voltage for the driver, $V_{DD,driver}$, was 1.1 V.

The amplifier delivers 27.4-dBm of power to a 50-Ω load at 6.5 GHz with a PA supply voltage of 3.6 V and maximum drain-source voltages of the core transistor and the I/O transistors less than 1.1 V and 2.5 V, respectively. For a PA supply voltage of 4.6 V, the output power at 6.5 GHz is 29.6 dBm. Table I shows the output power, efficiency, PAE, and

power gain (G_p) for these two cases. The measurement results include the loss in the connectors, board, and bond wires.

For maximum voltages of 1.1 V and 2.5 V across the drain-source of the core devices and I/O devices, respectively, the simulated output power and efficiency are 30.3 dBm and 38.3%. However, for the same maximum drain-source voltages, the measured output power and efficiency are 27.4 dBm and 19.2%. One reason is the loss in the resistance of the on-chip routing lines, which are estimated to be about 5%. Another source of discrepancy could be related to the routing inductance from the drain of M_2 and source of M_3 to L_{d2}. This large routing inductance impedes the effect of L_{d2} in reducing the loss associated with C_{p2}. To overcome this limitation, the amplifier can be divided into more sub-amplifiers, thus, reducing the routing inductance and increasing the value of L_{d2} for each sub-amplifier. This also reduces the resistance of the routing lines, thus reducing their loss.

If core devices are used for the entire stack, the amplifier can operate at higher frequencies. It is also possible to stack more transistors to increase the supply voltage further and increase the output power. However, the appropriate biasing circuitry must be designed to ensure that the transistors are not overstressed.

V. Conclusion

Transistor stacking has been used as a means of power combining and increasing supply voltage for RF power amplifiers integrated in deep-submicron CMOS VLSI technologies. An experimental stacked power amplifier has been designed and implemented in a standard 65-nm CMOS technology and achieves 29.6-dBm output power with 20.3% efficiency at 6.5 GHz when operated from a supply voltage of 4.6 V.

Acknowledgments

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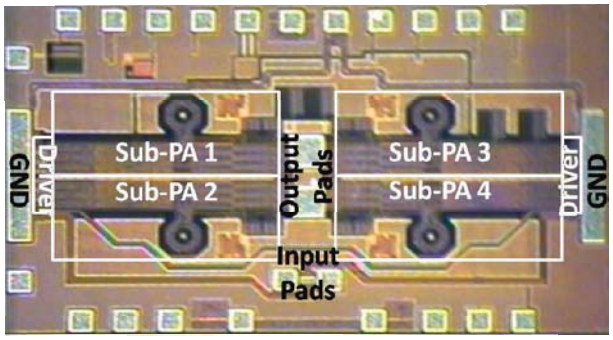

Fig. 5. Die photo of the PA chip.

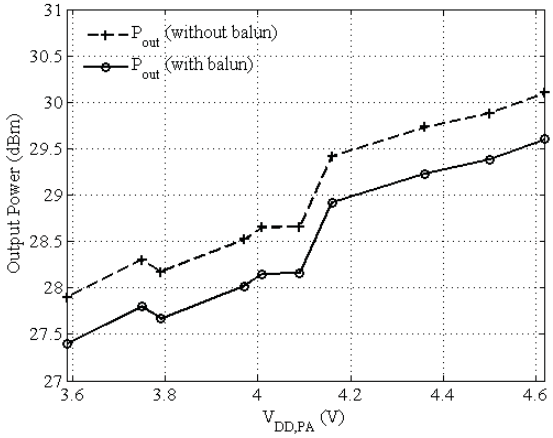

Fig. 6. Measured output power versus the supply voltage of the PA.

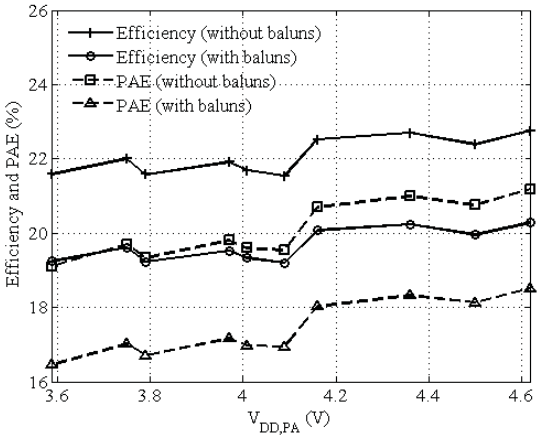

Fig. 7. Measured efficiency and PAE versus the supply voltage of the PA.

Table I
Performance Summary

$V_{DD,PA}$	P_{out} (dBm)	Efficiency	PAE	G_p (dB)	
3.6 V	27.4	19.2%	16.5%	8.4	with baluns
	27.9	21.6%	19.1%	9.4	without baluns
4.6 V	29.6	20.3%	18.5%	10.6	with baluns
	30.1	22.8%	21.2%	11.6	without baluns