A 77 GHz Power Amplifier Using Transformer-Based Power Combiner in 90 nm CMOS

Tao-Yao Chang, Chao-Shiun Wang, and Chorng-Kuang Wang

Graduate Institute of Electronics Engineering & Department of Electrical Engineering
National Taiwan University, Taipei, Taiwan

***Abstract* - A 77 GHz fully-integrated power amplifier (PA) with 50 Ω input and output matching has been realized in a general purpose 90 nm CMOS technology. In order to improve the output power and reduce the signal loss, a transformer and a short stub topology are employed respectively. The power amplifier achieves a saturated output power ($P_{out,sat}$) of +13.2 dBm and 1dB compressed output power ($P_{out,1dB}$) of +11.2 dBm with a peak power-added efficiency (PAE) of 10.4% while operated with a 1.2 V supply.**

***Index Terms* - automotive radar, 77 GHz, transformers, CMOS millimeter-wave integrated circuits, CMOS power amplifiers, power combiners.**

I. Introduction

Recently, researchers show great interest in the application of wireless communication in millimeter-wave (MMW) band, such as the automatic cruise control (ACC) and collision-avoidance systems of 77 GHz automotive radar systems [1] and 60 GHz short-range high data-rate communications [2-3]. In a typical automotive radar system, the transceiver has to deliver a +10 dBm power to antenna port [4]. However the inevitable loss exists between the power amplifier and the antenna, the further improvement in output power capability of the power amplifier is desired. Furthermore, higher output power transmitted from the transceiver can also improve the signal-to-noise ratio (SNR), thus the detection range and the resolution of the radar system can be enhanced.

Since the low supply voltage, low breakdown voltage, and the loss of on-chip passive components in deep-submicron CMOS technology, the most design-challenging RF building block is the power amplifier, especially at millimeter-wave frequencies. Those inherent drawbacks in CMOS technology cause the limitation of the maximum output power capability and efficiency. Several 77 GHz CMOS power amplifiers have been published [1], [8], those power amplifiers are realized in typical circuit topology such as common-source or cascode configuration. However the output power has been relatively low under the low supply voltage requirement of CMOS technology. The state-of-the-art in [9] demonstrates the high output power due to operating at high supply voltage, but the power consumption is higher than other previous works. Therefore it is increasingly crucial to design the more efficient power combining component and the low loss inter-stage matching network to improve the output power capability and efficiency of the power amplifier.

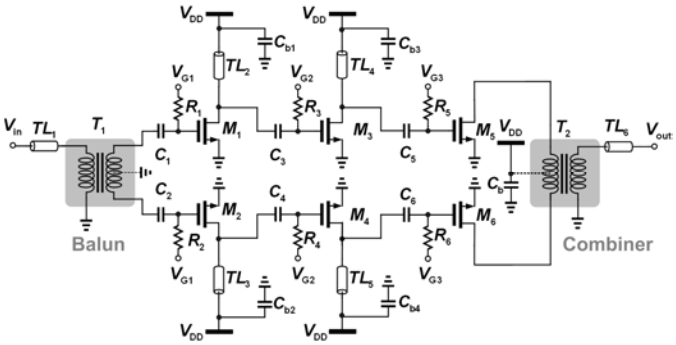


Fig. 1. Schematic diagram of the 77GHz power amplifier

In this paper, a 77 GHz power amplifier is presented by using a transformer-based combiner and short stub matching networks to alleviate those bottlenecks, and realized in a 90 nm general purpose CMOS technology.

The remainder of this paper is organized as follows: section II presents the detailed circuit diagram and design considerations of the 77 GHz power amplifier. Section III demonstrates the power amplifier measurement results and the performance comparisons. Finally, the conclusion is given in section IV.

II. Circuit Description

A. Amplifier Design

The circuit diagram of the power amplifier is shown in Fig. 1. It consists of three stage pseudo-differential cascaded common-source amplifiers. This configuration can provide high linearity and high output power at a low supply voltage. The cascode configuration provides flat I_{DS}-V_{DS} characteristic, lager output impedance and higher gain relative to those of common-source, but its low available output voltage swing is not suitable for the power amplifier operating at low supply voltage.

The gate width of the NMOS in each stage is optimized with taking into account the trade-offs among gain, output power capability, and stability. Since the first and the second stage of the power amplifier act as pre-amplifiers, the device size of the transistors is designed to achieve high gain but moderate output power. On the other hand, in order to deliver high output power, the size of transistor at the last stage is rather wide which is 80 μm. The optimum device size is decided by using a load-pull simulation and load-line theory simultaneously.

978-1-4244-5760-1/10/$26.00 ©2010 IEEE

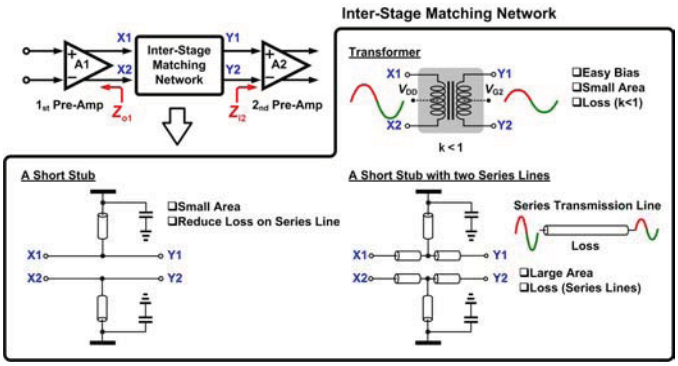


Fig. 2. Typical inter-stage matching networks.

The input and output matching networks are composed of transmission lines and transformers. Each transmission line is a microstrip transmission line with a 0.81 μm thick top metal (copper), since its simplicity on structure provides easily meandered in layout and greatly minimizes the chip area. The layout of the whole microstrip transmission lines is verified by electromagnetic simulators to guarantee the performance at 77 GHz.

B. Inter-Stage Matching Networks and Power Combing

With the conductive substrate and without an ultra-thick metal option (UTM) in general purpose CMOS process, the large loss in passive components in millimeter-wave band is a significant obstacle. Those shortcomings tremendously degrade the power gain and efficiency of the power amplifier. Fig. 2 shows typical inter-stage matching networks between the two differential amplifiers, A_1 and A_2, which are the first and the second stage pre-amplifier of the power amplifier respectively. The networks are designed for the impedance matching from the output impedance of the first stage pre-amplifier, Z_{o1}, to the input impedance of the second stage pre-amplifier, Z_{i2}. Transformers that are employed in a multistage amplifier can both provide a simple way for circuit biasing and greatly reducing chip area consumption. However, it is not suitable for designing an inter-stage matching network since it may increase signal path loss and corrupts PAE due to its poor coupling coefficient, which is usually less than one. Furthermore, series transmission lines in matching network also lead to loss in signal path, which not only decrease the gain performance but also occupy larger area.

In this work, using a short stub topology instead of matching with two series lines can reduce the loss from the series transmission lines in signal path, and therefore enhance the power gain and minimize the chip area simultaneously.

The drawbacks in the deep-submicron CMOS technology are the low breakdown voltage, the low supply voltage, and the low output impedance of transistors, which limit the saturated output power across a given load. Transformers perform the impedance transformation, differential-to-single-ended conversion, and provide the isolation between the primary and the secondary windings to protect transistors.

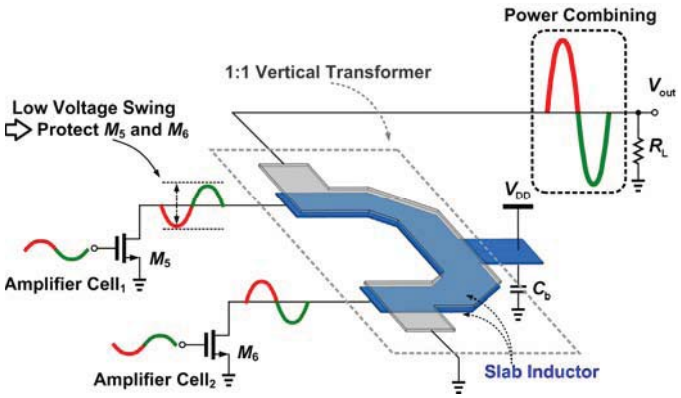


Fig. 3. The output matching network of the power amplifier.

Therefore, applying transformers to combine power is a viable solution to alleviate all problems mentioned above. The transformer-based power combining is shown in Fig. 3 conceptually. The amplifier cells drive the primary windings and the secondary windings of transformers are connected in series configuration. By using the isolation of the transformer, the primary windings operating in low voltages can protect the amplifier cells, and the secondary windings can sum up the voltages from primaries to deliver the higher output power. Since the magnetic flux cancellation from the oppositional line exists in a conventional spiral transformer, this non-ideal effect degrades the power transformation efficiency. The transformer built up by slab inductors can solve this drawback [5].

As shown in Fig. 3, a 1:1 vertical transformer consists of two coupled slab inductors which are designed using top two metals to minimize the loss. This on-chip transformer provides a higher coupling coefficient and better area efficiency than the lateral one. Therefore the vertical transformer used as the output matching network dramatically enhances the power transformation efficiency and transmits much higher output power.

III. Experimental Results

This 77 GHz power amplifier was fabricated in a 90 nm general purpose CMOS technology. Fig. 4 shows the die micrograph. The core area of 0.35×0.3 mm^2 demonstrates a small area, which benefits from the use of a short stub topology and transformers. For the on-wafer testing setup, the measurement results are shown in Fig. 5 and Fig. 6 respectively. Using a 1.2 V supply, the power amplifier provides a small signal gain of 9.9 dB at 77 GHz with input and output matching better than -10 dB, delivers a 1 dB compressed output power of +11.2 dBm and a saturated output power of +13.2 dBm with a peak PAE of 10.4%, and consumes 140.4 mW.

Since the power amplifier draws a lot of current from the power supply, the supply of the power amplifier must be separated from other blocks. Furthermore, the power amplifier can operate with higher supply voltage than other blocks to obtain a larger output power. The 77 GHz power amplifier is measured with a supply voltage raised to 1.5 V as well. Then

it provides a small signal gain of 10.2 dB at 77 GHz with input and output matching better than -10 dB, and delivers a 1 dB compressed output power of +11.8 dBm and a saturated output power of +14.6 dBm with a peak PAE of 10.1%, and consumes 201 mW. The measured output power is comparable to the SiGe amplifier operating at a higher supply voltage [6].

The measured stability K-factor and the reverse isolation are shown in Fig. 7. The stability K-factor is calculated based on the measured S-parameters. The power amplifier is unconditionally stable and reverse isolation is less than -30 dB from DC to 95 GHz while operating at 1.2 V and 1.5 V supply voltages. Table. I summarizes the measured performance and compares with the prior literatures.

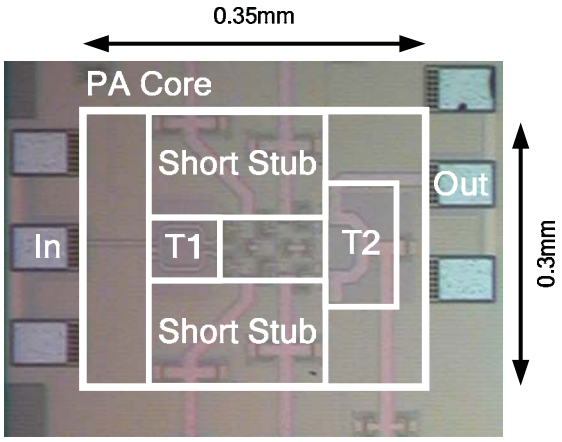
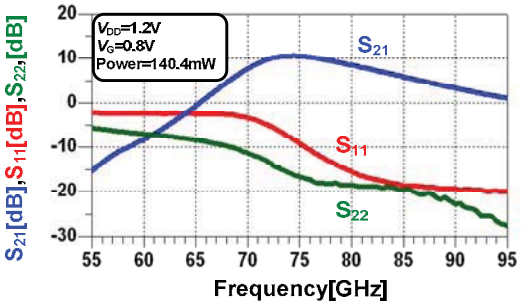
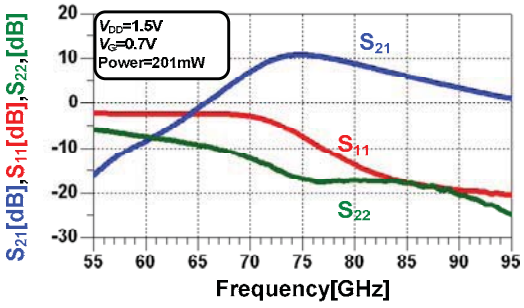


Fig. 4. Die micrograph.

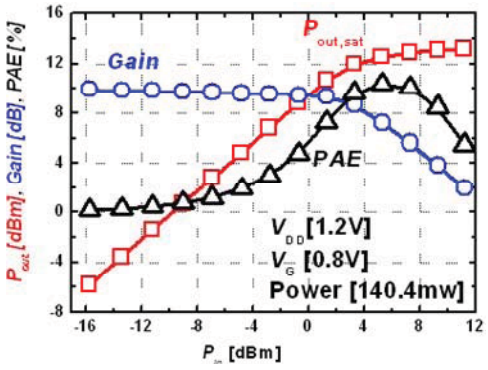


(a)

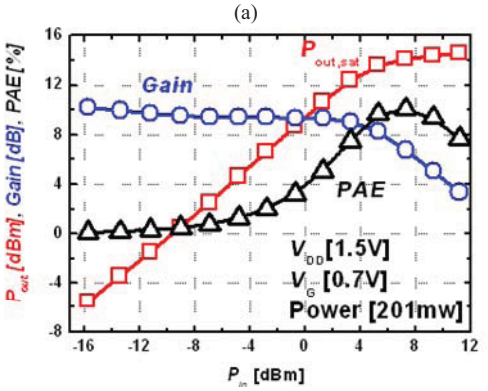


(b)

Fig. 5. Measured S-parameters of the power amplifier operating at (a) 1.2 V and (b) 1.5 V supply.

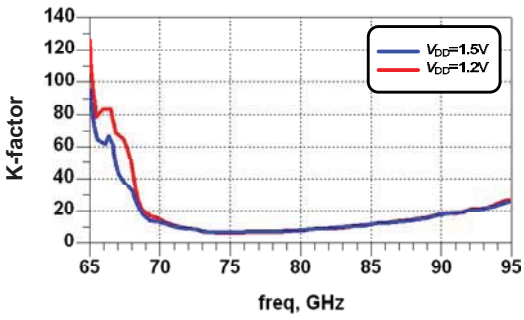


(a)

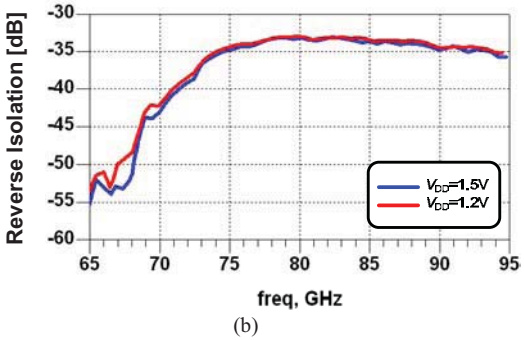


(b)

Fig. 6. Measured large-signal parameters of the power amplifier operating at (a) 1.2 V and (b) 1.5 V supply.



(a)



(b)

Fig. 7. Measured (a) K-factor and (b) reverse isolation of the power amplifier while V_{DD} is biased at 1.2 V and 1.5 V.

IV. Conclusion

A 77 GHz power amplifier in a 90 nm general purpose CMOS technology is presented. A small signal gain of 9.9

dB, a 1 dB compressed output power of +11.2 dBm, a peak power-added efficiency of 10.4% and a saturated output power of +13.2 dBm at 77 GHz have been achieved with a 1.2 V supply. The power amplifier consumes 140.4 mW from a 1.2V supply voltage and the core area is $0.35\times0.3mm^2$. By using the vertical transformer to combine the power from amplifier cells and the short stub inter-stage matching networks to reduce signal loss to improve gain performance, this work is the highest output power and power-added efficiency of CMOS power amplifier at 77 GHz reported, and is comparable to SiGe power amplifiers. This design technique has demonstrated that CMOS technology is suitable for the power amplifier at high output power application such as 77 GHz automotive radar system.

V. Acknowledgments

The authors would like to acknowledge Chip Implementation Center (CIC) and UMC Co., Hsinchu, Taiwain for chip fabrication. They also appreciate High Frequency Testing Center (HFTC) NDL on chip measurement and Prof. Heui Wang, NTU, for equipment support. Also, special thanks give to Hua-Chin Lee, Fu-Chien Huang, Kun-Da Chu and Sung-Han Wen for valuable discussions. This work is supported in part by NSC, and MediaTek Inc., Taiwan.

VII. References

[1] Y.-A. Li, M.-H. Hung, S.-J. Huang, and Jri Lee, "A Fully-Integrated 77GHz FMCW Radar System in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 216-217, Feb. 2010

[2] B. Razavi, "A mm-Wave CMOS Heterodyne Receiver with On-chip LO and Divider," *ISSCC Dig. Tech. Papers*, pp. 188-189, Feb. 2007.

[3] Jri Lee, Y. Huang, Y. Chen, H. Lu, and C. Chang, "A Low-Power Fully Integrated 60GHz Transceiver System with OOK Modulation and On-Board Antenna Assembly," *ISSCC Dig. Tech. Papers*, pp. 316-317, Feb. 2009.

[4] L. H. Eriksson and B.-O As, "A high performance automotive radar for automatic AICC," *IEEE Aemspace and Eleetmnic Sys-tem Magazine*, vol. 10, no. 12, pp. 13, Dee. 1995.

[5] J. Kang, A. Hajimiri, and B. Kim, "A single-chip linear CMOS power amplifier for 2.4 GHz WLAN," *ISSCC Dig. Tech. Papers,* pp. 761–769, Feb. 2006.

[6] U. R. Pfeiffer, S. K. Reynolds and B. A. Floyd, "A 77 GHz SiGe Power Amplifier for Potential Applications in Automotive Radar Systems," *IEEE RFIC Symp.*, pp. 91-94, June 2004.

[7] A. Komijani and A. Hajimiri, "A Wideband 77GHz, 17.5dBm Power Amplifier in Silicon," *Proc IEEE CICC*, pp. 571-574, Sept. 2005.

[8] T. Suzuki, Y. Kawano, M. Sato, T. Hirose and K. Joshin, "60 and 77GHz power amplifier in standard 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 562-563. Feb. 2008.

[9] Jeffery Lee, Chung-Chun Chen, Jen-Han Tsai, Kun-You Lin and Huei Wang;, "A 68–83 GHz power amplifier in 90 nm CMOS," *2009 IEEE MTT-S Int. Microwave Symp. Dig*., pp. 437-440, June 2009.

Table. I. Summary and Comparison

	[6]	[7]	[8]	[9]	[1]	This Work
Frequency [GHz]	77	77	77	68-83	77	77
P_{sat} [dBm]	12.5	17.5	6.3	$\leq$11 / <12 *	10.5	13.2/14.6
$P_{out,1dB}$ [dBm]	11.6	14.5	4.7	$\leq$7.5 / $\leq$10*	6.7	11.2/11.8
PAE [%]	2.5	12.8	--	6.5 / 6 **	8.4	10.4/10.1
Gain [dB]	6.1	17	8.5	>17.6 / >18.1	13.7	9.9/10.2
Supply [volt.]	2.5	1.8	1.2	2.4 / 3.0	1.2	1.2 / 1.5
Power [mW]	325	297	142.2	379 / 495	115	140.4/201
Chip Area [mm^2]	2.1×0.75	1.35×0.45	1.5×0.65	0.8×0.82	N/A	0.35×0.3***
Technology	0.12μm SiGe HBT	0.12μm SiGe HBT	90nm CMOS	90nm CMOS	65nm CMOS	90nm CMOS

*@77GHz **@70GHz, PAE is not available @77GHz ***without pad