3D Multi-chip Integration with System on Integrated Chips (SoIC™)

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Abstract

The electrical characterization of System on Integrated Chips (SoIC™), an innovative 3D heterogeneous integration technology manufactured in front-end of line with known-good-die is reported. Chiplets integration of devices including foundry leading edge 7nm FinFET technology with SoIC™ illustrates its advantages in high bandwidth density and high power efficiency, as compared with 2.5D and conventional 3D-IC with micro-bump/TSV.

Keywords: SoIC, 3DIC stacking, micro-bump, TSV, AI, Chiplets, Heterogeneous System Integration, Front-end Stacking

Introduction

The more challenging performance/power improvement and escalating cost associated with Moore's Law scaling had triggered semiconductor industry reconsidering device and system scaling strategy. Two distinctive efforts and directions emerged recently. One is to boost system performance by adding algorithm-specific performance accelerator/booster chips next to the central processing units. Recent flourish of accelerator processing units (APU) for AI application is an example. And another direction is to optimize the scaling cost by partition SoC chips and scale only those most critical circuit blocks. This is known as SoC partition and "chiplet" integration. A 3D system integration technology platform with high interconnection density, high bandwidth, and high power efficiency is desirable to realize both directions. However, that may not be met by conventional integration using micro-bump stacking. The I/O pin counts of this flip chip stacking have been limited by the micro-bump size, which is difficult to scale beyond 10 um pitch. Furthermore, the scaled micro-bumps/underfill interconnect adds to parasitic capacitance, resistance and inductance, degrading its performance and power

By leveraging advanced foundry wafer front-end processes, SoIC achieves the integration of known good dies (KGDs), that is mixed-and-matched with different chip sizes, technology nodes, technologies (logic/memory, active/passive), and materials, all integrated on a single, compacted new system chip. SoIC offers vertical interconnect density beyond 10K/mm^2 for ultra-high bandwidth interconnection [1-3]. Fig. 1 shows the schematic of how a SoC chip, Fig. 1a, with SRAM blocks partitioned and re-integrated using SoIC technology, Fig 1b. This paper presents more detailed electrical results of SoIC on device, circuit and SRAM functions.

Electrical Characterization

5 advanced packaging interconnect structures, including 2.5D interposer (CoWoS), typical 3D-IC with micro-bumps, and SoIC, with and/or without TSV as illustrated in Fig. 2 are compared. Their electrical performance benchmark results are shown in Table I. It has been reported that 3D-IC performs better than 2.5D [4-6] although the later outperform the former in heat dissipation. SoIC technology enables both ultra-low link latency and ultra-low energy consumption. These results come from the fine pitch (higher bond density), and the shorter wire delay of SoIC bonding. The later comes from its simplified structure and short connection. Near zero capacitance of SoIC interconnect consumes the least energy. SoIC further improves the density of vertical interconnect than that typical 3D-IC does. SoIC also triggers the driver / receiver to be optimized to achieve higher speed and lower power consumption in the future. SoIC shows the advantages in bandwidth density and in energy per bit, an important system index in machine learning, AI inference and training. TSV plays an important role in SoIC system integration and performance. Fig. 3a shows TSV with liner-B exhibits lower leakage current than TSV with liner-A. While Fig. 3b shows no difference in leakage performance for TSV with barrier-A and TSV with barrier-B upon the time finishing the TSV process. However, barrier-B can withstand 400^{o}C for 3 hours thermal torture while barrier-A leads to significant leakage current as depicted in Fig. 3c. The keep out zone (KOZ) size and the impact of TSV stress on near-by device is dominated by TSV dimension. Fig 4 shows the effects of TSV sizes and KOZ on MOEFET Idsat. TSS uses a larger TSV dimension thus requires a larger KOZ to avoid the stress impact on Idsat. SoIC enables a thinner chip stacking with smaller TSV, leading to much smaller KOZ and better chip area utilization. This is particularly important for ultra-high interconnection density in SoC partitioning and chiplet integration.

To characterize possible impact of SoIC integration on the system performances from transistor, circuit, to functional block levels, We carefully compare the performance of foundry 7nm node N and P MOSFETs, ring oscillators (RO), and SRAM compilers, both before and after SoIC stacking [7-9]. On transistor level, Fig.5 and Fig. 6 show the I-V characteristics of SoC (before stacking) and SoIC (after stacking) are identical, showing the robustness of SoIC processes. Critical intrinsic properties of gate dielectrics, gate channel, and junctions, remains intact before and after SoIC integration, as validated by Ion-Ioff, Fig. 7a for NMOS and Fig. 7b for PMOS. On circuit-level, multi-stage ring oscillators exhibits excellent consistency on oscillating frequency vs. off and on power consumption as depicted in Fig. 8a and Fig. 8b, respectively. In-house 7nm SRAM logic chip consisting of various types of compilers – 1-port register file (1PRF), single-port single-bank (SPSB), and ultra-high density single-port single-bank (UHDSPSB), was stacked with SoIC on another logic chip to form a logic-on-logic 3D system integration. Fig. 9a shows the high stability of SRAM minimum operating voltage (Vccmin) before and after SoIC 3D system integration. Fig. 9b shows the stable performance on operating speed of various SRAM compilers modes through a built-in self-test.

Conclusion

Multi-chip integration (chiplet, etc.) enables lower cost and reduced cycle-time at (sub)system level. SoIC™ realizes 3D chiplets integration with additional advantages in system performance, power and form factor. In particular, it shows lower latency and higher power efficiency than conventional 3DIC with micro-bumps. The small form-factor allows it maintain the same size as original SoC, so the "frontend" SoIC™ can be readily integrated with "backend" packaging including fan-out and interposer to enable an innovative holistic 3Dx3D heterogeneous integration for both higher functionality and system performance/ power [10-12].

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References

[1] Doug C.H. Yu, "Advanced System Integration Technology Trend", SiP Global Summit, SEMICON Taiwan 2018.

[2] F.C. Chen, *et al.*, "System_on_Integrated Chips (SoIC) for 3D Heterogeneous Integration", To be presented in ECTC, 2019.

[3] Doug C.H. Yu, "WLSI and Wafer Foundry Growth with Moore's Law and More-than-Moore, and Vice Versa", IWLPC 2018

[4] T. Lo, *et al.*, "Thinning, stacking, and TSV proximity effects for Poly and HK/MG CMOS devices in an adv. 3D integ. process", IEEE IEDM, 2012.
[5] K.F. Yang, *et al.*, "Yield and reliability of 3DIC technology for advanced 28nm node and beyond", VLSI Technology, 2011.
[6] Yang Zhang, "Benchmarking Digital Die-to-Die Channels in 2.5-D and 3-D Heterogeneous Integration Platforms", IEEE TED, 2018.
[7] S.Y. Wu, *et al.*, "A 7nm CMOS Platform Technology Featuring 4th Generation FinFET Transistors with a 0.027um2 High Density 6-T SRAM cell for Mobile SoC Applications", IEEE IEDM, 2016.
[8] Jonathan Chang, *et al.*, "A 7nm 256Mb SRAM in High-K Metal-Gate FinFET Technology with Write-Assist Circuitry for Low-Vmin Applications", IEEE ISSCC, 2017.
[9] D.S. Huang, *et al.*, "Comprehensive device and product level reliability studies on advanced CMOS technologies featuring 7nm high-k metal gate FinFET transistors", Proc. IEEE IRPS, 2018.
[10] Doug C.H. Yu, "New System-in-Package (SiP) Integration technologies", Proc. IEEE CICC, 2014.
[11] Doug C.H. Yu, "WLSI for SiP", IEEE IEDM, 2014. [11] J.Y. Sun, "System scaling for intelligent ubiquitous computing", IEEE IEDM, 2017.
[12] M Ataul Karim, "Power Comparison of 2D, 3D and 2.5D Interconnect Solutions and Power Optimization of Interposer Interconnects", IEEE ECTC, 2013.

TABLE I.
Typical 2.5D, 3D-IC and SoIC Interconnect benchmark (see Fig. 2)

Technology	2.5D	3D-IC F2B	3D-IC F2F	SoIC F2B	SoIC F2F
Bump Density	0.8X	1.0X	1.0X	16.0X	16.0X
Speed*	0.01X	0.1X	1.0X	3.7X	11.9X
Bandwidth Density**	0.01X	0.1X	1.0X	59.7X	191.0X
Power Consumption (Energy/bit)	22.9X	3.7X	1.0X	0.6X	0.05X

*Speed: 1/total wire delay
**Bandwidth Density: Bump Density*Speed

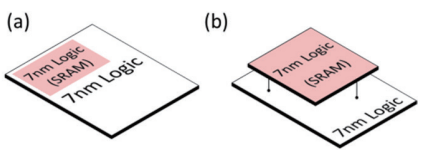

Fig. 1 Schematic pictorial view of (a) SoC before chip-partition, and (b) SoIC after chip-partition and stacking

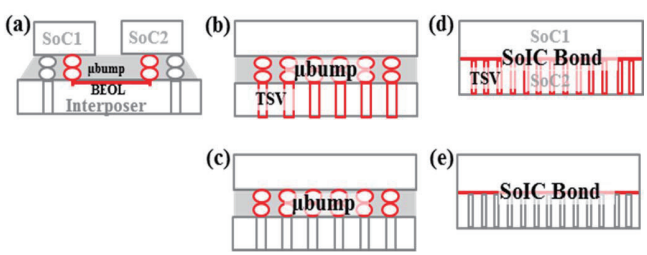

Fig. 2 Interconnect of five package structures: (a) 2.5D Interposer: uBump+1mm BEOL (b) 3D-IC F2B: uBump & TSV (c) 3D-IC F2F: uBump (d) SoIC F2B: SoIC bond & TSV (e) SoIC F2F: SoIC bond.

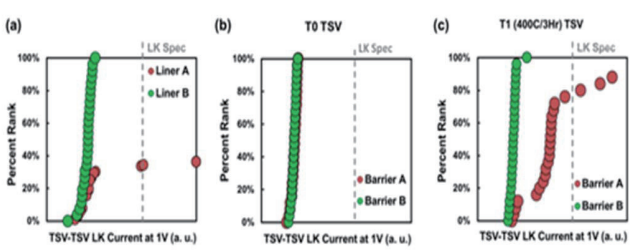

Fig. 3 TSV leakage dependent on (a) TSV liners, (b) TSV barriers. and (c) reliability dependency on the barrier after thermal torture.

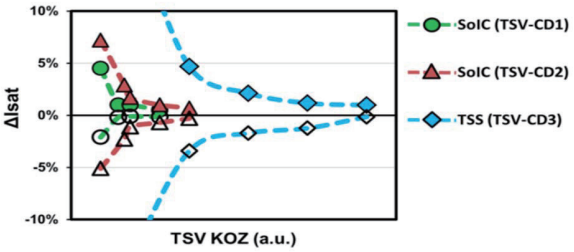

Fig. 4 Idsat characteristics of MOS device with different TSV sizes and KOZ

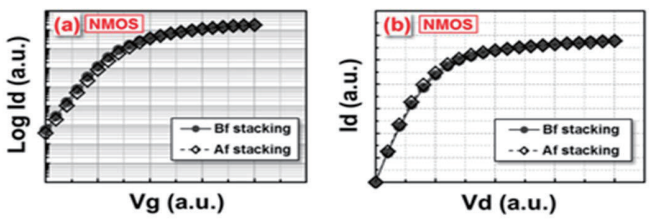

Fig. 5 NMOS (a) Id vs. Vg and, (b) Id vs. Vd before and after SoIC stacking

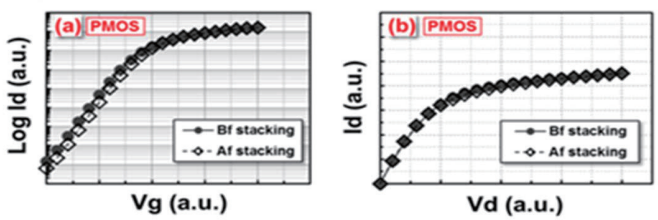

Fig. 6 PMOS (a) Id vs. Vg and, (b) Id vs. Vd not impacted by SoIC

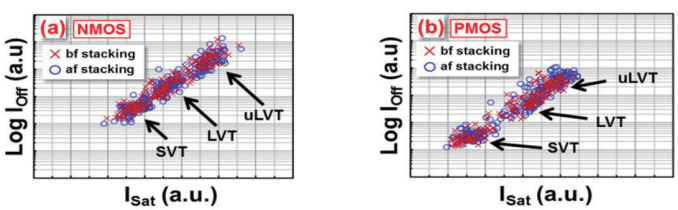

Fig. 7 (a) NMOS and (b) PMOS device performances are comparable with SoIC stacking

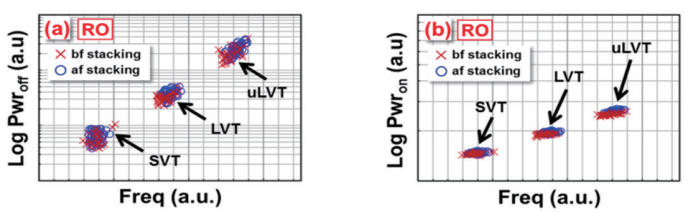

Fig. 8 (a) Off-power vs frequency (b) On-power vs frequency plot for ring oscillators are consistent before and after SoIC stacking

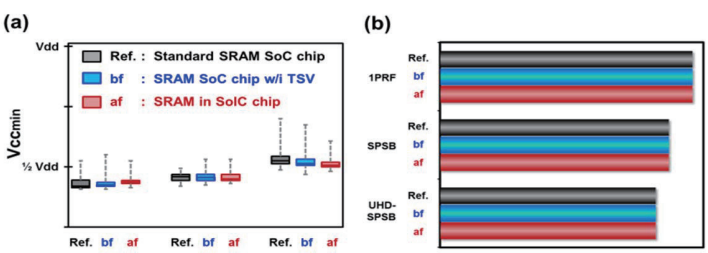

Fig. 9. (a) Vccmin and (b) Speed of SRAM compiler before and after SoIC 3D stacking. SRAM with 1PRF, SPSB, and UHDSPSB modes shows superior stability