Preferential oxidation of Si in SiGe for shaping Ge-rich SiGe gate stacks

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Abstract

The oxidation of SiGe is quite different from that of Si or Ge. By paying attention to the oxidation kinetics of SiGe, a gate stack formation guideline on SiGe is proposed. Based on the understanding of oxidation kinetics, we design the gate stack formation process and demonstrate very good C-V characteristics on SiGe with Si-cap free passivation, by direct deposition of a designed dielectric film, followed by an optimal post-deposition annealing.

1. Background and objective

SiGe gate stack formation process is quite different from that of Si or Ge. A simple oxidation of SiGe does not provide a permissible gate stacks. However, no reliable oxidation model of SiGe in order to achieve a lower D_{it} has been proposed. Since Ge concentration in SiGe recently increases, the oxidation control to manage dielectric/SiGe interface characteristics from fundamental viewpoints is urgently required. Thermal oxidation [1], plasma oxidation [2, 3] and direct high-k dielectrics deposition [4] or nitridation [5-7] have been so far tried to achieve a better gate stack on SiGe. The key technique to Ge-rich SiGe passivation beyond the Si passivation, however, still remains unclear.

Thus, the objective of this paper is to provide the thermodynamic guideline for SiGe gate stack formation, and to demonstrate well-behaved C-V characteristics on Ge-rich SiGe. The thermodynamic guideline will not be sensitive to small possible variations, even though there remains a room for further optimization.

2. Consideration of oxidation kinetics on SiGe

Based on our ample of experiences in Ge and Si oxidation and in conjunction with so many reports in the literatures, we first conjecture how SiGe should be oxidized thermodynamically for better gate stacks.

It is considered that GeO_x formation should degrade the interface in SiGe oxidation process, because GeO might be easily desorbed and poor GeO_x is definitely formed inside SiO_2. This is due to the formation energy difference between SiO_2 and GeO_2, as shown in **Fig. 1**, calculated by using the thermodynamic database [8]. Even if we can successfully form $SiGeO_4$ by "an advanced" oxidation process, SiO_2 is more stable than GeO_2 thermodynamically. This is essentially important for controlling SiGe gate stacks and is quite different from Ge oxidation, in which high-pressure O_2 oxidation works well to control Ge gate stacks [9].

Above hypothetical considerations point out the following two requirements for designing the SiGe gate stack formation.

(1) Preferential oxidation of Si without GeO_x formation.
(2) No Ge pile-up at the interface in the oxidation.

In order to meet the requirement (1), we first reinvestigate the oxygen affinity of Si and Ge thermodynamically in **Fig. 1**. A lower ΔG^o means a larger oxygen affinity of a material. Furthermore, it suggests that a low pressure O_2 (LPO) oxidation at relatively high temperature may suppress the oxidation of Ge, because ΔG^o may become positive. Therefore, LPO seems to be a way to preferentially oxidize Si in SiGe without GeO_x formation.

To meet the requirement (2), only a thin SiO_2 growth is allowed. However, this would be too thin for gate stack application. This means deposited film rather than oxidation is favored. Meanwhile, O_2-PDA is generally required for deposited film to anneal out oxygen vacancies (V_O), the O_2-PDA might degrade the interface of SiGe gate stacks owing to SiGe surface oxidation. To overcome such thermodynamically inconsistent challenges, the dielectric film with low O_2 diffusivity (a low oxygen chemical potential at SiGe dielectric film interface), and with high oxygen affinity (a low ΔG^0 in **Fig. 2**) should be designed. This process may hopefully enable us both to reduce the oxygen chemical potential at the SiGe interface and to stabilize the bulk dielectric film.

Here, we expect that *Y_2O_3 incorporation into SiO_2 could lower the O_2 diffusivity*. This was learned from Y_2O_3-doped GeO_2 [10]. Furthermore, Fig. 2 shows that *Y_2O_3 is one of the most stable oxide (high O_2 affinity)* in terms of the Gibbs free energy, and that Y_2O_3 is also known to be stable on Ge experimentally [11]. Thus, Y-Si-O system was studied for the deposited dielectric film on SiGe in this work.

3. Experimental

The starting substrate was 110-nm-thick SiGe (100) grown on low-doped p-Si (100). Raman spectroscopy analysis of this wafer, shown in **Fig. 3**, indicates that it was $Si_{0.58}Ge_{0.42}$. After HF-last SiGe substrate, $YSiO_x$ was deposited directly by co-sputtering of Y_2O_3 and SiO_2 in Ar, followed by O_2-PDA. Y:Si ratio in $YSiO_x$ (estimated by XPS) and O_2 partial pressure, temperatures and time in PDA were varied, and then SiO_x and GeO_x growth were estimated by XPS, and C-V characteristics were measured for characterizing interface properties of SiGe gate stacks below 100 kHz.

4. Results

First, we investigated the O_2 pressure dependence of SiGe oxidation at 600ºC. **Fig. 4 (a)** shows SiO_x formation which depends on the O_2 partial pressure, while **Fig. 4(b)** shows no GeO_x formation is detected in case of the oxida-

tion condition with O_2 partial pressure of 0.01-atm at 600°C for 30 sec. **Fig. 5** shows the time dependence of GeO_x formation at two different P_{O2} at 600°C. This fact clearly indicates that the preferential oxidation of Si is possible on SiGe by lowering the O_2 partial pressure as expected. It should be stressed that this is in striking contrast to Ge oxidation, where the high-pressure O_2 oxidation is thermodynamically desired [9].

Next, we discuss the O_2 diffusivity in sputtered $YSiO_x$ and SiO_2 films. **Fig. 6 (a)** shows Ge 3d XPS spectrum of $YSiO_x$/SiGe stacks after PDA at 600°C for 30 sec under 1-atm O_2, in which no GeO_x is observed. **Fig. 6 (b)** shows GeO_x growth rate on SiGe in PDA through both deposited SiO_2 and $YSiO_x$ films. This fact strongly suggests that $YSiO_x$ layer on SiGe is quite promising for improving the SiGe gate stack characteristics.

Fig. 7 shows bi-directional C-V characteristics of the Au/$YSiO_x$/SiGe MOSCAP with PDA at 600°C in 1-atm O_2 for 30sec. Note that well-controlled C-V characteristics with no hysteresis are shown in Si-cap free $Si_{0.58}Ge_{0.42}$ gate stack. Since high frequency C-V was strongly affected by the buried SiGe/Si hetero-interface contribution [7], 100 kHz was the maximum in the present measurement configuration.

MOSCAPs with different Y:Si ratio and PDA temperatures were also tested. **Fig. 8** shows the results with different Y:Si ratio. **Fig. 9** shows the results with different PDA temperature for Y:Si ratio of 1:1. Less Y ratio severely degrades the gate stacks (Fig. 8) and more oxidation occurs at higher temperature PDA (Fig. 9), because the accumulation capacitance at 700°C is much higher than that at 400°C. From those results, the condition with 1:1 ratio of Y:Si and PDA at 600°C seems to be the best in the present experiments. Moreover, the results in Fig. 2 and Fig. 6 suggest that SiO_2 will be slightly formed at the interface. The cross-sectional TEM shows that SiO_2-IL is formed ($\leq$ 1 nm), as clearly shown in **Fig. 10**, and that SiGe interface remains sharp even after PDA at 600°C.

5. Discussion

The preferential oxidation has been investigated in the oxidation process of metal-silicide ($MeSi_x$) [12]. The oxidation of $FeSi_2$ or $CoSi_2$ is the typical example in which SiO_2 is formed in the oxidation instead of MeO_x formation. In fact, the preferential SiO_2 coating on $MeSi_x$ has been demonstrated on $FeSi_2$, and it is also thermodynamically understood as schematically shown in **Fig. 11**.

In case that there is initially a Si-based oxide at the surface of SiGe, it is expected that the oxygen chemical potential should be quite low at the SiGe interface [13]. That should work quite effectively for suppressing Ge oxidation of SiGe in the present case, as expected in Fig. 1.

It is known that there are a few phases in Y-Si-O system such as Y_2SiO_5, $Y_4Si_3O_{12}$, or $Y_2Si_2O_7$ [14]. In fact, Y_2SiO_5 was experimentally studied from the viewpoint of oxygen permeability [15]. The activation energy in the oxygen diffusion process in Y_2SiO_5 is rather higher than that in SiO_2. It is expected that the diffusion constant should be lower in Y_2SiO_5 around 600ºC. This result is quite consistent with the present results.

Next, let's think about the interface at SiGe/SiO_x naively. If the top surface of Si in SiGe is oxidized, the interface might be Ge rich after oxidation, and Ge-O bond should be detected. However, no Ge-O bond was detected within our experimental resolution in XPS. This fact suggests that Ge is not piled up at SiGe surface possibly due to an exchange of Ge to Si in thin SiO_2 region.

Finally, another interesting finding in this study is addressed. **Fig. 12** estimates the relative dielectric constant, *k*, of $YSiO_x$. A good linearity in the relationship between EOT and physical thickness of $YSiO_x$ shows that the *k* value of $YSiO_x$ is about 13. It is also interesting to note that the *k* value is higher than expected, because both SiO_2 and Y_2O_3 have a smaller *k* value than 13. This is explainable by considering the molar volume shrinkage in the film according to the Clausius-Mossotti relation, as discussed in Y-Sc-O system [16]. Further EOT scalability for advanced CMOS will be achieved by combining high-k dielectrics such as $YScO_3$ on medium-k $YSiO_x$ for SiGe.

6. Conclusion

We have proposed and achieved the thermodynamic control of SiGe oxidation. Key points are, 1) Ge oxidation should be suppressed, and 2) the interface layer should be SiO_2, which should be as thin as possible. Deposited films with the low O_2 diffusivity such as $YSiO_x$, together with the optimal O_2-PDA, meet those two requirements, and enable to achieve well-controlled gate stacks. This view can hopefully be generally applicable for the gate stack formation on new channel materials.

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References

[1] F. K. LeGouse et al., JAP **65**, 1724 (1989).
[2] P. W. Li et al., APL, **63**, 2938 (1993).
[3] M. Mukhopadhyay et al., APL **65**, 895 (1994).
[4] S. Pal et al., JAP **90**, 4103 (2001).
[5] J. Huang et al., APL **88**, 143506 (2006).
[6] J. Huang et al., APL **90**, 023502 (2007).
[7] J. Han et al., APEX **6**, 051302 (2013).
[8] HSC CHEMISTRY ver. 6.1 (2006).
[9] C. H. Lee et al., IEEE TED-**58**, 1295 (2011).
[10] C. Lu et al., APL **104**, 092909 (2014).
[11] A. Toriumi et al., chapter **11**, "Advanced Gate Stacks for High mobility Semiconductors," (Springer 2007).
[12] K. Kurokawa and A. Yamaguchi, Sol. Stat. Phenom. **127** (2007) 227.
[13] X. Li et al., IEDM 2015, 21.4
[14] Z. Sun, M. S, Li and Y. C. Zhou, Int. Mat. Rev. **59** (2014) 357.
[15] Y. Ogura et al., Mat. Trans. **42** (2001) 1124.
[16] C. Lu et al., APL **107** (2015) 072904.
[17] J. C. Tsang et al., JAP **75** (1994) 8098.
[18] R. Kube et al., JAP **107** (2010) 073520.

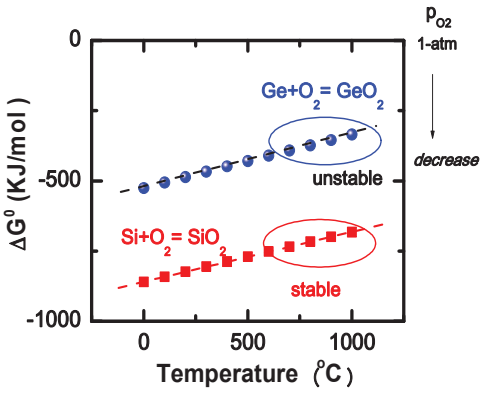

Fig. 1 The Ellingham diagram for GeO_2 and SiO_2. GeO_2 formation becomes unlikely as P_{O2} decreases at relatively high temperatures, while SiO_2 remains stable. This difference of the thermal stability between SiO_2 and GeO_2 suggests a pathway to selectively oxidize Si in SiGe oxidation.

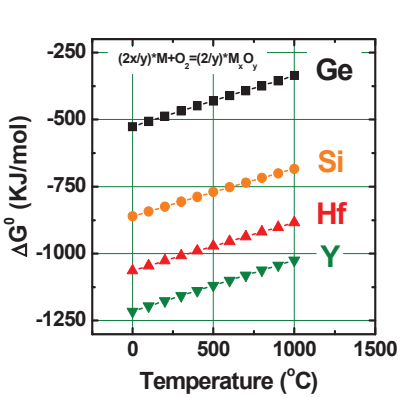

Fig. 2 The standard Gibbs free energy of various metal oxide formations as a function of temperature calculated from thermodynamic database [8]. Note that the chemical reaction is normalized to one O_2 molecule. It can be seen that Y_2O_3 is one of the most stable oxide (high O_2 affinity).

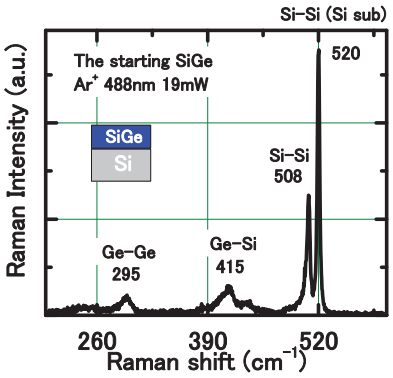

Fig. 3 A Raman spectrum of the starting SiGe substrate. By using the method developed by J.C Tsang *et al.* [17], Ge composition in the starting SiGe is found to be 42%.

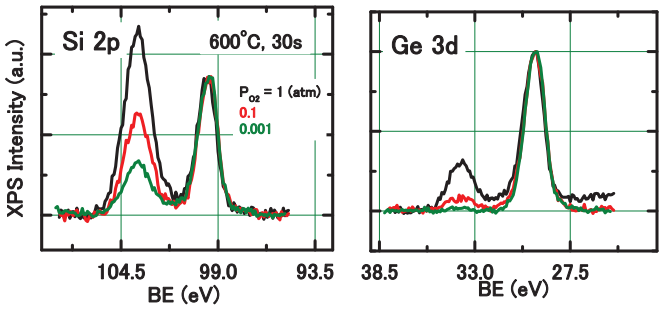

Fig. 4 XPS spectra of **(a)** Si 2p, **(b)** Ge 3d in SiGe oxidation at 600°C for 30 seconds at various P_{O2}. The results clearly show that a lower P_{O2} can effectively suppress the Ge oxidation (no GeO_x peak is detected at PO_2=0.001-atm). This result strongly suggests us the preferential oxidation of Si in SiGe may be possible thermodynamically, as expected in Fig. 1.

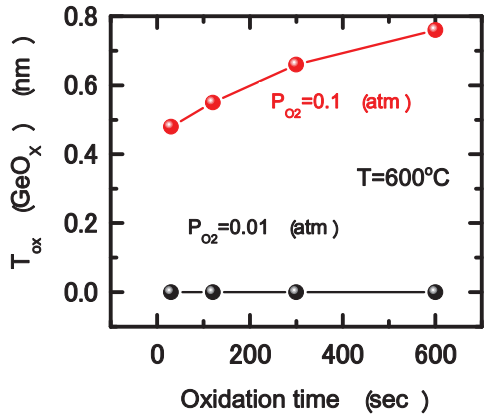

Fig. 5 Ge oxidation rate in SiGe oxidation at 600°C at two different P_{O2}. By reducing P_{O2}, Ge oxidation rate is dramatically reduced. GeO_2 thickness was measured by XPS. This suggests the possibility of Si preferential oxidation on SiGe over a certain period of time by reducing P_{O2}.

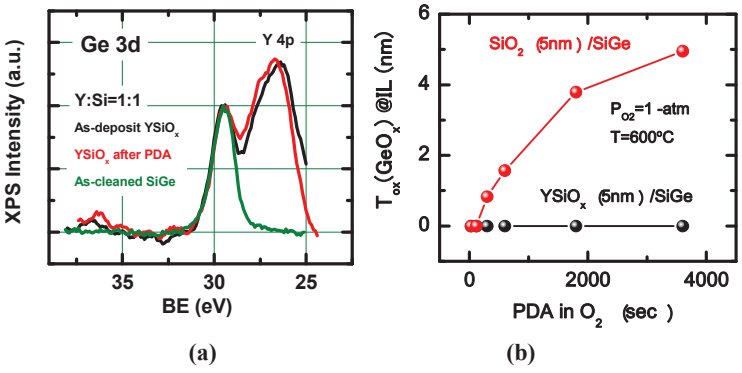

Fig. 6 (a) Ge 3d XPS spectrum of $YSiO_x$/SiGe stacks after PDA at 600°C for 30 seconds at 1-atm O_2. It shows that no Ge oxidation occurs during PDA. **(b)** The GeO_x growth of $YSiO_x$/SiGe and SiO_2/SiGe gate stacks during PDA also at 600°C for 30 seconds at 1-atm O_2. 5 nm of $YSiO_x$ and SiO_2 were both deposited on SiGe by sputtering prior to PDA. Combined with the observations in Fig. 2 and 3, this indicates that P_{O2} at $YSiO_x$/SiGe may be significantly reduced by $YSiO_x$, i.e. $YSiO_x$ has a low O_2 diffusivity, and that the O_2 chemical potential at the interface should be quite low. Thus, this process is very promising for SiGe gate stack formation.

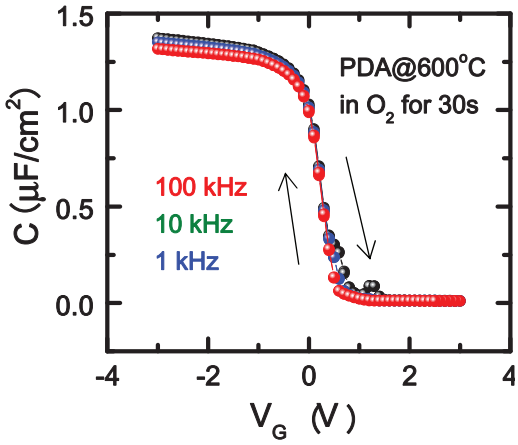

Fig. 7 Bi-directional C-V curves of an $YSiO_x$(Y:Si=1:1)/SiGe MOSCAP with PDA at 600°C in 1-atm O_2 for 30s. Au and Al were used as top and back contacts, respectively. Well-controlled C-V characteristics in MOS capacitors are achieved below 100 kHz. This fact indicates that $YSiO_x$ film can control SiGe interface well as designed.

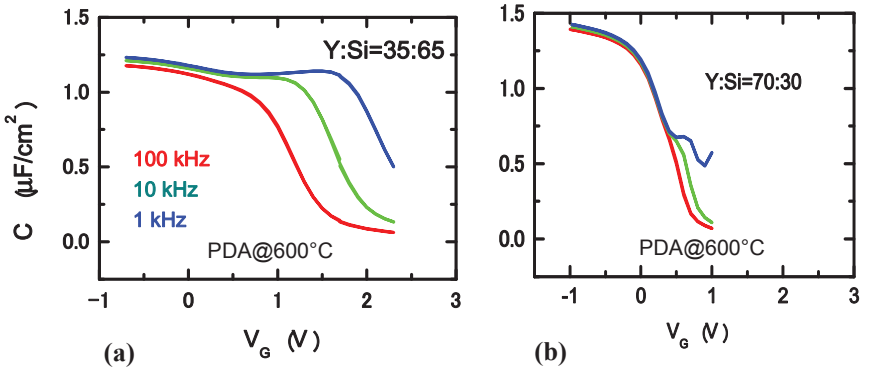

Fig. 8 The C-V curves of $YSiO_x$/SiGe MOSCAPs with **(a)** Y:Si=35:65, and **(b)** Y:Si=70:30. The whole fabrication process was the same as the one in Fig. 7 except the Y:Si ratio. The results show that in the same PDA, D_{it} increases as the Y:Si ratio deviates from 1:1, suggesting Y:Si=1:1 may be the best condition in terms of electrical properties.

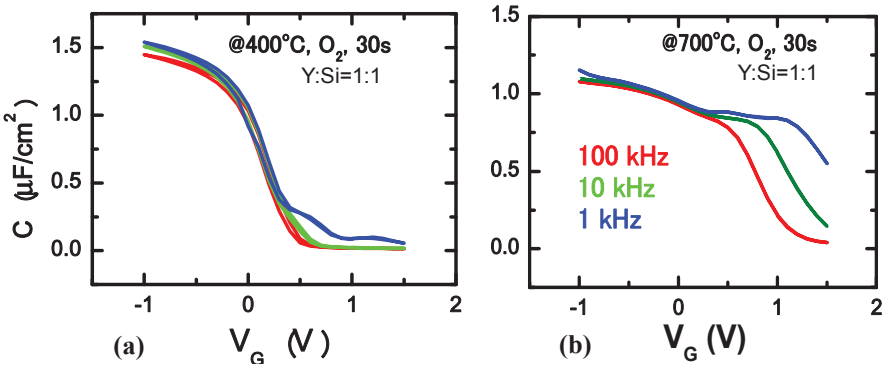

Fig. 9 The C-V curves of $YSiO_x$ (Y:Si=1:1)/SiGe MOSCAPs with PDA at **(a)** 400°C and **(b)** 700°C. The whole fabrication process was the same as the one in Fig. 7 except the PDA temperature. It can be seen that PDA at higher temperatures leads to the interface degradation, which might be due to Ge oxidation, while PDA at lower temperatures gives rise to a hysteresis, possibly due to remaining oxygen vacancy in the bulk. Hence, we conclude that 600°C is may be the optimal PDA temperature in terms of electrical properties in the present experimental conditions.

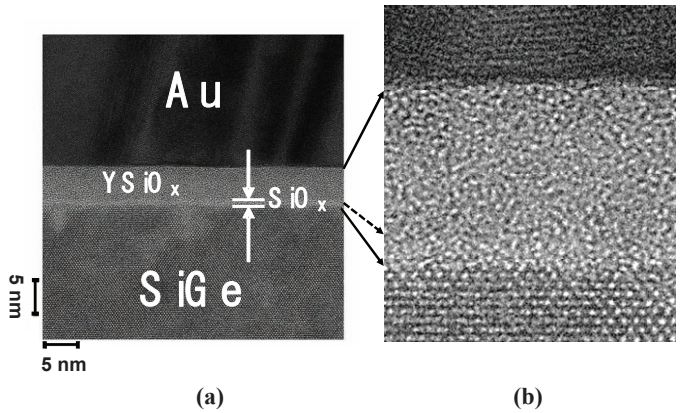

Fig. 10 (a) A cross-sectional TEM image of the $YSiO_x$/SiGe MOSCAP in Fig. 7. **(b)** The zoom-in image of the $YSiO_x$/IL(SiO_2)/SiGe interface. This shows the sharp $YSiO_x$/SiGe interface of the $YSiO_x$/SiGe MOSCAP after PDA at 600°C. The thickness of SiO_2-IL is estimated to be around 1 nm.

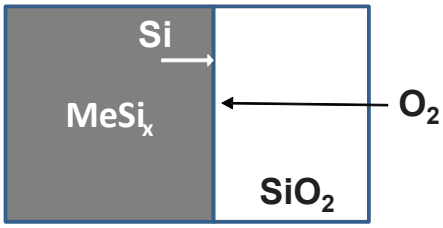

Fig. 11. A schematic of $MeSi_x$ oxidation. When the oxygen affinity of metal is lower than that of Si, and Si diffusion is fast enough to supply for Si oxidation, SiO_2 film is formed on $MeSi_x$. $FeSi_2$ is a typical example, while $TiSi_2$ or WSi_2 is not the case, but (MeO_x+SiO_x) film is formed. The former is basically the same as SiGe oxidation. Furthermore, it is reported that the diffusion constant of Si is comparable with that of Ge in SiGe [18]. Thus, SiO_2 is preferentially oxidized in thin SiO_2 region.

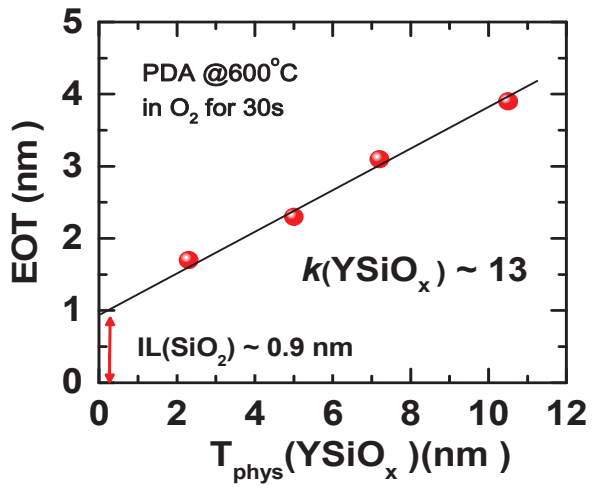

Fig. 12 EOT vs physical thickness to estimate the dielectric constant of $YSiO_x$ (Y:Si=1:1) on SiGe MOSCAPs with PDA at 600°C in 1-atm O_2 for 30s. It indicates that k~13, which is higher than as expected, because k of Y_2O_3 is around 12. It might be due to the molar volume shrinkage in the Clausius-Mossotti relationship. Furthermore, the thickness of IL (SiO_2) is estimated to be 0.9 nm, which is consistent with the TEM image in Fig. 10.