Non-Volatile RRAM Embedded into 22FFL FinFET Technology

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Abstract

This paper presents key specifications of RRAM–based non-volatile memory embedded into Intel 22FFL FinFET Technology. 22FFL is a high performance, ultra low power technology developed for mobile and RF applications providing extensive high voltage and analog support and high design flexibility combined with low manufacturing costs [1]. Embedded RRAM technology presented in this paper achieves 10^4 cycle endurance combined with 85°C 10-year retention and high die yield. Technology data retention, endurance and yield are demonstrated on 7.2Mbit arrays. We describe device characteristics, bit cell integration into the logic flow, as well as key considerations for achieving high endurance and retention properties.

Introduction

RRAM [2-4] and MRAM [5] are the leading candidates for replacing flash as embedded non-volatile memory solution for several growing market segments. Internet of Things devices, field-programmable arrays and chipsets with on-chip boot data storage are potential applications which stand to benefit from the lower manufacturing costs and excellent retention capabilities of these technologies. Due to its magnetic-field immunity, RRAM-based non-volatile memory technology is especially appealing for products which can be easily subjected to malicious magnetic attack. In addition, usage of a relatively simple device stack and well-established etch technologies simplifies achieving high yields at low manufacturing costs, positioning RRAM as an excellent low-cost alternative to the competing technologies.

Device Characteristics

This work uses a noble metal-based Bottom Electrode (BE) Assembly, a TaO_x-based HiK dielectric, and a Ta-based Oxygen Exchange Layer (OEL) (Fig.1a). Example Resistance-vs-Voltage characteristics are shown on Fig. 1b.

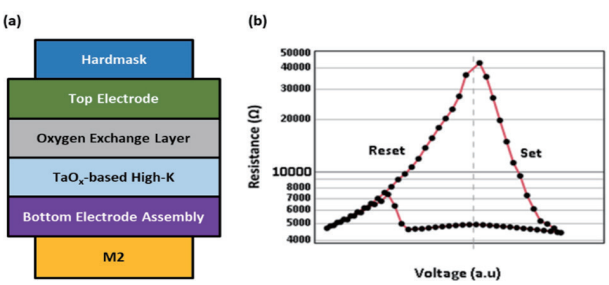

Fig. 1. (a) Simplified stack schematic. (b) Typical device R-V characteristics.

Typical Low Resistance State (LRS) resistances are in the range of 3kOhm – 7kOhm. A typical High Resistance State (HRS) resistance is >30kOhm. Typical forming voltages are 1V-1.5V. The target device size is ~100nm.

Test vehicle

Fig. 2 shows a cross-sectional TEM of an RRAM Array embedded between Metal 2 and Metal 4 layers of the 22FFL logic process.

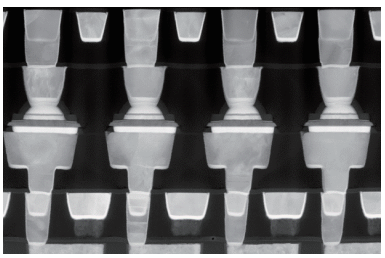

Fig. 2. Cross-sectional TEM of an RRAM array embedded between M2 and M4 of the 22FFL logic.

Fig. 3 shows the layout of the 1T-1R RRAM cell used in this work. The cell area is 216nm x 225nm = 0.0486μm^2.

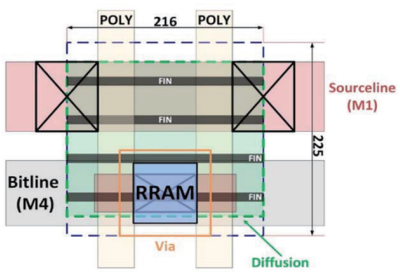

Fig. 3. Layout of the 1T-1R cell used in this work.

We employ a 128b-Triple error correction. The writing protocol employs Write-Verify-Write scheme with a sequence of pulses of increasing amplitudes and lengths. Read sensing is executed with a low amplitude pulse and data readout is performed by detecting the differential current between the RRAM element and a precision thin film resistor [6].

Endurance

Formation of a conductive filament and switching between the LRS and HRS involves the movement of oxygen ions. Management of the oxygen distribution throughout switching cycles is paramount to achieving high endurance and retention characteristics. The BE Assembly, OEL, and corresponding HiK interfaces all contribute to the evolution of the oxygen distribution. In practice, endurance of the RRAM array is largely driven by loss of oxygen ions from the filament area into the OEL during device cycling between LRS and HRS. Loss of oxygen to the OEL leads to an increase in the current needed to reset the device into HRS. A specific RRAM cell is no longer operational after the current needed to achieve the desired HRS resistance exceeds the current available from the access transistor.

Fig. 4 shows the I_Reset and I_Set for two stacks used during process development, Stack A and Stack B, as a function of the number of switching cycles experienced by the devices.

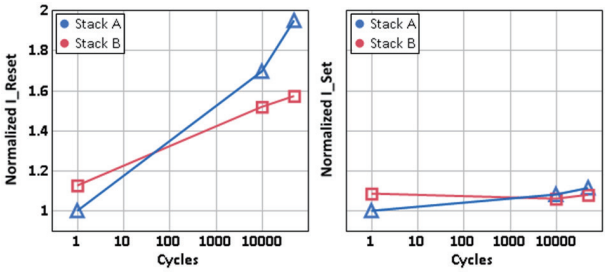

Fig. 4. Normalized I_Reset and I_Set vs the number of switching cycles experienced by the devices.

For this experiment, similarly to the array operation, the switching pulse amplitude was increased to achieve pre-set HRS or LRS resistance levels ("Verify" resistances).

Fig.5 shows median array-level bit error rate vs number of cycles for Stack B, designed to moderate I_reset increase with cycling. The data demonstrate a cycling-induced bit error rate <5E-6 for 10K cycles, a value well below the ECC budget.

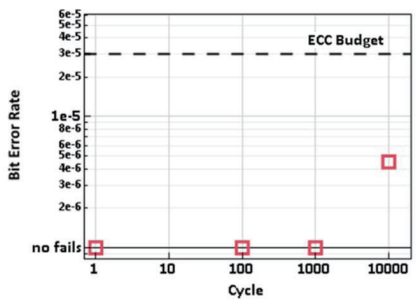

Fig. 5. Bit error rate vs number of switching cycles experienced by the arrays.

Retention

Fig. 6 shows the projected bit error rates for 85C 10-year retention for Stack A and Stack B. Data are shown for several Reference Resistance (RR) levels (RR1<RR2<RR3) for uncycled arrays and arrays subjected to 20K switching cycles.

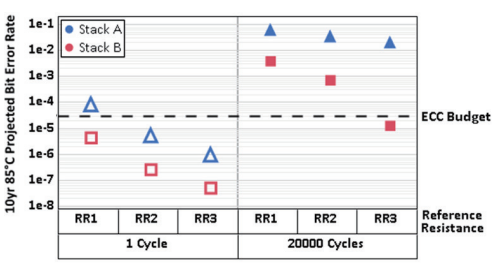

Fig. 6. Projected bit error rates for 85°C 10-year retention for different Reference Resistances (RR1<RR2<RR3). Uncycled arrays (left) vs arrays after 20K cycles (right).

Retention of TaO_x -based RRAM arrays is mainly driven by the retention of the LRS state. As such, projected 85°C 10-year bit error rate is decreasing with increasing Reference Resistance. The practical choice of the Reference Resistance value for RRAM array operation is the direct tradeoff between retention and endurance. Endurance data shown on Fig. 5 were collected at the Reference Resistance value of RR3, which was found to provide optimal overall characteristics. Stack B demonstrates 10-year 85°C projected bit error rates <10E-7 for uncycled bits and ~1E-5 for arrays after 20K switching cycles.

Cycling-induced retention degradation

Fig. 6 demonstrates substantial retention degradation between uncycled arrays and arrays which experienced 20K switching cycles. To help understand the nature of this degradation, Fig. 7 shows R-V characteristics of the LRS state of a bit which underwent an increasing number of switching cycles.

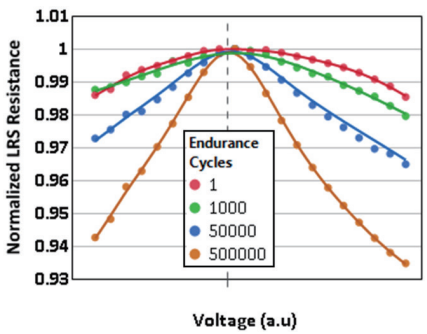

Fig. 7. R-V characteristics for the LRS state of a bit which has undergone an increasing number of switching events.

Increasing tunneling-like behavior of the cycled bits points to lower vacancy density and resultant higher oxygen concentration in the filaments of cycled bits. Degradation of the retention characteristics of the cycled bits is consistent with this increase of the oxygen content in the filament. As can be seen from Fig. 6, the amount of cycling-induced retention degradation is dramatically reduced for Stack B compared to Stack A. This improvement is due to significant moderation of cycling-induced I_reset increase for Stack B (Fig. 4) which results in lower oxygen content in the cycled filaments of this stack.

Summary

An industry-leading combination of high-retention, high-endurance RRAM-based e-NVM and high performance ultra low power 22FFL FinFET technology has been developed. RRAM technology achieves 85°C 10-year retention and 10K endurance, and was demonstrated on 7.2Mbit arrays and full 300mm wafers.

References

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