19.1 A Chopper Current-Feedback Instrumentation Amplifier with a 1mHz 1/*f* Noise Corner and an AC-Coupled Ripple-Reduction Loop

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In the precision mechatronics of wafer steppers, thermal expansion is an important source of error. To compensate for this, the temperature of critical mechanical components must be measured with high resolution (<1μK), typically by using precision thermistor bridges. Furthermore, this resolution must be maintained over several minutes, which means that the amplifier used for bridge readout should have a 1/*f* noise corner of only a few mHz. Such noise performance is well beyond the capabilities of currently available CMOS amplifiers [1-3].

Although 1/*f* noise can be reduced by chopping or auto-zeroing, chopping is preferred for its superior low-frequency noise performance [4]. However, the up-modulated offset and 1/*f* noise causes significant ripple. This may be suppressed by a sample-and-hold filter [1,5], or by the use of auto-zeroing [4]. However, both techniques involve sampling, and therefore, incur a certain noise penalty due to noise folding.

This paper describes a chopper current-feedback instrumentation amplifier (CFIA) with a continuous-time (CT) ripple-reduction loop (RRL). The loop synchronously demodulates the amplifier's output ripple, and then drives it to zero by canceling the offset of the input stage. Due to the CT nature of the loop, it does not suffer from noise folding. By using a three-stage nested-Miller topology [6], and chopping the 1st and 2nd stages, the amplifier achieves a 1/*f* noise corner of 1mHz, a noise density of 15nV/√Hz and an offset of less than 5μV. Furthermore, the combination of chopping and the use of a current-feedback topology [5] results in a DC CMRR of greater than 130dB.

A simplified block diagram of the chopped CFIA and the RRL is shown in Fig. 19.1.1. Input transconductor G_{m3} and feedback transconductor G_{m4} convert the input and feedback voltages into corresponding currents. Their difference is then applied to the virtual ground established by a 2-stage opamp (G_{m2} and G_{m1}). The overall feedback ensures that the output currents of G_{m3} and G_{m4} cancel and thus $V_{out}/V_{in} = (R_1+R_2)/R_2$. To save power, while retaining 50pF drive capability, a Class-AB output stage G_{m1} is chosen. The preceding two stages, G_{m3} (G_{m4}) and G_{m2} are both chopped to eliminate their 1/*f* noise. G_{m3} (G_{m4}) is also gain-boosted, and together these two stages provide enough DC gain (190dB) to reduce the input-referred 1/*f* noise of the output stage to negligible levels.

The RRL consists of capacitor C_4, chopper CH_6, G_{m6}, C_3 and G_{m5}. C_4 converts the amplifier's output ripple $V_{out,ripple}$ into an AC current I_{AC}, whose amplitude is proportional to the derivative of $V_{out,ripple}$. This current is demodulated by CH_6, and the resulting DC current I_{DC} is integrated by C_3 to generate a voltage V_D that is proportional to the ripple amplitude. This is fed back via G_{m5} to the outputs of G_{m3} and G_{m4}, thus compensating for the offset of G_{m3} (G_{m4}). The RRL functions as a narrowband notch filter at the chopping frequency f_{chop}. Since the notch is quite narrow (~3.5kHz wide at a gain of 20 and a 40kHz chopping frequency), it has little effect on the amplifier's measured closed-loop response (Fig. 19.1.5).

Due to the action of CH_6, the integrator's offset, V_{OS3}, appears as a square wave at node B (Fig. 19.1.1). This square wave appears across C_4, and cannot be distinguished from the output ripple. As a result, the ripple will not be completely cancelled. The problem can be mitigated by using a gain-boosted cascode buffer to isolate CH_6 from C_4, as shown in Fig. 19.1.2. However, as depicted in Fig. 19.1.3 (left), the chopped offset of the boosters GB_n and GB_p together with the drain capacitance C_{par} of the current sources M_{25} and M_{26} will still lead to significant residual ripple. To reduce this further, the position of the chopper is modified, as shown in Fig. 19.1.3 (right) so that these drain capacitances are located at the virtual grounds established by the gain-boosting amplifiers [7]. The chopped offset of the booster only results in a small AC current $i_{AC,}$, which is then filtered out by C_3 acting as a passive integrator.

While the chopped offset of the 1st stage is integrated by the nested-Miller compensation network, the chopped offset of the 2nd stage experiences a different transfer function. Thus, the RRL cannot cancel these two sources of ripple simultaneously. In this design, the RRL is used to cancel the ripple associated with the 1st stage, while the ripple associated with the 2nd stage is suppressed by chopping it at a much higher frequency. With CH_1, CH_2, CH_3, CH_6 clocked at f_{ch1}=30kHz and CH_4, CH_5 clocked at f_{ch2}=510kHz, measurements show that the amplitude of the output ripple at f_{ch1} is reduced 1100 times: from 48mV to 41μV. However, a larger second harmonic (78μV) is also present. This is due to the fact that any chopper residuals across C_3 (Fig. 19.1.2) are modulated by CH_3 to the even harmonics of f_{ch1}. However, at the closed-loop gains for which the amplifier is designed (=183), the amplifier's bandwidth is low enough to effectively filter out such harmonics. At a gain of 200, the input-referred output ripple and noise are 0.55μV_{rms} and 0.95μV_{rms} respectively, into a 4kHz bandwidth.

Since the gain error of a thermistor bridge is about 0.5%, the amplifier's gain accuracy does not need to be much better. This can be achieved by ensuring that the transconductances G_{m3} and G_{m4} are well matched. Fig. 19.1.4 shows the schematic of the 1st-stage amplifier. Since the common-mode voltages of G_{m3} and G_{m4} are different, low-threshold cascode transistors M_3, M_4, M_9 and M_{10} are used to regulate the drain-source voltages of the input transistors M_1, M_2, M_7 and M_8 of G_{m3} and G_{m4}, thus reducing mismatch due to the channel-length modulation. Measurements on 20 samples show that the amplifier's gain accuracy is less than ±0.5% at a nominal gain of 200.

The 4.8mm² chip is fabricated in a 0.7μm CMOS process (Fig. 19.1.7). Noise measurements are made with the CFIA configured for a closed-loop gain of 6667 (to ensure that its noise is dominant) and followed by a low-noise amplifier with a gain of 100. The amplifier's unchopped 1/*f* noise corner is 3kHz. Chopping only the 1st stage results in a noise density of 15nV/√Hz and a 1/*f* noise corner of 0.1Hz. Measurements on 12 samples show that the amplifier's offset is then less than 1μV. Chopping both the 1st and 2nd stages increases the offset to 5μV, mainly due to the high chopping frequency used in the 2nd stage. However, as shown in Fig. 19.1.6, the noise spectral density of 15nV/√Hz now remains flat down to 1mHz. Since the amplifier's offset is smeared by the window function of the spectrum analyzer (HP3562A), the 1/*f* noise corner could not be accurately measured, but it is clearly about 1mHz. This agrees well with the results of periodic noise analysis simulations in Spectre RF. This low 1/*f* noise and thermal noise have been achieved with low-power consumption: the amplifier's noise-efficiency factor [8] is 8.8, which is quite respectable [1,2].

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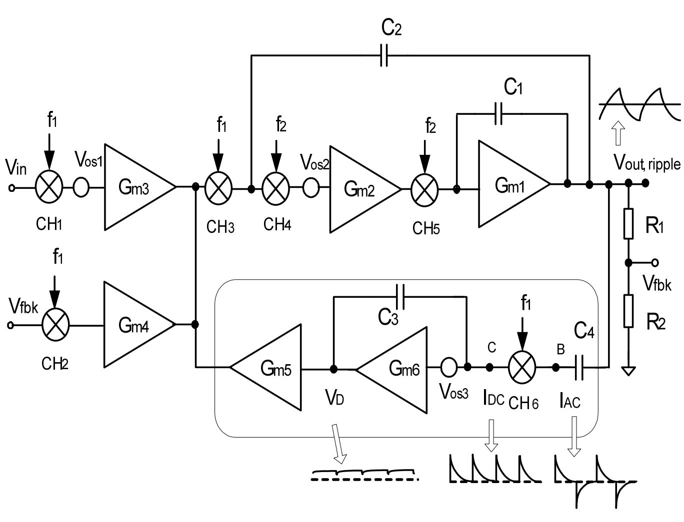

Figure 19.1.1: Simplified block diagram of a current-feedback instrumentation amplifier with an AC-coupled ripple reduction loop.

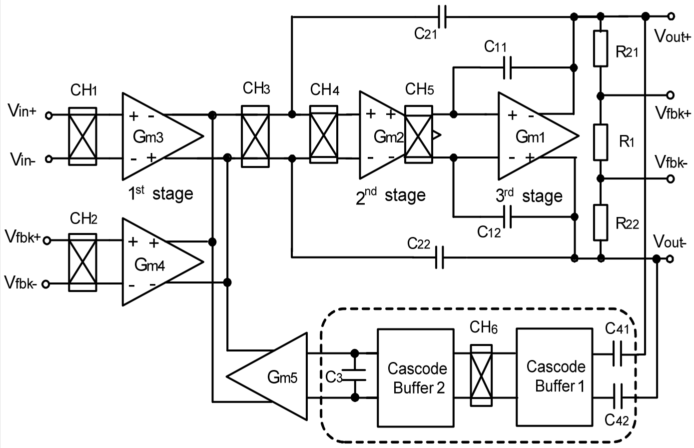

Figure 19.1.2: Block diagram of the implemented CFIA.

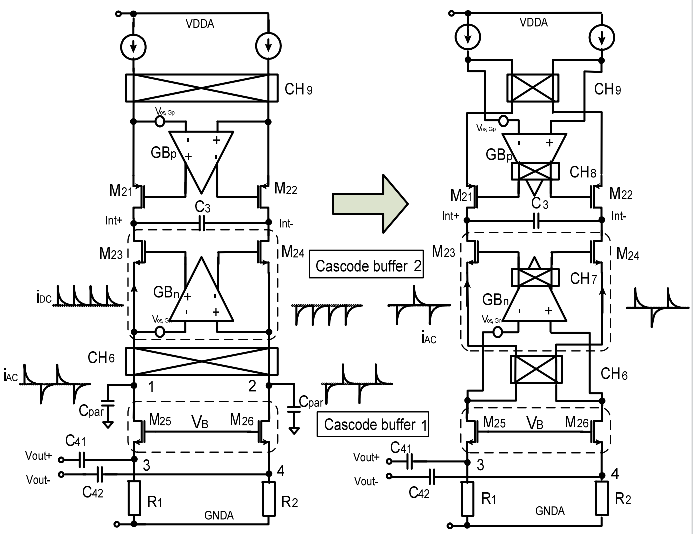

Figure 19.1.3: Implementation of the gain-boosted cascode buffer.

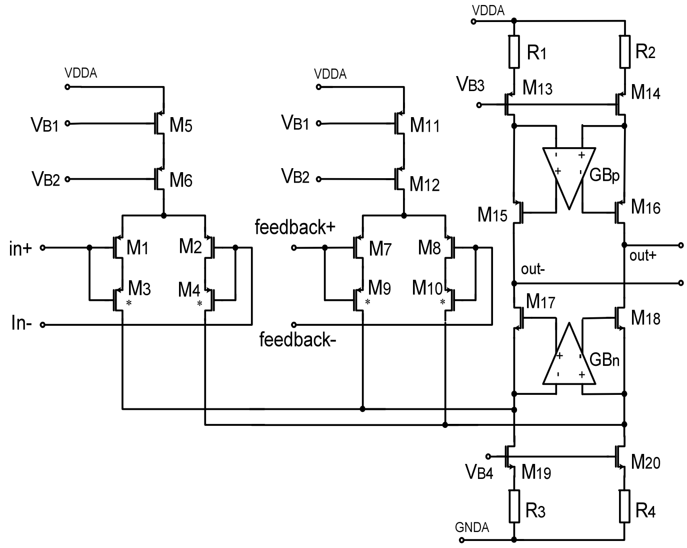

Figure 19.1.4: Schematic diagram of the first stage.

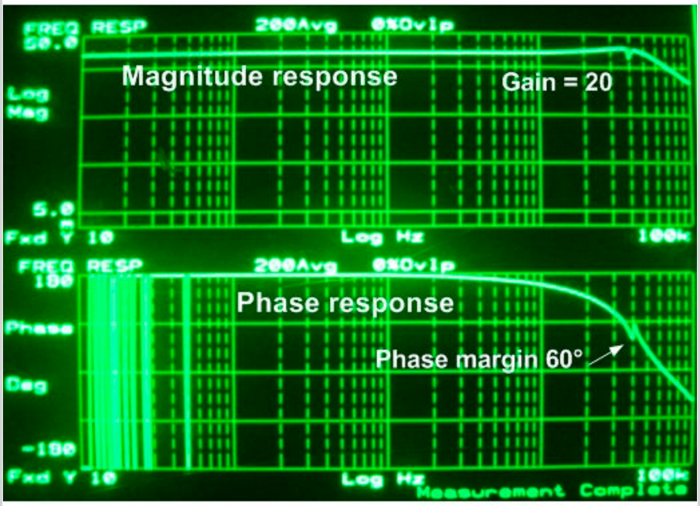

Figure 19.1.5: Frequency response of the CFIA at a gain of 20. (CFIA is stable for gains > 20, f_{ch1} = 40kHz, f_{ch2} = 510kHz).

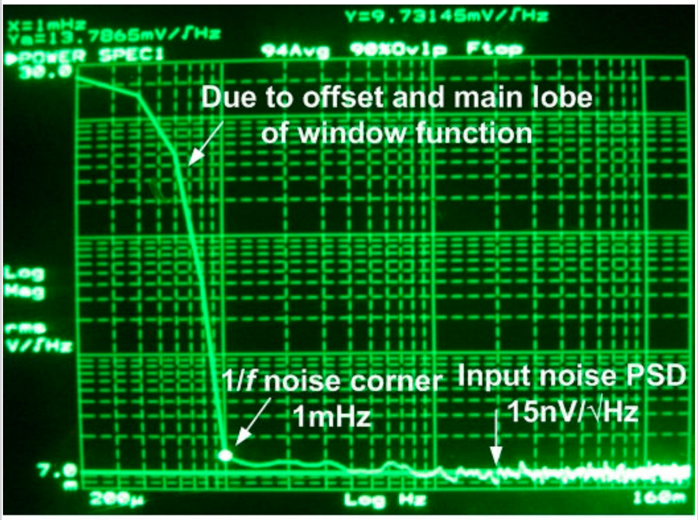

Figure 19.1.6: Output noise spectrum from 200μHz to 160mHz.

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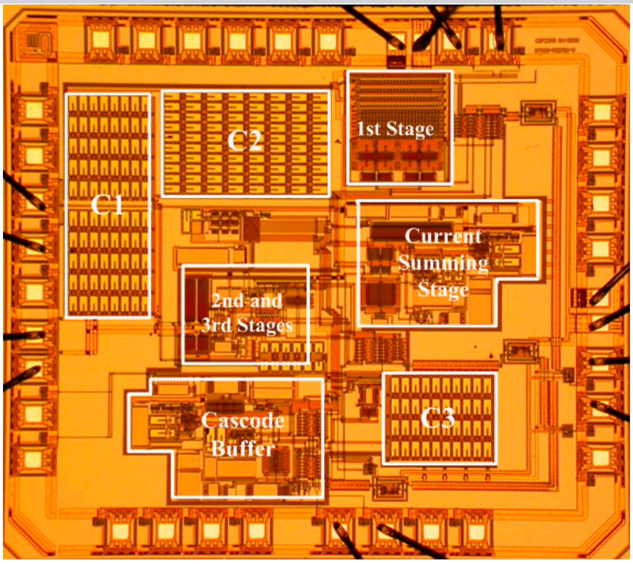

Figure 19.1.7: Chip micrograph of the current-feedback instrumentation amplifier.

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