20.2 An 8.5Gb/s CMOS OEIC with On-Chip Photodiode for Short-Distance Optical Communications

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Recently, low-cost silicon optoelectronic integrated circuits (OEICs) have been drawing attention for applications in short-distance optical communications such as chip-to-chip and board-to-board interconnects, LAN, data storage networks, etc [1-4]. Particularly, single-chip OEICs with on-chip silicon photodiodes provide a number of advantages including low cost, reduced ground-bounce, and bond-wire-induced coupling. Nevertheless, the slow response of silicon photodiodes in a standard CMOS process serves as a major bottleneck for high-speed communication [1]. To improve the bandwidth of silicon photodiodes, either some process modification or avalanche photodiode implementation has been developed. However, the former results in increased costs, whereas the latter has reliability issues. Although a differential photodiode configuration was originally proposed for bandwidth extension [2-4], the operation speed is still limited to several-hundred Mb/s. Meanwhile, the bandwidth can be extended by exploiting equalization filter [1, 3]. For relatively low-Gb/s operations, fixed equalization filter is sufficient, because photodiode responsivity is dominantly determined by diffusion currents which are not sensitive to process and temperature variations. For higher speeds, the responsivity becomes strongly dependent on the process and temperature variations, because it is mainly determined by the carrier mobility. Thereby, equalizers for high-Gb/s optical receivers require an adaptation algorithm to compensate the significant process and temperature variations. In this paper, an OEIC with on-chip photodiode is presented. Bandwidth and responsivity are compensated by a compact adaptive equalizer, thus achieving 8.5Gb/s operation.

Figure 20.2.1 shows the architecture of the OEIC receiver. It consists of an on-chip silicon photodiode, a regulated-cascode (RGC) TIA, a fixed equalization filter, an adaptive equalizer, a cascaded LA, and an output buffer. The on-chip silicon photodiode is realized in a differential configuration with n-well to p-substrate photodiode [2]. The RGC TIA is exploited to convert photocurrents from the silicon photodiode to mV-level voltage signals even under low supply voltages [5]. The large parasitic capacitance of the silicon photodiode limits the TIA bandwidth significantly, and therefore the first fixed equalization filter compensates the limited bandwidth of TIA. The adaptive equalizer, on the other hand, compensates the photodiode frequency response against the process and temperature variations. The LA consisting of 5 identical stages provides 6.9GHz bandwidth and 45dB gain. The offset cancellation network removes the offset voltages from the multi-stage equalizer and LA circuits.

The architecture of the adaptive equalizer is based upon the proposed slope-detection scheme that minimizes the difference of the slopes between the equalizer output and the LA output. Figure 20.2.2 shows the block diagram of the proposed slope-detection circuit and its operation principle. Here, each slope is detected by generating a fixed output current pulse while the input signal passes through the two fixed reference voltages, V_L and V_H. The difference of the two slope detectors' output is integrated by a capacitor, providing a control voltage, V_{ctrl}. This voltage controls the zero frequency of the variable equalization filter to form a feedback loop. Since faster edge-slopes result in smaller output charges, the control voltage V_{ctrl} either increases at under-equalization ($S_A<S_D$), or decreases at over-equalization ($S_A>S_D$). V_{ctrl} remains constant when S_A is equal to S_D.

The equalizer in this work is comprised of 8 equalization filters in cascade: the first 3 stages exist for the TIA equalization and the latter 5 stages for the photodiode equalization. Hence, the zero frequency of the equalization filters is fixed for the first 3 stages, while it is adjusted by the control voltage V_{ctrl} from the adaptation block for the latter 5 stages. The equalization filters use negative capacitance (NC) circuits to enhance the high-frequency gain [6]. Figure 20.2.3 depicts the schematic diagram of a single gain-cell of the LA, where the proposed negative resistance-capacitance (NRC) circuit is used to increase both the output resistance and the bandwidth, simultaneously. Small-signal analysis shows that the equivalent impedance (Z_{NRC}) of NRC circuit is modeled as a parallel combination of 3 negative resistors and a capacitor. Therefore, the LA can enhance the DC-gain by the negative resistance (NR) in parallel to the amplifier output resistance, yielding very high output resistance. Simultaneously, the bandwidth is extended by cancelling out the load capacitance with the parallel NC. HSPICE simulations reveal that the proposed LA achieves 20dB voltage gain enhancement and 35% bandwidth extension, when it is compared with a conventional LA without NRC.

Figure 20.2.4 shows the dependency of the bandwidth upon temperature for both the photodiode and the whole receiver (including PD+TIA+EQ). It is clearly seen that the equalization maintains the bandwidth variation within 7.8% even in the range of -40°C to 80°C, while the photodiode itself shows the bandwidth variation of 44%.

The OEIC is fabricated in a 0.13μm CMOS process. The on-chip photodiode consists of 6 fingers with minimum spacing, and occupies the area of 70×70μm^2. The photodiode parasitic capacitance is about 3pF. Figure 20.2.5 demonstrates the measured eye-diagrams for 2^{31}-1 PRBS optical signal at different data rates of 2.5Gb/s, 4.25Gb/s, and 8.5Gb/s, respectively. In order to verify the bandwidth enhancement due to equalization, Fig. 20.2.5(a) shows the output eye-diagram when the equalizer is forced to operate with minimal equalization by the external control signal. The rms jitter of the output eye-diagrams is measured to be 7.6ps for 8.5Gb/s signal. The optical sensitivity is measured to be -3.2dBm for 10^{-12} BER at 8.5Gb/s operation. The chip consumes 47mW (excluding output buffer) from a single 1.5V supply. Figure 20.2.6 shows the chip micrograph of the proposed OEIC

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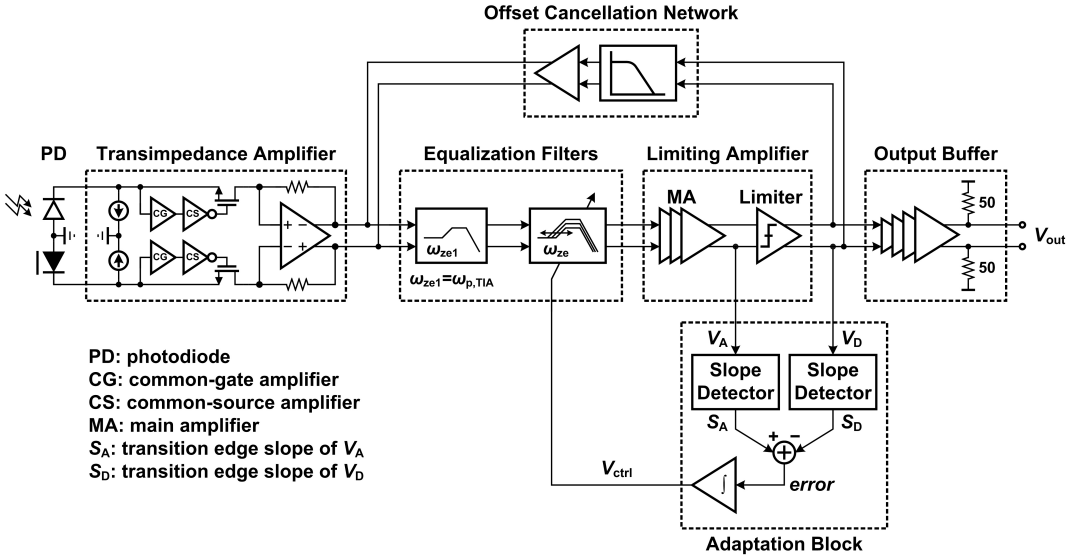

Figure 20.2.1: Architecture of the proposed OEIC receiver.

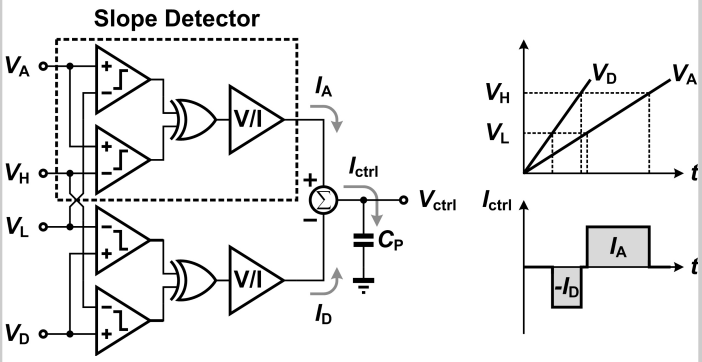

Figure 20.2.2: Block diagram and operation principle of the adaptation circuit.

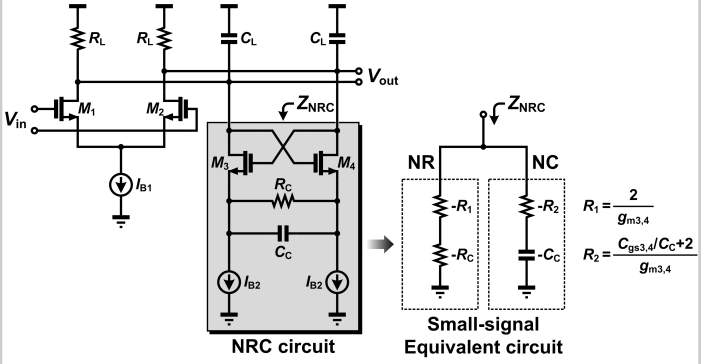

Figure 20.2.3: Schematic diagram of the LA gain cell.

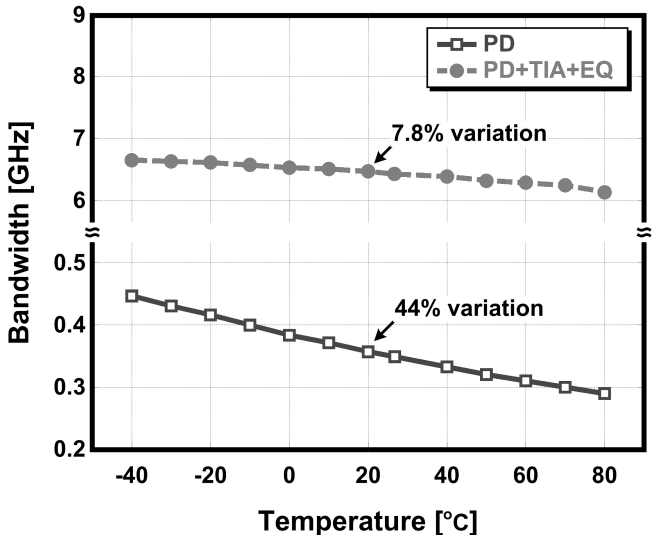

Figure 20.2.4: Bandwidth dependence upon temperature for the silicon photodiode (from device simulations) and for the proposed receiver.

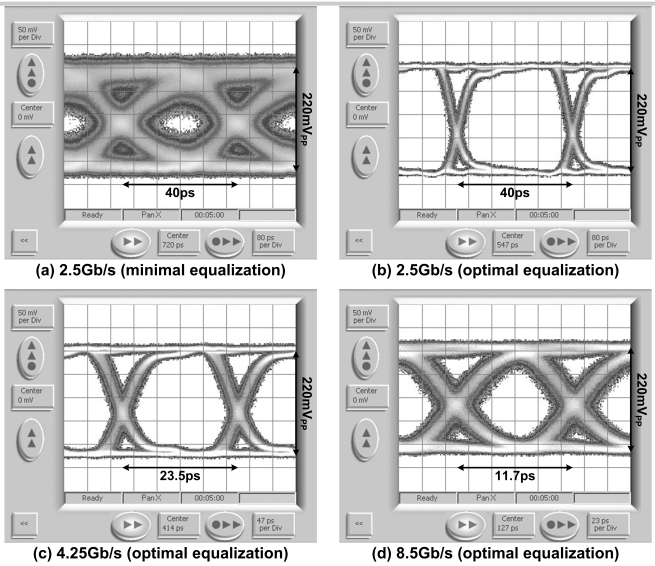

Figure 20.2.5: Measured eye-diagrams for 2^{31}-1 PRBS at different data rates.

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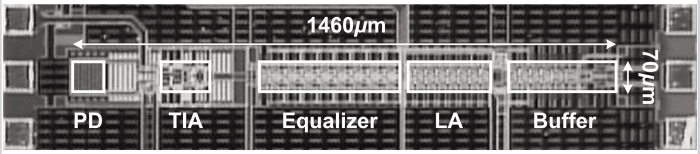

Figure 20.2.6: Chip micrograph.

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