13.5 A 4-Antenna-Path Beamforming Transceiver for 60GHz Multi-Gb/s Communication in 28nm CMOS

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Millimeter-Wave transceivers with beamforming capabilities, such as the one presented in this work, are a key technology to reach 4 or 6Gb/s at 10m range with the IEEE 802.11ad standard. Moreover, for mm-Wave access in 5G it will also be necessary to boost peak data-rates far beyond 1Gb/s at hundreds of meters in small cells. Transceiver architectures with beamforming often combine superheterodyne with RF beamforming [1], leading to a high power consumption and a suboptimal RX noise figure due to losses in the beamforming circuitry. In contrast, the 57-to-66GHz TRX IC presented in this paper, whose architecture is depicted in Fig. 13.5.1, uses direct conversion and analog baseband beamforming. Direct-conversion radios are inherently simpler than superheterodyne and do not have to cope with the image frequency, but on the other hand they may suffer from pulling of the PA on the VCO. In this work this is avoided by the non-integer ratio of 2.5 between the operating frequency and the 24GHz PLL that subharmonically injection locks a 60GHz quadrature oscillator (Fig. 13.5.2).

The 24GHz integer-N PLL can operate with a PFD and a charge pump with programmable current (classical mode) and also in subsampling mode (SS in Fig. 13.5.2) to eliminate charge-pump noise [4]. A divide-by-two at the VCO output generates a 12GHz quadrature signal that is fed via a chain of inverters to a 5× injection-locked quadrature oscillator (QILO); a ring oscillator between the two ILOs improves quadrature accuracy. Each ILO has a 4b binary- weighted capacitance array that covers the whole PLL operating frequency range. The ILO locking range is larger than 3GHz, which guarantees a robust lock condition.

The VCO has a tuning range from 21.5 to 26.4GHz by means of analog tuning and a digitally controlled capacitor array. The worst-case phase noise, translated to 60GHz and measured over the 4 802.11ad channels, is -93.3dBc/Hz and -117dBc/Hz at 1MHz and 10MHz offsets respectively. The PLL loop bandwidth is adjustable between 100kHz and 1MHz. In combination with the common phase-error removal in the digital domain, which suppresses close-in phase noise, the best EVM performance is obtained with the minimum PLL loop bandwidth. The output of the QILO is fed into the LO buffering that drives all IQ mixers for the RX and TX signal paths. The two layers of LO buffers in Fig. 13.5.2 are pseudo-differential pairs loaded with transformers and the transmission lines that bridge the distance with the mixers. The LO swing is programmable and at maximum swing the whole LO buffering consumes 98mW.

A transformer at the input of the RX converts the signal to differential and provides more than 1kV HBM ESD protection. Since a low power consumption in the circuitry before signal combination is crucial as this is replicated over the antenna paths, a current-reuse 2-stage differential LNA topology is used, as shown in Fig. 13.5.3. It only consumes 18mW that compares favorably with other multistage LNA designs [1-3]. The passive downconversion mixer drives a variable-gain baseband amplifier with DC offset compensation at its output. The beamforming at analog baseband is based on a Cartesian vector modulator with 20 parallel digitally controllable transconductors for I and Q, resulting in less than 5 degrees phase resolution and less than 1dB gain variation. In contrast with RF beamforming, analog baseband beamforming decouples the phase shift from the RF frequency and can easily achieve constant amplitude response versus phase. A second-order gm-C filter rejects the adjacent channel and out-of-band noise after beamforming. The 4 paths are then combined in two layers (Fig. 13.5.1 bottom) with identical variable-gain amplifiers with DC offset compensation. Two more of the same stages are used after combination to extend the gain range. Finally, a push-pull buffer implemented with 1.8V devices drives an off-chip 100Ω differential load while consuming 77mW. The maximum measured RX gain is 62dB with a baseband bandwidth of 880MHz and an output compression point around 1dBm.

At the transmitter side the baseband signal is split over the 4 antenna paths. To drive the large capacitive load due to the long interconnects to the 4 paths and the 4 phase shifters with more than 1GHz bandwidth and a 0dBm output 1dB compression point, the combination of a source follower and a flipped source follower shown in Fig. 13.5.2 is implemented with 1.8V devices (4 of these drivers are used for I/Q differential signals). Fine control of the DC output voltage for offset compensation with 1.6mV step is obtained by acting on the bulk of the diode-connected device in the bias branch. At the output of the baseband phase shifters DC offset can be further compensated to minimize LO feedthrough for each antenna path. In the mm-Wave part an active IQ mixer is followed by a 2-stage PA, each stage realized with push-pull common-source circuits with transformer load and cross-coupled capacitive neutralization (Fig. 13.5.2). An envelope detector is connected to the output and can be used to calibrate LO feedthrough and IQ imbalance. The entire TX chain has a measured conversion gain of 32dB. The measured baseband bandwidth, partially constrained by the measurement setup, is more than 1GHz.

A micrograph of the 7.9mm^2 TRX chip implemented in 28nm CMOS is shown in Fig. 13.5.7. The die is flip-chip assembled on the back of a module in a 12-layer board technology. The front of the module hosts 4 pairs of patch antennas. Each pair is connected to either a TX or an RX antenna path, resulting in either a 4TX or a 4RX module. The antenna array is designed for beam steering in an azimuth scan range from -45° to 45° and an elevation scan range from -30° to 30°. The measured broadside gain of the module arrays is close to 12dBi for the entire 60 GHz band.

For electrical test purpose, a second module where antennas are replaced with GSG pads for probing is used. The entire RX consumes 431mW (excluding the 77mW of the 100Ω drivers). The noise figure, measured for a single antenna path and including 0.5dB transition loss on the module, is lower than 6.2dB over the four 802.11ad channels at maximum gain, as reported in Fig. 13.5.3. After compensation, the residual DC offset at the RX output is less than 10mV. The RX sensitivity level for 16QAM (MCS12 mode from 802.11ad) of one antenna path is -57dBm.

The TX consumes 670mW with a measured output compression point higher than 7.5dBm. After calibration, the LO feedthrough is below -32dBc and the image rejection is better than 38dB. The measured TX EVM for single-carrier (SC) QPSK and 16QAM is better than -21dB in the 4 channels, which meets the 802.11ad requirements. The power spectrum of the TX output meets the 802.11ad spectral mask, as shown in Fig. 13.5.4.

Beamforming is tested with a horn antenna. Figure 13.5.4 shows the relative RX and TX gain as a function of a variable phase shift: antenna paths 1 and 4 are kept at a constant phase while antenna paths 2 and 3 are set to the variable phase shift. The measured antenna patterns are also shown in Fig. 13.5.4 as a function of 1, 2 and 4 antennas; directivity and/or power increase as the number of activated antennas increases. The measured EIRP of the module is larger than 24dBm in all four 802.11ad channels.

A TX-to-RX link has been established at a distance of 1m. An arbitrary waveform generator generates the TX analog baseband input and an oscilloscope digitizes the RX analog baseband output. The measured TX-to-RX EVM is better than -20dB in the 4 channels for the standard QPSK and 16-QAM modulations as well as for the SC-64QAM (not foreseen in the standard), as from the constellations shown in Fig. 13.5.5.

The table of comparison with prior art in Fig. 13.5.6 shows that this work has a lower overall TRX power consumption and the TX has the highest EIRP normalized to the DC power consumption.

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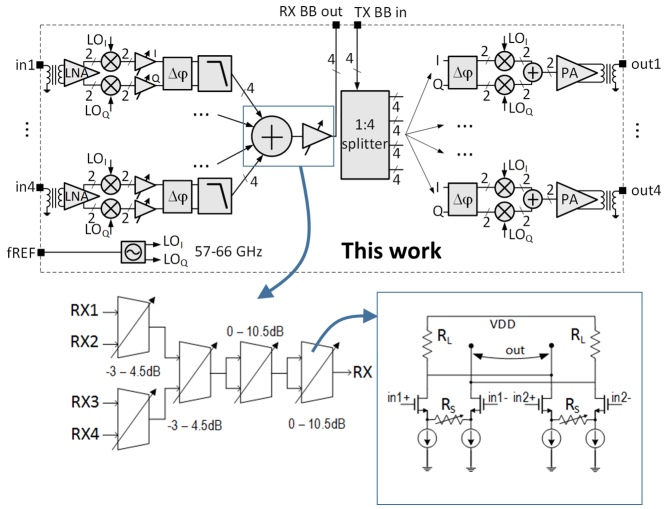


Figure 13.5.1: 4-antenna RX and TX beamforming architectures (top), signal combination and variable gain at baseband RX (bottom left) with gain range indicated; (bottom right) simplified schematic of the VGA.

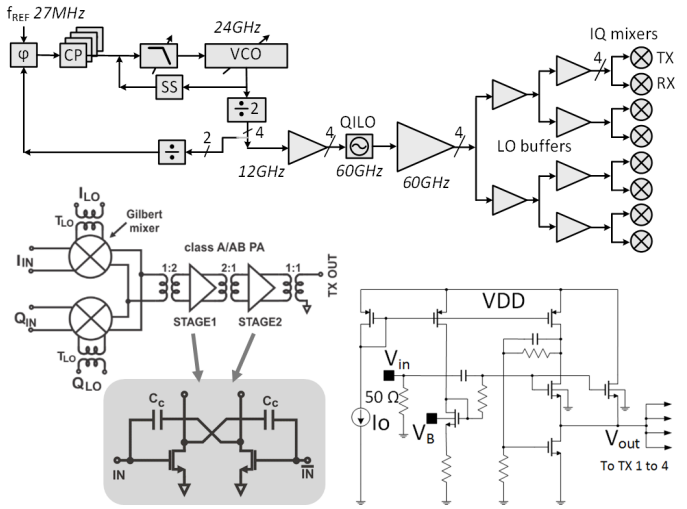


Figure 13.5.2: LO architecture (top). TX front-end with PA active cell (bottom left). Schematic of the splitter at the TX input (bottom), where four splitters are used for I/Q differential signals.

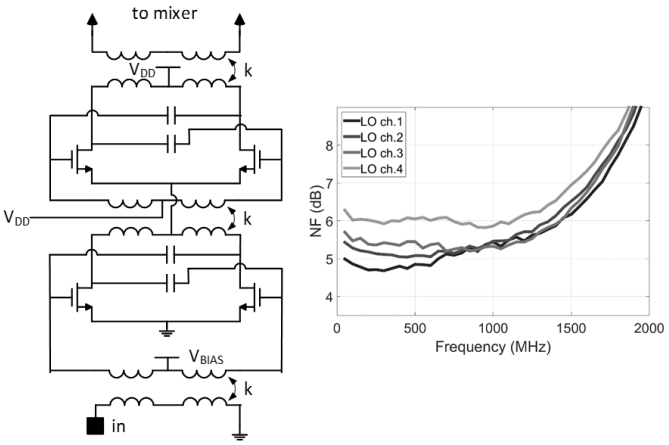


Figure 13.5.3: LNA schematic (left), and (right) measured NF of one complete RX antenna path for the four IEEE 802.11ad channels.

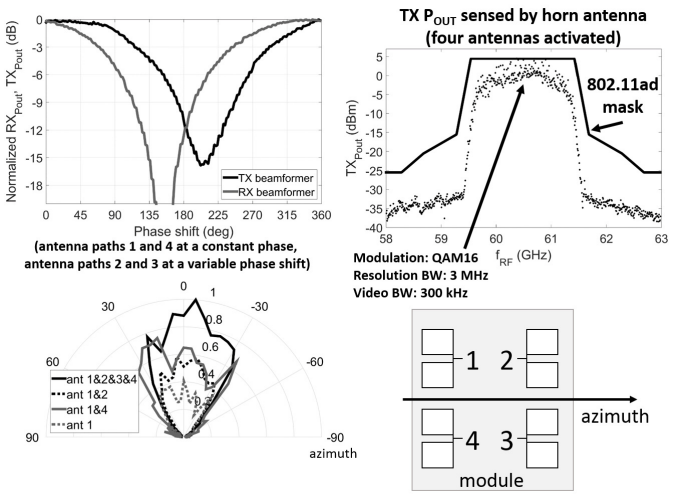
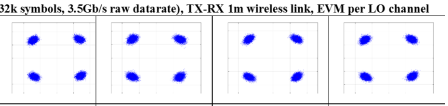


Figure 13.5.4: Measurement results on TX and RX: normalized RX POUT and TX POUT vs. phase shift; TX spectral mask at P_{1dB}-5dB; TX antenna pattern over azimuth; antenna's location with respect to azimuth.

QPSK (32k symbols, 3.5Gb/s raw datarate), TX-RX 1m wireless link, EVM per LO channel

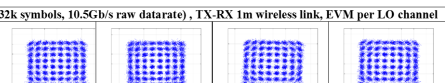


Channel	1 – 58.32 GHz	2 – 60.48 GHz	3 – 62.64 GHz	4 – 64.8 GHz
TX EVM *	-22.3 dB	-22.7 dB	-21.4 dB	-21.9 dB
EVM	-20.3 dB	-20.1 dB	-20.6 dB	-20.3 dB
BER	Not detectable	Not detectable	Not detectable	Not detectable

16QAM (32k symbols, 7Gb/s raw datarate) , TX-RX 1m wireless link, EVM per LO channel

Channel	1 – 58.32 GHz	2 – 60.48 GHz	3 – 62.64 GHz	4 – 64.8 GHz
TX EVM *	-22.6 dB	-21.6 dB	-22.3 dB	-21.0 dB
EVM	-20.2 dB	-20.0 dB	-20.2 dB	-20.4 dB
BER	Not detectable	2.6×10^{-5}	3.5×10^{-5}	7.0×10^{-5}

64QAM (32k symbols, 10.5Gb/s raw datarate) , TX-RX 1m wireless link, EVM per LO channel



Channel	1 – 58.32 GHz	2 – 60.48 GHz	3 – 62.64 GHz	4 – 64.8 GHz
EVM	-20.9 dB	-20.4 dB	-20.5 dB	-20.7 dB
BER	6.4×10^{-3}	9.1×10^{-3}	8.7×10^{-3}	7.1×10^{-3}

* Including a waveguide-based reference receiver. The TX EIRP is 24 dBm.

Figure 13.5.5: TX-to-RX constellation diagrams and EVM values. The frame length limits the minimum detectable BER.

	This work	[1] ISSCC '14	[2] ISSCC '13	[3] ISSCC '14	[5] JSSC '15
Technology	28 nm CMOS	40 nm LP CMOS	40 nm LP CMOS	65 nm CMOS	130 nm SiGe BiCMOS
Supported channels	4	4	3	Bonding	4
Architecture	Direct conversion	Superhet.	Direct conversion	Direct conversion	Direct conversion
Frequency synthesis	Sub. inj. locking	Superhet.	Fundamental PLL	Sub. inj. locking	Fundamental PLL
Beamforming	4-way, BB	16-way, RF	4-way, BB	Not present	Not present
Integration	RF, LO, analog BB	RF, LO, IF ****	RF, LO, analog BB	RF, LO, analog BB	RF, LO, analog BB
EIRP (dBm)	+24 (4 antenna)	+24 (16 antenna)	N. A.	N. A.	14 (QPSK) 10.4 (16-QAM)
TX conversion gain per antenna path (dB)	32	N.A.	31	15	23
RX conversion gain per antenna path (dB)	62	N.A.	45	> 20	72
NF (dB)	4.8-6.2 * (whole antenna path)	< 10 **	5.5	N.A.	3 - 5
TX EVM (dB)	< -21 ***	< -23	N.A.	< -27 (1 ch.) -20 (ch. bonding)	-25
TX-to-RX EVM (dB)	< -20	< -22	< -13.1	-26	-20.5
PDC TX (mW)	670 (class A) 546 (class AB) (4 antenna)	1190 **** (16 antenna)	584 (4 antenna)	251 (1 antenna)	720 (1 antenna)
EIRP(mW)/PDC$_{TX}$ ×100	**37% (class A, 4 antenna)**	**26% **** (16 antenna)**	N.A.	N.A.	3.5%
PDC RX (mW)	431 (4 antenna)	960 **** (16 antenna)	496 (4 antenna)	220 (1 antenna)	340 (1 antenna)

* It includes the transition from the module to the silicon chip. This transition has a simulated loss of 0.5 dB.
** The receiver NF is better than 10 dB including 2 dB loss from the DPDT switch (from Boers, JSSC, vol. 49)
*** Including a waveguide-based reference receiver.
**** RF chip only/ BB chip not included.

Figure 13.5.6: Comparison to state-of-the-art.

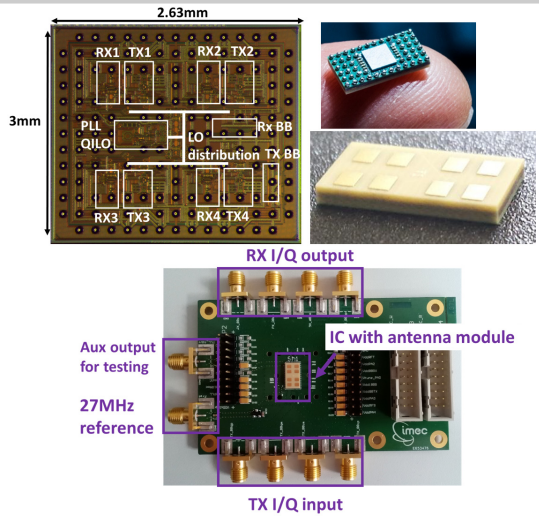


Figure 13.5.7: Die micrograph. Die mounted on the antenna module. Module: front side with patch antennas (two patches for each of the four antenna paths) and I/O connections.

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