26.6 A 1.4ps$_{rms}$-Period-Jitter TDC-Less Fractional-N Digital PLL with Digitally Controlled Ring Oscillator in 65nm CMOS

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State of the art digital PLLs can be divided in two categories, depending on the implementation of the digital phase detector. Digital clocking and wireline applications mostly use a Bang-Bang detector (BBPLLs) [1-3], offering very low jitter values in integer-N mode but not supporting fractional-N synthesis, which is desirable to implement, i.e., spread spectrum clocking (SSC) for EMI reductions. Wireless applications implement time to digital converters (TDC) [4-6] which allow fractional-N synthesis, but require high architecture complexity, need calibration routines for period normalization, and introduce analog limitations that a digital PLL should be intended to eliminate.

This paper introduces a digital PLL architecture, which, in order to reduce the phase quantization error without a traditional TDC, exploits the multiphase output of a 3-phases digitally controlled ring oscillator (DCRO) providing built-in period normalization and a quantization error which is an exact known fraction of the output clock period. To cope with the poor supply noise rejection of CMOS inverters, the DCRO is supplied by a low drop out (LDO) regulator, with a distributed architecture allowing an extended frequency range without area penalty.

The block diagram of the PLL is shown in Fig. 26.6.1. It consists of the DCRO with fine- and coarse-tuning inputs, a $\Delta\Sigma$ modulator (DSM), a phase quantization block (PQ) and a digital core, which includes a phase detector (PD) and a loop filter (LF).

The 3 clock phases (CLKD<2:0>) are used in the PQ to determine the phase information, which is subtracted from the accumulated frequency control word (FCW) in the PD. The resulting phase error is filtered by the LF, which includes a proportional and an integral path (PI) with programmable factors. The LF produces a 4-bit word for coarse tuning and a 15-bit oscillator tuning word (OTW). The 5 LSBs of the OTW are delivered to a 1st order DSM, which dithers the LSB of the DCRO for higher frequency resolution. The DSM runs on a divided version of CLKD (division factor 2^M, M programmable from 1 to 8). Additionally, a digital generator adds a programmable waveform to the FCW in order to provide SSC modulation.

The coarse tuning of the DCRO is done in closed-loop operation. The OTW is set to a fixed value, and the PLL controls the coarse tuning input of the DCRO while operating in a pure proportional mode. After the PLL has locked, the coarse tuning values are frozen, the LF switches to PI mode, and the PLL then re-locks by controlling the fine tuning of the DCRO.

In contrast to [4], in this PLL the TDC is replaced by a mechanism inside the PQ, which provides the fractional phase information (Fig. 26.6.2). The PQ consists of a CLKD cycle counter and a phase sampler. In order to avoid metastability FREF is re-synchronized to CLKD. The resulting CLKR is used as a system clock for the digital core and to sample the DCRO cycle counter.

The CLKD cycle counter determines the integer number (PQ_{int}) of CLKD cycles during one CLKR cycle. The fractional information (PQ_{frac}) is determined inside the phase sampler by sampling the 3 CLKD phases with FREF. By analyzing the sampled pattern, it is possible to identify the position of FREF within the period of CLKD, with a resolution of 1/6 of a CLKD cycle (Fig. 26.6.2).

Duty cycle distortion (DCD) and phase mismatch (PM) of the DCRO phases generate spurs in fractional-N mode. However, practical values of DCD and PM do not impact the output period jitter.

For further improvement of the jitter performance, in case of integer-N channels, an offset of 1/12 is added in the PD, which lets the PLL act as a BBPLL.

The architecture of the DCRO (Fig. 26.6.3) consists of 3 sections. A 3-stages CMOS inverter top ring which is always on, a coarse-tuning block including 9 3-stages CMOS inverter rings connected in parallel, and a fine-tuning block composed by a matrix of 15 x 18 CMOS tri-state inverters (unity cells) which are enabled using a scheme similar to that presented in [2], allowing 270 frequency settings.

An efficient low-power and high-resolution fine tuning matrix is a trade-off between number of cells and associated wiring parasitic capacitance. To overcome this limitation, this DCRO includes 3 independently enabled tri-state inverters whose size is half that of the unity cells, so that a total of 540 frequency steps are available for each coarse setting, without area and power penalty. Furthermore, 3 independent tri-state half-size inverters for frequency dithering are included.

The fine tuning scheme in principle introduces a deterministic phase mismatch since the load and driving strength of the 3 phases is not always identical. However, the mismatch is negligible and not practically affecting the jitter. For instance, a frequency step of 3MHz operated by 1 phase only while the DCRO is oscillating at 3GHz gives a phase mismatch of 0.33ps.

In the distributed LDO (Fig. 26.6.3), a single error amplifier controls 9 local output devices, one for each ring in the coarse section. These devices are used to perform 1.0V voltage regulation and switching function (like the top-device of a tri-state inverter) at the same time. This structure increases the driving strength of the coarse ring by reducing the number of the stacked transistors from 4 to 3 in the inverter cells. One additional output device supplies the fine matrix and top ring (like in a conventional scheme LDO).

The design is fabricated in a standard low power 65nm CMOS technology. The active area of the circuit (without JTAG) is 190x200μm^2. The JTAG occupies an area of 190x40μm^2. In all measurements the reference clock frequency is 25MHz, the supply of the LDO is set to 1.3V, while the rest sits on a 1.1V supply.

The measured DCRO tuning curves and DNL plot are shown in Fig. 26.6.4, together with current consumption of the DCRO alone (without LDO) and K_{DCRO} values. The tuning range goes from 190 to 4270 MHz, and the DCRO consumes 2.1mA at 1GHz, 3.7mA at 2GHz and 5.7mA at 3GHz, independent from the coarse tuning selected.

For digital clocking applications an important figure of merit is the peak-to-peak (pp) period jitter. Values of jitter and current consumption are shown in Fig. 26.6.5, together with a histogram of the period showing a Gaussian distribution in fractional-N mode. At 3GHz the current consumption of the whole PLL is 9.3mA and the period jitter is 1.4ps$_{rms}$ and 15ps$_{pp}$, both in integer and fractional mode. At 375MHz the PLL consumes 2.65mA, with a period jitter of 8.4ps$_{rms}$ and 75ps$_{pp}$. The power dissipation depends linearly on the output frequency with a slope of 3.3mW/GHz and an initial offset of 1.85mW. The power figures are substantially lower than already published DCRO implementations [2],[7].

Figure 26.6.6 shows the spectrum of the output clock at 3GHz in integer and fractional-N mode with SSC enabled. The SSC parameters are typical for serial communication links.

Figure 26.6.7 shows the chip micrograph and the layout of the active area.

Acknowledgements:
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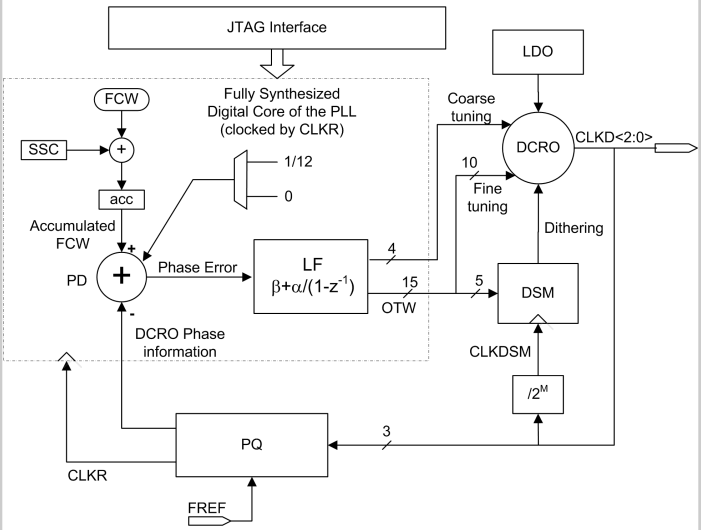


Figure 26.6.1: Block diagram of the PLL.

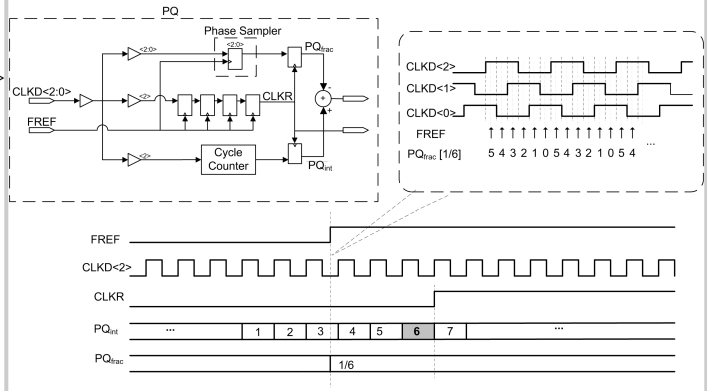


Figure 26.6.2: Block diagram and timing of the phase quantizer (PQ).

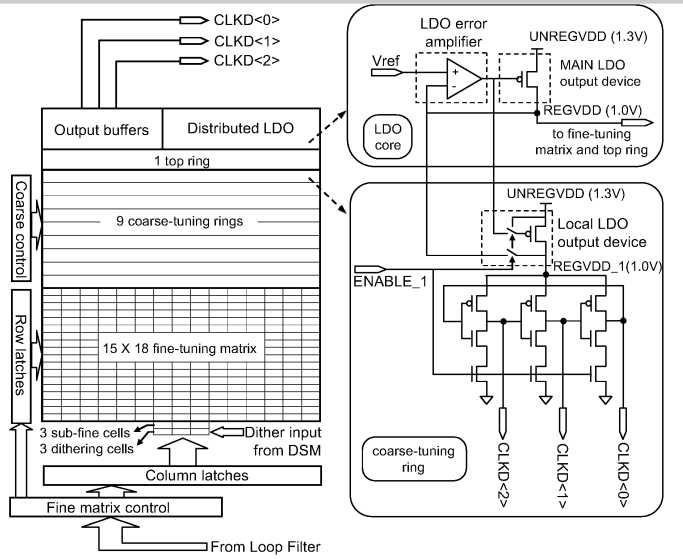


Figure 26.6.3: Architectures of the DCRO and distributed LDO.

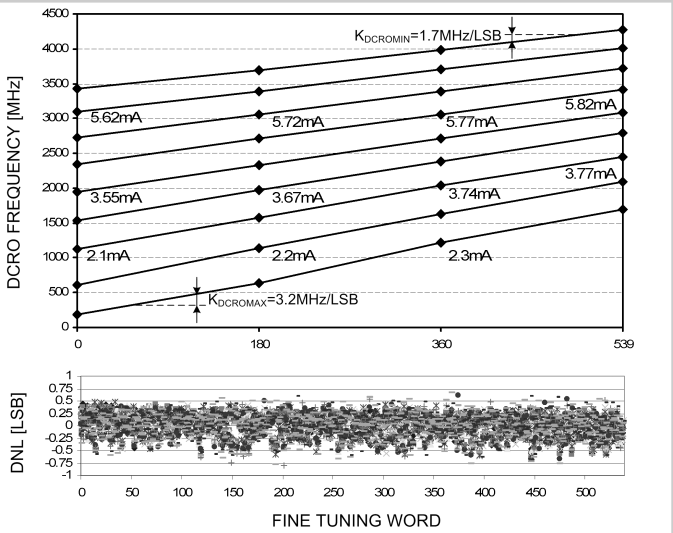
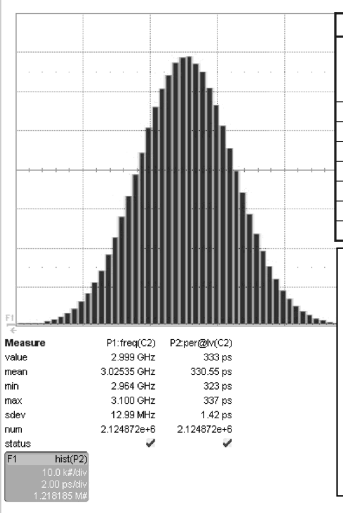


Figure 26.6.4: DCRO tuning curves and DNL. Labels indicate DCRO current consumption, maximum and minimum DCRO gain.



Period jitter and current consumption

Freq [GHz]	Jp(rms) [ps]	Jp(pp) [ps]	Current of DCRO + LDO [mA]	Current of Dig.Core + PQ + DSM [mA]
3	1.45	15	6.8	2.5
3.0253	1.42	15		
1.5	3.75	38	3.8	1.5
1.5018	3.88	40		
0.75	4.84	50	2.4	1
0.751575	5.51	54		
0.375	8.16	75	1.9	0.75

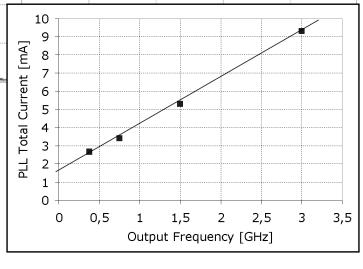


Figure 26.6.5: Histogram of the clock period at 3025.35MHz, jitter and power consumption values in different modes.

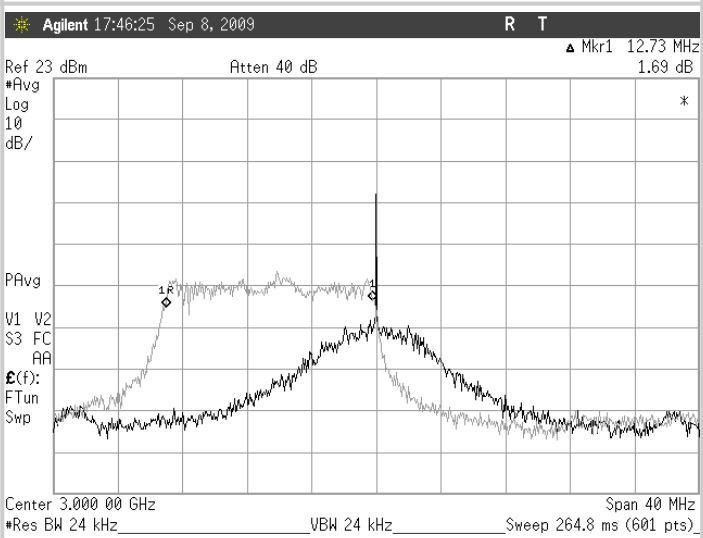


Figure 26.6.6: Spectrum of the 3 GHz output in integer-N mode and fractional-N mode with SSC (33kHz modulation).

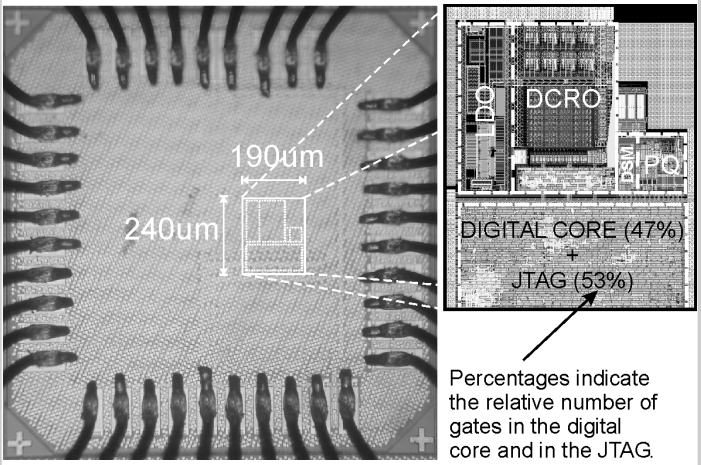


Figure 26.6.7: Die micrograph of the PLL with layout.

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