An 802.11ba 495µW -92.6dBm-Sensitivity Blocker-Tolerant Wake-up Radio Receiver Fully Integrated with Wi-Fi Transceiver

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***Abstract*—An 802.11ba-based wake-up radio (WUR) receiver is presented. The WUR receiver prototype is integrated within an 802.11a/b/g/n/ac Wi-Fi transceiver, occupying 0.05mm² for RF/analog frontend and 0.08mm² for digital baseband. The WUR receiver consumes 495µW standalone and consumes 667µW from Wi-Fi system supply. The receiver has a measured sensitivity of -92.6dBm and can tolerate -40.5dBm Wi-Fi adjacent channel blocker with 3dB receiver de-sensitization. The WUR receiver can operate when the Wi-Fi system is in sleep mode and can turn on Wi-Fi radio upon receiving 802.11ba-based wake-up packet over the air.**

***Keywords*—802.11ba, wake-up radio, Wi-Fi**

I. Introduction

IEEE 802.11 standard based Wi-Fi is the most widely adopted connectivity solution. However, its unscheduled nature means there exists a fundamental trade-off between low-power and low-latency operations. This limitation of Wi-Fi presents significant challenges not only for achieving low-power always-connected systems, such as wireless sensor networks and Internet of Things, but also for reducing power consumption and latency for next generation Wi-Fi system for mobile/laptop platforms. To overcome this, an event-driven low power wake-up radio (WUR) can be added for monitoring the wireless channel. WUR would turn on the Wi-Fi radio only upon receiving wake-up message, thereby achieving both low power and low latency. In December 2016, a task group was formed for IEEE 802.11ba (TGba), aiming to standardize the WUR operation within IEEE 802.11 standard.

Various non-standard based WUR solutions have been proposed in 2.4GHz/5GHz bands [1-4], however, they all have major shortcomings for future Wi-Fi chip integration. Off-chip high-Q inductors are required for achieving high WUR sensitivity in [1-2] and >1mm² silicon area for RF/analog frontend is needed in [2], both obstructing WUR receiver adoption in Wi-Fi chip. In [2-3], for achieving low WUR power consumption, ultra-low voltage supply for major power consuming blocks is used. However, the power could quickly expand after system integration once supply efficiency is factored in. In [4], although no off-chip component and no low-voltage supply is needed, its sensitivity and blocker tolerance is not sufficient for the WUR replacing legacy Wi-Fi wake-up mechanism without significant loss of communication range and quality.

In this paper, we present a first-ever prototype of an 802.11ba-based WUR receiver design as well as monolithic integration of WUR and Wi-Fi transceiver to demonstrate the technology. The presented WUR receiver prototype can achieve sensitivity and blocker tolerance performance close to Wi-Fi chips [5] for comparable communication range and quality while consuming only 495µW standalone and 667µW from the switching supply in a Wi-Fi system. Moreover, the WUR only occupies 0.05mm² for RF/analog frontend and 0.08mm² for digital baseband (DBB) without requiring external components, which is crucial for the adoption of WUR in next generation Wi-Fi chips.

II. 802.11ba Wake-Up Radio

802.11ba is an amendment to the 802.11 standard currently in development by TGba, with a goal to standardize the WUR operation and achieve less than 1mW WUR receiver active power and low latency for Wi-Fi devices. Based on TGba Draft 1.0 [6], the 802.11ba utilizes multi-carrier-on-off-keying modulation scheme (MC-OOK). The MC-OOK uses the center 13 OFDM subcarriers among 64 total subcarriers within a 20MHz Wi-Fi channel, thus occupying 4MHz bandwidth. For a mandatory 62.5kbps PHY rate, each MC-OOK symbol is 2µs for the WUR preamble and 4µs for the WUR data field with each WUR data bit represented by 4 MC-OOK symbols with 1/4 rate Manchester-coding. A WUR packet starts with legacy 802.11 preamble to provide coexistence between the legacy 802.11 and new 802.11ba devices. The 802.11 preamble is followed by MC-OOK based WUR preamble for packet acquisition and then WUR data field. An example of 802.11ba signal is shown in Fig. 1(a).

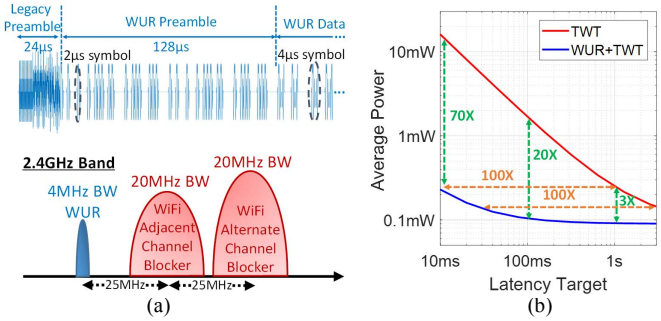


Fig. 1 (a) 802.11ba WUR signal overview in time and frequency domain; (b) TWT vs. WUR+TWT for average power and latency

802.11ba also supports duty-cycled WUR operation, allowing WUR receiver to power on and off periodically to save even more power. The WUR duty-cycle can be scheduled according to a target-wake-time (TWT) schedule. TWT is a power saving feature adopted in 802.11ah/ax, where the 802.11 station (STA) turns on Wi-Fi radio to receive data from the access point (AP) at a pre-negotiated wake-time after sleep, regardless whether there is buffered data in AP to be transferred or not. When WUR is used together with TWT, the STA only needs to turn on the WUR receiver at the schedule wake-time and only wakes up Wi-Fi radio if needed based on the received WUR packet. Fig. 1(b) shows latency target versus the average system power consumption when there is no buffered data in AP. The system power is estimated from 802.11ax power consumption model in [7] and WUR is assumed to consume 667µW active power and be active for 2ms in each TWT interval (which is also latency target). As shown in the figure, up to two orders of magnitude improvement on average power or latency can be achieved by having WUR with TWT versus TWT alone.

III. WUR Implementation and Wi-Fi Integration

For WUR and Wi-Fi system integration, the WUR receiver needs to achieve not only low power operation, but also compact area. Fig. 2 shows a block diagram of the proposed 802.11ba-based WUR receiver. A mixer first architecture was adopted for the WUR [4]. The double balanced (DB) mixer is followed by an interleaved dynamic amplifier, which significantly improves gain and noise figure by virtue of common gate–common source (CG-CS) coupling. To achieve similar blocker tolerance of the main Wi-Fi radio, an overall 4th order baseband filtering was designed for WUR by adding another 2nd order bi-quad filter. Meanwhile, an LC-VCO is also adopted for providing sufficient phase noise performance. The LC-VCO is embedded within a frequency lock loop (FLL) which provides sufficient frequency accuracy for the MC-OOK demodulation while only using a 32.768kHz RTC reference. The RF/analog frontend is followed by a 7-bit asynchronous SAR ADC and an 802.11ba-based DBB. Integration scheme for WUR and main Wi-Fi radio is also shown in Fig. 2. The WUR RF inputs directly tap on the Wi-Fi receiver inputs. A 1.1V switching supply from system platform is used as the main power source, with micro-LDOs designed for WUR internal supplies.

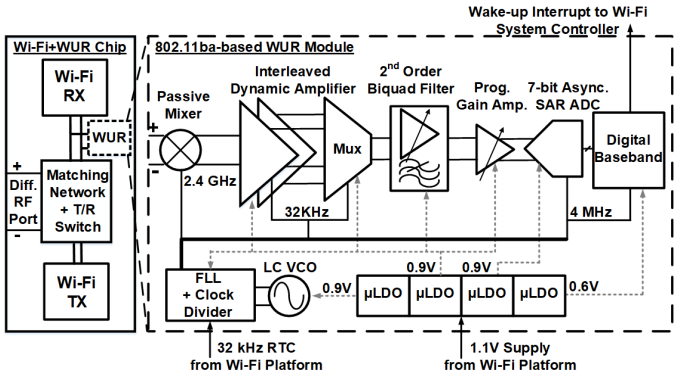


Fig. 2 WUR architecture and Wi-Fi chip integration diagram

A. RF/analog Frontend

Minimizing the device sizes in the passive mixer is vital for lowering overall WUR power. However, this increases the noise of zero IF receiver chain. To reduce the noise figure (NF) while keeping low power consumption for signal amplification chain, a novel mixer-embedded dynamic baseband low noise amplifier (LNA) is proposed.

The dynamic amplifier is shown in Fig.3 (a). It uses common gate–common source (CG-CS) coupling and complimentary current reuse structure to accomplish low noise and low power operation. LNAs have used CG-CS coupling for its noise cancellation properties. But in the proposed low-power baseband LNA, the input impedance of the CG devices are much higher than the source impedance, thus limiting the amount of CG-CS noise cancellation. Still, the noise reduction properties of CG-CS coupling makes it attractive for low power amplifiers.

The noise reduction can be explained by noting that due to CG-CS coupling, signal gain is twice that of the device noise gain. For the same power, this higher signal to device noise ratio at the amplifier output reduces amplifier noise contribution towards NF by a factor of 4 comparing to a non-CG-CS coupling structure. Amplifier power efficiency is further enhanced by adopting a complementary structure for current reuse.

Dynamic biasing technique is used to realize CG-CS coupled structure in baseband, as conventional AC coupling with resistor based DC biasing will either result in gigantic passive devices or significantly higher NF due to the biasing circuit. Dynamic biasing for an amplifier involves storing the required biasing voltage across a capacitor during a reset mode and later using this stored voltage to keep the amplifier in proper operating region while it amplifies the signals. Dynamic amplifier control signal is given in Fig.3 (b). Fig 3 (c) shows the reset mode of proposed amplifier during which the amplifying devices are diode connected and their gate to source voltages are stored across capacitors. Illustrated in Fig. 3 (d) is the active mode, during which the CG-CS coupled devices amplify the signal while the biasing capacitors keep them in their proper operating region. The reset mode of the dynamic amplifier causes disruption to signal amplification. Continuous signal amplification is enabled by interleaving two dynamic amplifiers, with one being active and the other being off or in reset. This only cause negligible power consumption overhead

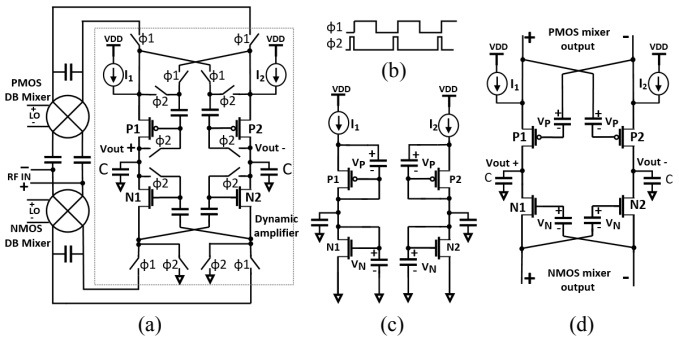


Fig.3 (a) Mixer-embedded dynamic baseband LNA design; (b) active-reset control signal; (c) reset mode; (d) active mode

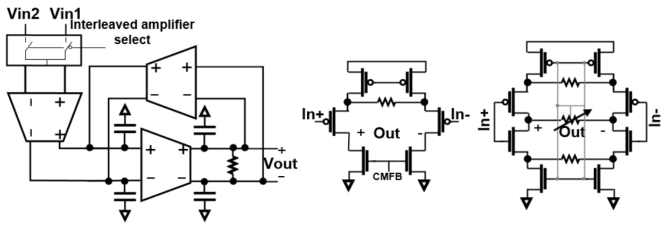


Fig.4 (a) g_mC biquad; (b) g_m cell in the biquad; (c) PGA

as the inactive amplifier is turned off most of the time and only turned to reset for a small fraction of the overall time-interleaving cycle. Thanks to the circuit architecture, this mixer-embedded analog frontend has a high gain of 42dB and NF of 11dB while only consuming 37uA current. The simulated NF improvement by using CG-CS coupling is 2.7 dB, as improvement is limited by mixer noise contribution.

The complex pole filter [8] after dynamic amplifier is shown in Fig. 4 (a) (b). The biquad is followed by a programmable gain amplifier (PGA) shown in Fig. 4 (c) whose gain can be varied from 0dB to 18dB. The entire signal chain has a 60dB peak gain with 6dB tuning step and a 2MHz typical bandwidth.

B. Frequency Synthesizer

As phase coherence is not required for MC-OOK demodulation, a frequency lock loop (FLL) is sufficient for generating the WUR LO signal. The FLL architecture is shown in Fig. 5, similar to the one in [4]. The reference clock is a 32.768kHZ RTC from the Wi-Fi platform, minimizing the Wi-Fi system overhead when it is in sleep mode. The LO frequency tuning step is 0.5MHz, achieved by a programmable counter. The simulated FLL frequency variation caused by the counter's quantization error is within ±0.2MHz. As a result, the overall LO frequency error is <0.5MHz without calibration, causing <0.5dB WUR signal power loss in a 2MHz-bandwidth baseband.

Based on analysis, for achieving sufficient phase noise performance that leads to similar Wi-Fi blocker tolerance as main Wi-Fi radio, LC-VCO is a lower power option than ring-VCO for WUR receiver. The LC-VCO design is shown in Fig. 5. The design is highly area constrained, with a 10nH inductor achieving a quality factor of 6 at 2.4GHz, which limits the VCO swing. A VCO buffer is then used for amplifying the swing by about 4 times at the cost of worsened but still sufficient phase noise performance.

C. ADC and DBB

An 802.11ba-based DBB is integrated with the WUR frontend. The DBB is constantly monitoring the wireless channel for frontend automatic gain control and WUR preamble detection. Upon WUR packet acquisition, WUR data frame is demodulated and parsed.

Different from using a single bit ADC [1-3], a 7-bit asynchronous SAR-ADC is adopted for digitization. Multiple ADC output bits not only provide wider dynamic range, but also provide flexibility for DBB to correct frontend non-idealities, such as DC offset and filter out any low frequency noise. Both the ADC and the DBB is driven by an

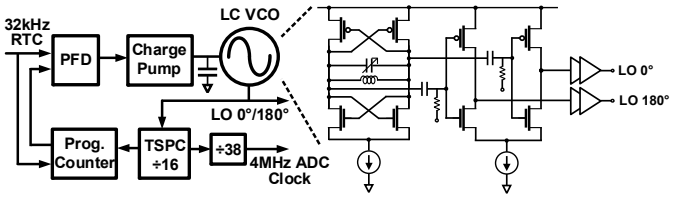


Fig. 5 FLL block diagram and LC-VCO design

approximately 4MHz clock, which is 1/608 of LO frequency. This results in <2% clock frequency error for various 2.4GHz bands and it is also corrected by the DBB using a frequency/timing tracking algorithm.

D. WUR and Wi-Fi Integration

As shown in Fig. 2, the WUR receiver frontend is connected in parallel to the Wi-Fi receiver, interfacing the Wi-Fi transmitter with the same T/R switch. A step-up matching network is embedded within the T/R switch, providing passive voltage gain for both WUR and Wi-Fi receiver, improving their sensitivity.

The WUR receiver requires 0.9V supply for RF/analog frontend and 0.6V supply for DBB. For WUR system integration, a 1.1V switching supply is used. Multiple micro-LDOs (µLDOs) were designed for WUR internal supplies for noise isolation. The µLDOs filter switching supply noise at WUR signal frequency (<2MHz), improving front end sensitivity, and at Wi-Fi blocker frequency (>15MHz), for LC-VCO phase noise performance. The four µLDOs combined consume 16µA quiescent current and occupy 0.01mm^2.

IV. Measurement Results

The integrated 802.11ba-based WUR receiver and 802.11a/b/g/n/ac Wi-Fi transceiver is fabricated in 28nm CMOS technology. Fig. 6 shows photos of two sections of the WUR design (surrounding Wi-Fi blocks are not shown). The active area for the WUR frontend blocks measures 0.05mm^2 while the DBB measures 0.08mm^2. Table 1 shows a current consumption breakdown of the receiver during active WUR packet acquisition. The total current consumption is 606µA, leading to a total power consumption of 495µW with 0.9V RF/analog supply and 0.6V digital supply. While integrated within the Wi-Fi chip, the WUR receiver consumes 667µW from a 1.1V system power supply. The majority of the current consumption comes from the LC-VCO, which is limited by the adoption of a low-Q inductor for saving silicon area.

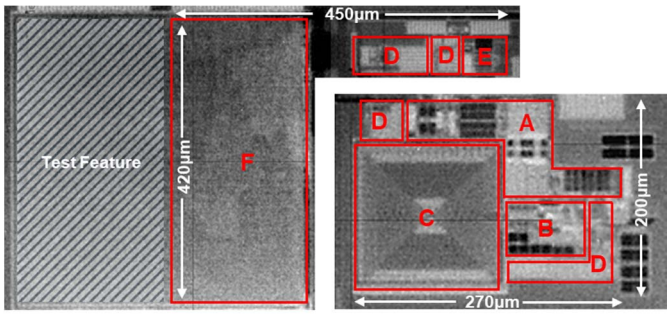
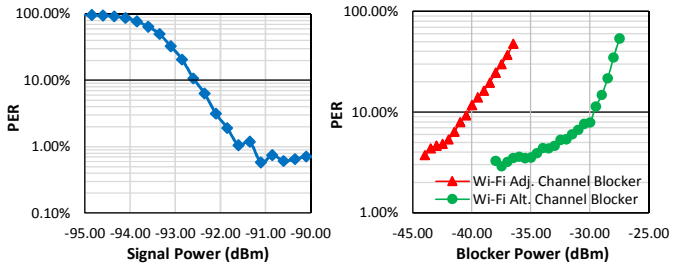


Fig. 6 Chip photo: (A) RF/analog frontend, (B) FLL, (C) VCO inductor, (D) µLDOs, (E) ADC, (F) DBB

Table 1. WUR Receiver Current Consumption Breakdown

	VCO and LO Driver	RF/analog frontend	ADC	DBB	Total
Current (µA)	325	86	25	170	606



(a) (b)

Fig. 7 (a) WUR sensitivity performance; (b) WUR receiver Wi-Fi blocker tolerance performance (-89.6dBm WUR signal input)

The WUR receiver is operated in 802.11ba mandatory mode at 2.4GHz band with 62.5kbps data rate. Fig. 7 (a) shows the receiver sensitivity performance, with WUR packet containing Wi-Fi legacy preamble, WUR preamble and a 64-bit data field. As shown in Fig. 7 (a), we can achieve -92.6dBm sensitivity for 10% PER. Fig. 7(b) shows Wi-Fi blocker tolerance of the receiver. With 3dB receiver de-sensitization, the WUR can tolerate -40.5dBm or -30dBm Wi-Fi blockers from non-overlapping adjacent channel (25MHz offset) or alternate channel (50MHz offset). This corresponds to signal to interference ratio (SIR) of -49dB and -60dB respectively.

Wi-Fi system wake-up through WUR was demonstrated over the air. The WUR can monitor the wireless channel for wake-up packet while the Wi-Fi system is in sleep mode. Upon successfully receiving an 802.11ba-based wake-up packet, the WUR receiver generates a wake-up interrupt signal that is routed to a Wi-Fi system controller and turns on the Wi-Fi main radio. When WUR is turned-off, no performance degradation is observed for the Wi-Fi radio as compared to the original Wi-Fi transceiver without WUR.

Table 2 shows a comparison for state-of-art WUR designs. This work is the first reported 802.11ba-based WUR design and also the first integration of WUR receiver with Wi-Fi chip. Compared to [2-4] which has no DBB, this work with full WUR receiver can achieve state-of-art sensitivity, blocker tolerance and power consumption without requiring external components while maintaining a highly compact area which eases Wi-Fi system integration.

V. Conclusion

The first-ever 802.11ba-based WUR receiver as well as its integration prototype with an 802.11a/b/g/n/ac Wi-Fi transceiver is demonstrated in this paper. WUR receiver can achieve state-of-art -92.6dBm sensitivity, >49dBr Wi-Fi adjacent channel blocker tolerance and 495µW power consumption without using external passive components while occupying 0.13mm^2 silicon area. This demonstration shows low-cost, high performance 802.11ba-based WUR and high performance Wi-Fi main radio can co-exist.

Table 2. State-of-art WUR receiver comparison

	[2]	[3]	[4]	This work
Process	65nm	40nm	14nm	28nm
Freq. band (GHz)	2.4	5.8	2.4	2.4
Modulation	FSK	OOK/ FSK	MC-OOK	MC-OOK
Data rate (kbps)	25/50	62.5	62.5	62.5
Power supply (V)	0.6	0.5/0.95	0.95	0.6/0.9
Power consumption (µW)	466 (no DBB)	470 (no DBB)	95 (no DBB)	392 (frontend) 495 (w/ DBB)
Sensitivity (dBm)	-102*	-92.5*	-72*	-92.6**
SIR (dB)	<-52†	-24†	-20‡	-57†/-49‡
802.11ba based	No	No	No	Yes
Wi-Fi integration	No	No	No	Yes
External passive components	High Q Inductor	No	No	No
Active area (mm^2)	1.5 (no DBB)	0.17 (no DBB)	0.15 (no DBB)	0.05 (frontend) 0.13 (w/ DBB)

* 0.1% BER, bit level performance only
** 10% PER, including packet acquisition and decoding performance
† Continuous wave blocker @ 20MHz offset
‡ 20MHz bandwidth Wi-Fi blocker @ 25MHz offset adjacent channel

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