

A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

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Abstract

In this paper, a 10 bit 1 GS/s current-steering CMOS D/A converter is presented. The measured INL is better than ± 0.2 LSB. The 1 GS/s conversion rate has been obtained by a fully custom designed thermometer decoder. The dynamic limitations have been solved, resulting in more than 61 dB measured SFDR in the interval from DC to Nyquist at all conversion rates up to 1 GS/s. At this conversion rate, the power consumption equals 110 mW. The chip has been processed in a standard $0.35\mu\text{m}$ CMOS technology and has an active area of only 0.35 mm^2 .

Introduction

The evolution in the field of wireless communications and the mixed signal area pushes the designer to put an increasing amount of effort in the integration of digital and analog systems on one chip. Consequently, the interface between these systems is becoming one of the most challenging blocks to design in the telecommunication devices of today. High performant D/A converters find applications in the area of e.g. HDTV and GSM. Because they are inherently fast and cost effective, CMOS current-steering D/A converters are the ideal candidates for such applications.

Recent papers [1, 2] have revealed that achieving a Nyquist output signal together with a combination of a high accuracy and a high update rate, is a challenge. In [3] more than 60 dB SFDR (spurious free dynamic range) is achieved up to 200 MS/s for a 10 bit D/A converter. The presented chip achieves more than 61 dB SFDR up to 1GS/s and has a small area and power consumption. From the measurements, it will be concluded that the presented chip outperforms all -by the authors known- published D/A converters.

In the next paragraph, the different building blocks of the current-steering D/A converter are discussed in detail, namely the current cell, the switch transistors, the switch driver and the thermometer decoder. The impact of the layout is discussed in the second paragraph followed by the presentation of the measurement results of the realized chip. Finally, a conclusion has been formulated.

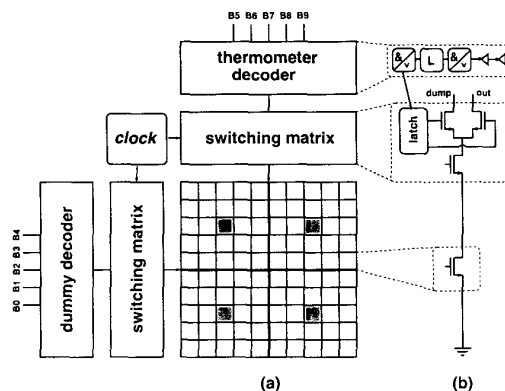


Fig. 1 : Floorplan of the D/A converter

D/A Building Blocks

A. Introduction

The 10 bit D/A converter has been implemented with an equal number of binary and unary bits. Fig.1 shows the floorplan of the 10 bit segmented current-steering CMOS D/A converter. The chip is divided in two sub-blocks. The decoder used to process the MSB's is a thermometer decoder. The LSB's are implemented in a binary way. Here a dummy decoder -with identical cells- has been added so that the latency between the signals generated by the LSB's and those generated by the MSB's is minimized.

Due to the 1 GHz high speed specification, a fully custom decoder has been designed taking all layout parasitics into consideration.

B. The Current Cell

The current cell (fig. 2) consists of three building blocks namely the cascoded current source, a pair of differential switches and the load resistor. Each of these blocks will be discussed in more detail.

Since the D/A converter's performance depends on technology variations, it is important to know the yield specification (the ratio of the number of functional DACs to the number of fabricated DACs) in function of the matching properties of the used technology. This relationship can be

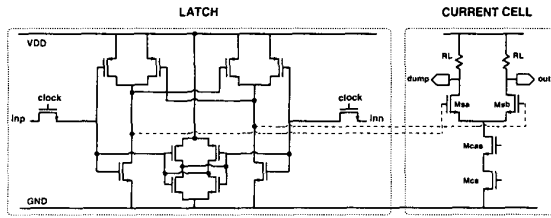


Fig. 2 : The switch driver and the current cell

found using Monte Carlo simulations or statistically. The dimensions of the current source transistors are given by [4] :

$$W^2 = \frac{I}{2KP(\sigma/I)^2} \left[\frac{A_\beta^2}{(V_{GS} - V_T)_{CS}^2} + \frac{4A_{VT}^2}{(V_{GS} - V_T)_{CS}^4} \right] \quad (1)$$

$$L^2 = \frac{KP}{2I(\sigma/I)^2} \left[A_\beta^2 (V_{GS} - V_T)_{CS}^2 + 4A_{VT}^2 \right]$$

If the gate overdrive voltage of the current sources is taken as large as possible, the area consumed by the current source array is small. However, the value of $(V_{GS} - V_T)_{CS}$ is limited by the fact that both the cascode transistor M_{cas} and the switch transistors M_{sa} and M_{sb} have to operate in the saturation region. A trade-off has to be made. For the given technology, the dimensions of the unit current source transistor are given by a width W of $2 \mu\text{m}$ and a gate-length L of $8 \mu\text{m}$ for a yield specification of 99.7 %.

As is generally known, the impedance seen in the drain of the switch transistors Z_{imp} of each current cell has to be made large so that its influence on the INL (integral non-linearity) specification of the DAC is negligible. The relation between this impedance and the achievable INL specification is given by [5] :

$$INL = \frac{I_{unit} R_L^2 N^2}{4Z_{imp}} \quad (2)$$

with R_L the load resistor, I_{unit} the LSB current and N the total number of unit current sources. The cascode configuration of the switch and current source is high enough to achieve the INL specification. However, this is only true over a limited frequency bandwidth since the impedance Z_{imp} is frequency dependent as is indicated in fig. 3. The impedance that is required to obtain a certain resolution can be calculated and approximately equals [6] :

$$Z_{imp} \approx \frac{NR_L}{4Q} \quad (3)$$

with Q the ratio between the signal and the second order harmonic. This formula indicates that for a 10 bit accuracy, Z_{imp} has to be at least $6.5 \text{ M}\Omega$. Using a regular current source the obtainable Nyquist frequency is about 100 MHz . Going to higher operation frequencies, the frequency dependency of Z_{imp} has to be adjusted by using a cascoded current source. In this case the obtainable Nyquist frequency f_{obt} is about 10 times higher than the one obtained by a non-cascoded current source. This is qualitatively shown in fig. 3.

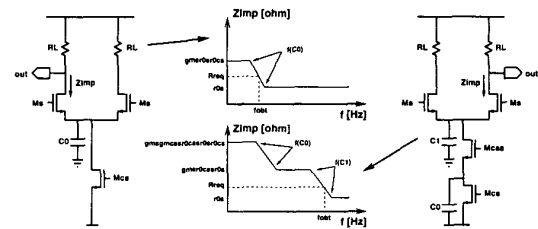


Fig. 3 : The current source with and without cascode transistor

For high speed reasons, the gate-length of the switch transistors is chosen minimal. To determine the width, the gate overdrive voltage of the switches has to be chosen as large as possible since in that case the drain capacitance of these transistors is small. As a consequence the settling time of the D/A converter is improved and the glitch energy error introduced by this capacitance is lowered. However, the value of $(V_{GS} - V_T)_{sw}$ is limited by the operation of the cascoded current source.

C. The thermometer decoder

Designing a thermometer decoder using standard cell libraries has the great disadvantage that the achievable operation speed is limited by the timing constraints of the used cells. Therefore, the decoder has been manually designed and layouted at transistor level.

After regeneration of the incoming digital signals, the 32 outputs of the thermometer decoder are generated by a three stage logic chain as is depicted in fig. 1. The first and third block are identical and perform a simple NOR and NAND operation. The logic block L is actually a four input NANDNOR used to realize all the necessary combinations of the terms generated by the first block. It can be concluded that only three blocks are necessary to build the entire decoder. The layout of these blocks has been optimized to area and symmetry. Wherever necessary, dummy blocks and/or interconnects have been included as to match the loads and avoid timing mismatches. The maximum achievable operation speed of this decoder exceeds 1 GHz .

D. The synchronization block

The problems causing a degradation of the dynamic performance of a current steering D/A converter can nowadays be solved by the use of one well designed and carefully layouted synchronized driver placed immediately in front of the switches (fig. 2).

The main function of this driver is the shifting of the crossing point of the switch transistor control signals so that these transistors are never simultaneously in the off-state. Since the driver is clocked and placed immediately in front of the switches, the delay introduced by the digital decoding logic - leading to a timing difference between the control signals of the switches - can be circumvented. Furthermore, the glitch energy error caused by the C_{GD} feed-through is significantly lowered by the use of a reduced voltage swing at the input of

the switches. This is also be realized by the same driver circuit. The circuit schematic of the driver circuit is given in fig. 2.

Layout

To compensate for symmetrical and graded errors caused by the temperature, process and electrical gradients, special switching schemes are implemented nowadays [1,7]. In this design, the current source of the unary array is divided into 4 current sources each delivering 8 times the LSB current. In every quadrant a current source is placed based on the switching scheme presented in [8]. Since in each quadrant 31 current sources have to be placed, a 6*6 array is used. The five remaining places are occupied by the binary bits and the bias transistor Mo. Four dummy rows and columns have been added as to avoid edge effects. A graphic representation of the structure of the current source array is given in fig. 4. The shaded area represents the dummy cells.

The switch driver and the switches are placed in a separate array from the current sources. This is done to avoid coupling between the digital and the analog block. Furthermore, guard rings have been placed.

The cascode transistor Mcas (fig. 2) has also been placed in the switch array because otherwise this transistor loses its purpose. From the Bode diagram depicted in fig. 3 it becomes clear that C1 has to be as small as possible since the second pole and zero are determined by this capacitance. The capacitance introduced by the interconnections is then situated at the drain node of the current source transistors and is given by C0.

To minimize the systematic error introduced by the voltage drop in the ground lines of the current source transistors, sufficiently wide lines have been used and are drawn on top of the transistors. Also the interconnections needed to implement the switching scheme are drawn over the transistors. In this way, a very compact current source array has been realized.

Throughout the whole design, layout parasites have been taken into account and symmetry has been introduced. At layout level this implies that all the connections have been

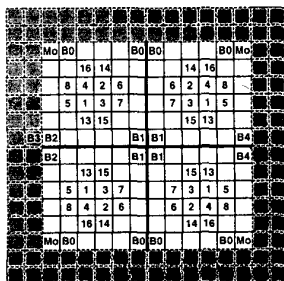


Fig. 4 : The structure of the current source array

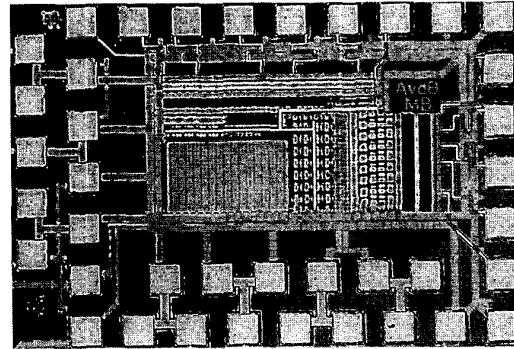


Fig. 5 : Chip photograph of the 10 bit D/A converter

made identical. This is not only true for the interconnections between any of the digital blocks, but also for e.g. the interconnection between the switch driver and the switch transistors. Wherever possible all blocks have the same load. For this purpose dummy switch transistors have been introduced for the binary bits.

Much attention has been paid at the final layout of the chip. One of the main goals was the minimization of the used silicon area. Most of the routing runs on top of the transistors and occupies no extra area. This leads to a 10 bit D/A converter with an active area of only 0.35 mm² which is better than that of other published high performance 10 bit current-steering D/A converters [3]. Fig. 5 shows a chip photograph of the realized design.

Measurement results

All measurements have been performed on a single ended 50Ω double terminated output. The analog voltage supply is 3V, while the digital part of the chip operates at only 1.9V.

Figure 6 shows the measured INL and DNL of the 10 bit CMOS D/A converter. The INL is smaller than +/- 0.2 LSB proving the 10 bit accuracy. The DNL error lies between -0.1 LSB and 0.15 LSB.

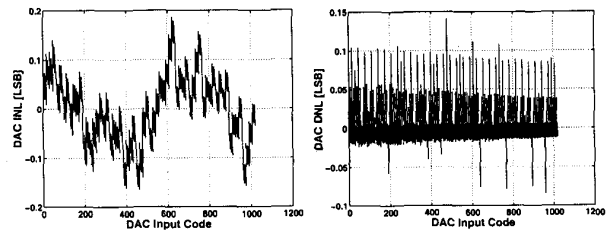


Fig. 6 : The measured INL and DNL specification

The D/A converter has been measured for different conversion rates up to a 1Gsample/s, which is the limit of the measurement equipment. For all the measurements a SFDR of over 61 dB has been measured in the interval from DC to the Nyquist range. An overview of the measured dynamic results is given in fig. 7. Figures 8 and 9 show some typical measured output spectra for a 1 GS/s clock rate.

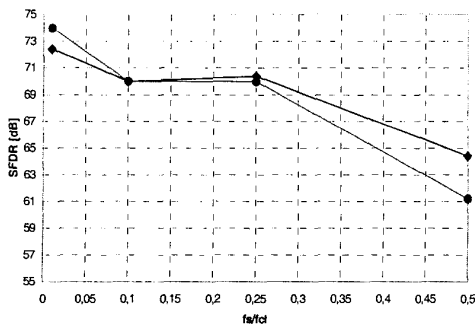


Fig. 7 : The SFDR of the 10 bit D/A converter for a conversion rate of 100 MS/s (◆) and 1 GS/s (●)

The power consumption has been measured for a 490 MHz input signal at a sample frequency of 1 GS/s. The digital part of the chip (the regenerative buffers at the input, the two decoders and the switch driver) consumes only 62 mW while the analog part consumes 48 mW. The total power consumption equals 110 mW.

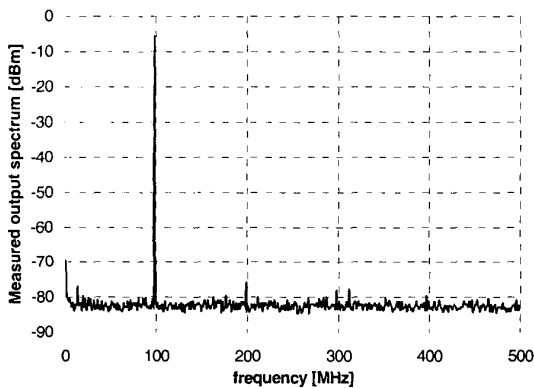


Fig. 8 : The output spectrum for a 100 MHz signal @ 1GS/s

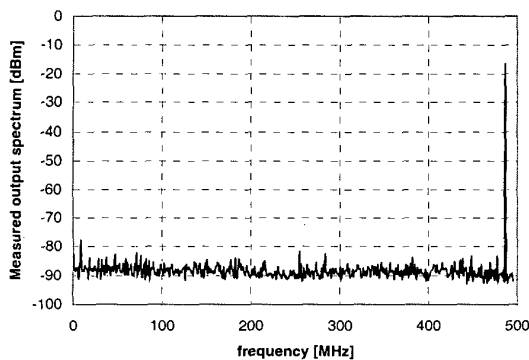


Fig. 9 : The output spectrum for a 490 MHz signal @ 1 GS/s

Table I summarizes the specifications of the 10 bit 1 GS/s current-steering CMOS D/A converter.

TABLE I
CHARACTERISTICS OF THE D/A CONVERTER

Resolution	10 bit
Update rate	Up to 1 GS/s
INL	< 0.2LSB
DNL	< 0.15 LSB
SFDR (490MHz@1GS/s)	61.2 dB
Analog/digital voltage supply	3V / 1.9 V
Power consumption	110mW (490MHz@1GHz)
Active area	0.35 mm ²
Process	0.35 μm CMOS

Conclusion

In this paper, the first 1GS/s, full Nyquist, 10 bit CMOS current-steering D/A converter has been presented. Due to the fully custom decoder and the especially designed switch driver, the D/A converter achieves a conversion rate of 1 GS/s. The dynamic limitations have been analyzed and solved, resulting in a full Nyquist behavior up to 1GS/s, which was the maximal speed of the measurement equipment. The D/A converter has a 16 mA full swing output current and consumes 110 mW for a 490 MHz input signal at a 1 GS/s clock. Much attention has been paid at the layout. Not only have the layout parasitics been taken into account during the design phase, also the floorplan of the analog and digital block has been studied to minimize the chip area. The D/A converter has been processed in a standard 0.35 μm CMOS technology and has an active area of only 0.35 mm².

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